

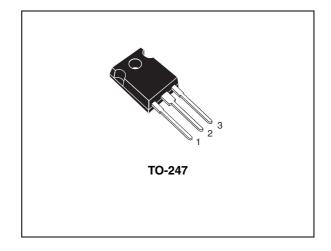
STW43NM60ND

N-channel 600 V, 0.075 Ω, 35 A TO-247 FDmesh[™] Power MOSFET (with fast diode)

Features

Туре	V _{DSS} @ T _{JMAX}	R _{DS(on)} max	I _D
STW43NM60ND	650 V	< 0.088 Ω	35 A

- The worldwide best R_{DS(on)}*area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities.



Application

Switching applications

Description

The FDmesh™ II series belongs to the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout and associates all advantages of reduced onresistance and fast switching with an intrinsic fast-recovery body diode.It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters.

Figure 1. Internal schematic diagram

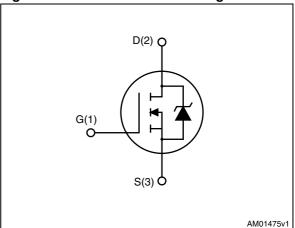


Table 1. Device summary

Order code	Marking	Package	Packaging	
STW43NM60ND	43NM60ND	TO-247	Tube	

February 2011 Doc ID 14402 Rev 4 1/13

Contents STW43NM60ND

Contents

1	Electrical ratings 3
2	Electrical characteristics 4
	2.1 Electrical characteristics (curves) 6
3	Test circuits8
4	Package mechanical data
5	Revision history12

STW43NM60ND Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	600	V
V _{GS}	Gate-source voltage	± 25	V
I _D	Drain current (continuous) at T _C = 25 °C	35	Α
I _D	Drain current (continuous) at T _C = 100 °C	22	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	140	Α
P _{TOT}	Total dissipation at $T_C = 25$ °C	255	W
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Max. operating junction temperature	150	°C

^{1.} Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.49	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T _I	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	14	Α
E _{AS}	Single pulse avalanche energy (starting T _J =25 °C, I _D =I _{AS} , V _{DD} =50 V)	1000	mJ

^{2.} $I_{SD} \leq 35$ A, di/dt ≤ 600 A/ μ s, $V_{DD} = 80\%$ $V_{(BR)DSS}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	600			٧
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, @125 °C			10 100	μ Α μ Α
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	٧
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 17.5 A		0.075	0.088	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =15 V _, I _D = 17.5 A	-	17	-	S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V, } f = 1 \text{ MHz,}$ $V_{GS} = 0$	-	4300 250 25	-	pF pF pF
C _{oss eq.} (2)	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V	-	530	-	pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}, I_{D} = 35 \text{ A},$ $V_{GS} = 10 \text{ V},$ (see Figure 15)	-	145 18 80	-	nC nC nC
R _g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	1.7	-	Ω

^{1.} Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

^{2.} $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300 \text{ V}, I_{D} = 17.5 \text{ A}$ $R_{G} = 4.7 \Omega V_{GS} = 10 \text{ V}$ (see Figure 14)	-	30 40 120 50	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current		_		35	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				140	Α
V _{SD} (2)	Forward on voltage	I _{SD} = 35 A, V _{GS} = 0	-		1.3	V
t _{rr}	Reverse recovery time	$I_{SD} = 35 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		190		ns
Q_{rr}	Reverse recovery charge	V _{DD} = 100 V	-	1.6		μC
I _{RRM}	Reverse recovery current	(see Figure 16)		17		Α
t _{rr}	Reverse recovery time	$I_{SD} = 35 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		280		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 150 ^{\circ}\text{C}$	-	3.0		μC
I _{RRM}	Reverse recovery current	(see Figure 16)		22		Α

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: Pulse duration = $300 \mu s$, duty cycle 1.5%

Electrical characteristics STW43NM60ND

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

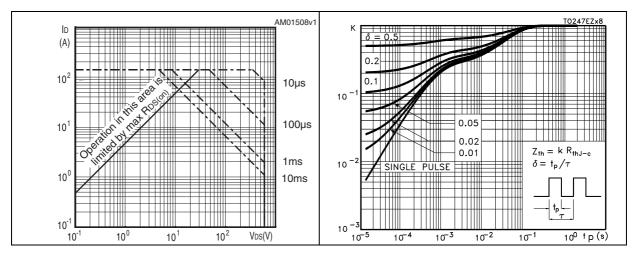


Figure 4. Output characteristics

Figure 5. Transfer characteristics

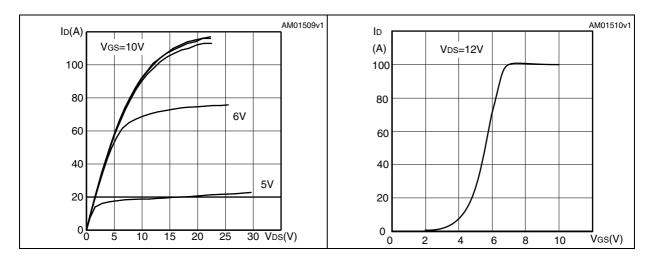
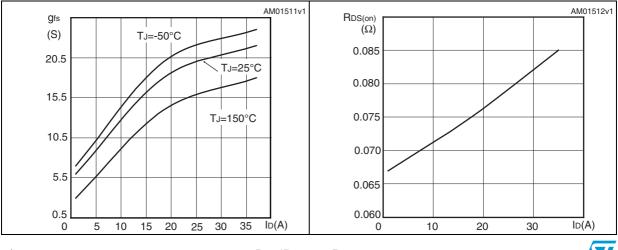


Figure 6. Transconductance

Figure 7. Static drain-source on resistance



6/13 Doc ID 14402 Rev 4

Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

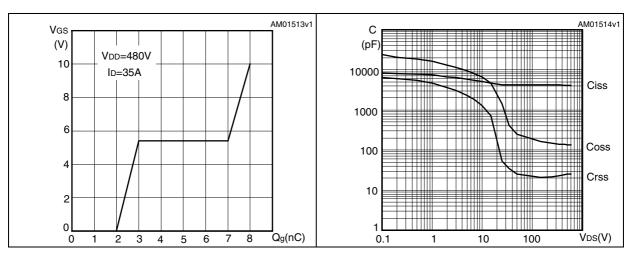


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

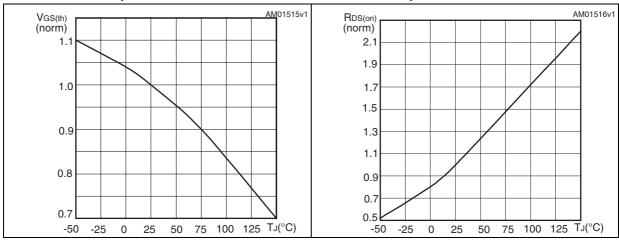
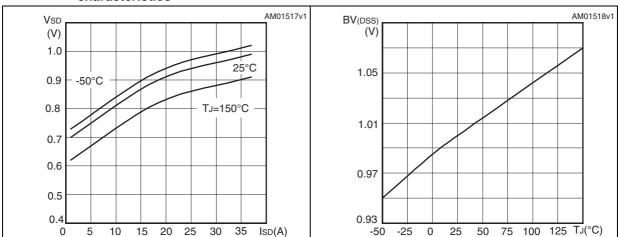


Figure 12. Source-drain diode forward characteristics

Figure 13. Normalized \mathbf{B}_{VDSS} vs temperature



577

Test circuits STW43NM60ND

3 Test circuits

Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

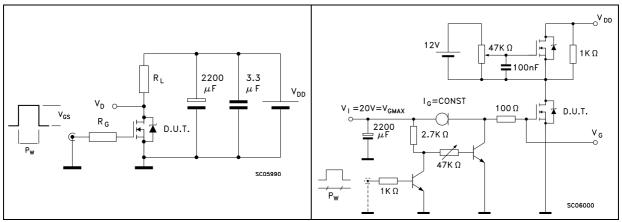


Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped inductive load test circuit

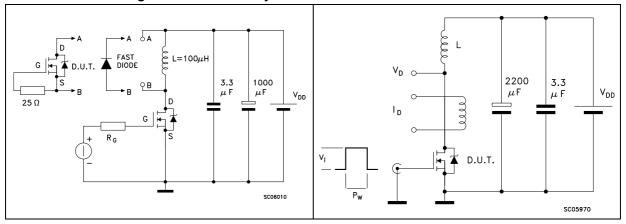
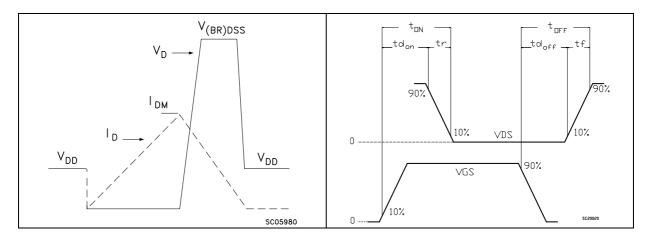


Figure 18. Unclamped inductive waveform

Figure 19. Switching time waveform



8/13 Doc ID 14402 Rev 4

4

4 Package mechanical data

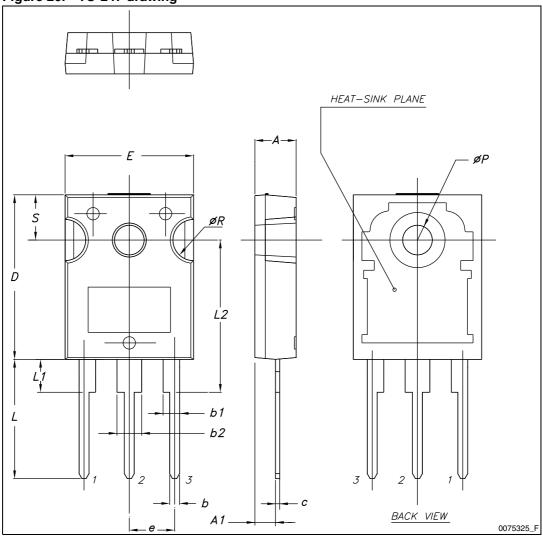
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Table 9. TO-247 mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	b2 3.0		
С	0.40		0.80
D	19.85		20.15
E	15.45		15.75
е		5.45	
L	L 14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 20. TO-247 drawing



57

Revision history STW43NM60ND

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Feb-2008	1	First release
22-Jan-2009	2	Document status promoted from preliminary data to datasheet.
16-Feb-2010	3	Figure 13: Normalized B _{VDSS} vs temperature has been corrected.
14-Feb-2011	4	I _{DSS} value in <i>Table 5</i> has been corrected.

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Doc ID 14402 Rev 4

13/13