Si834x Data Sheet

Isolated Smart Switch

The Si834x provides four isolated high-side or low-side switches with low R_{ON}. These switches are ideal for driving resistive and inductive loads like solenoids, relays, and lamps commonly found in industrial control systems like Programmable Logic Controllers (PLC). Each switch is galvanically isolated for safety using Skyworks' groundbreaking CMOS-based isolation technology, offering better reliability and performance than the traditional optocoupler-based isolation, including high Common-Mode Transient Immunity (CMTI) over 100 kV/µs.

The logic interface supports low-power 2.25 V MCUs, while the switches offer a wide supply range of 9 V – 32 V ideal for industrial voltage levels. The switches are capable of providing 0.7 A depending on load conditions. Each switch offers complete fault protection. An innovative multi-voltage clamp efficiently handles an unlimited amount of demagnetization energy (E_{AS}). The over-current protection includes an Inrush Current Mode to drive loads like lamps. Additionally, the device power supplies are monitored, and the switches are safely constrained or shutdown on faults.

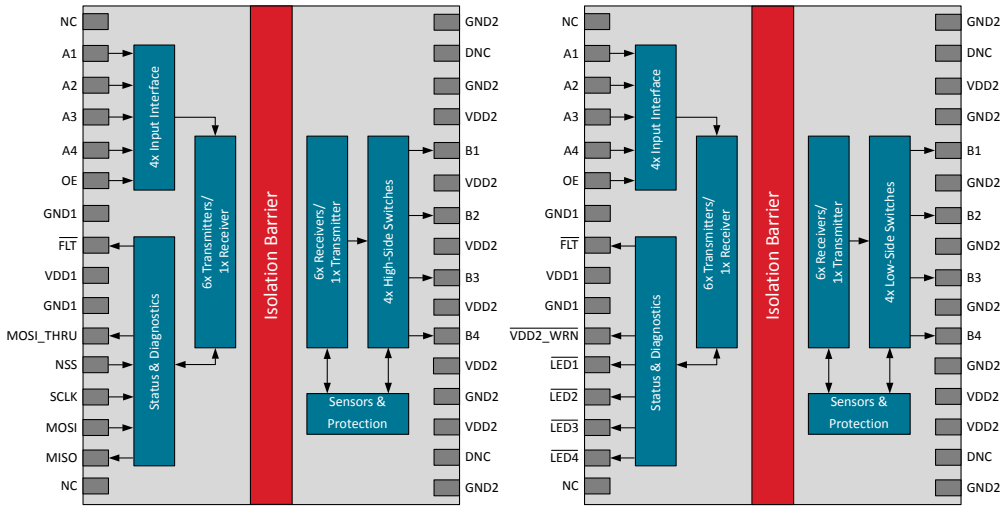
Eight diagnostics are reported through the logic interface, offering an unprecedented level of details and control. Diagnostics are configured, monitored, and cleared via the Serial Peripheral Interface (SPI) or exposed on active-low, open-drain indicator pins for easy access and combination. Diagnostic communication is independent of switch control signals, with separate isolation channels and constant error checking, ensuring long-term reliability.

Applications

- Programmable logic controllers
- Industrial data acquisition
- Motion controllers
- Smart solid-state relays

Safety Approvals (Pending)

- UL 1577 recognized: Up to 1500 Vrms for 1 minute
- CSA certified under: IEC 60950-1, 62368-1
- VDE certification conformity: VDE 0884-10
- CQC certification approval: GB4943.1



Si83408AFA-IF **Si83414AAA-IF**

KEY FEATURES

- High-side or low-side switch
- Logic Supply: 2.25 V – 5.5 V
- Switch Supply: 9 V – 32 V
- Fast (10 µs) update rate
- High continuous current (700 mA) and low R_{ON} (145 mΩ)
- Unique multi-voltage output clamp
  - Unlimited demagnetization (E_{AS})
  - Efficient and fast turn-OFF
- Inrush Current Mode: 8 A for 20 ms
- Current-limited overload protection
- Over-temperature protection
- Undervoltage protected supplies
- Up to 8 different diagnostics
  - Multiple power supply reports
  - Over-current, over-temperature
  - Open-circuit warning
  - Communication error
- Channel status indicators
- Dedicated fault indicator
- Disable outputs asynchronously
- Control 128 channels via SPI
- 1.5 kV_{RMS} safety rated isolation
- Transient immunity > 100 kV/µs
- Compliant to IEC 61131-2
- Compact 9x9 DFN-32 package
- 5 kV ESD Protection
- -40 – 125 °C operating temperature

1. Ordering Guide

Table 1.1. Si834x Ordering Guide

Ordering Part Number	Output[1] Switch Type	Input[2] Interface	Output Channels	Continuous Output Current	Channel Status Indicators	Low Voltage Indicator	Open Channel Indicator	Clear Fault Input	Iso. Rating
Products Available Now									
Si83404AAA-IF	Sourcing	Parallel	4	0.7 A	Yes	Yes	No	No	1.5 kVrms
Si83408ADA-IF		SPI				No	No	No	
Si83408AFA-IF		Parallel/ SPI			No	No	No	No	
Si83414AAA-IF	Sinking	Parallel	4	0.7 A	Yes	Yes	No	No	
Si83418ADA-IF		SPI				No	No	No	
Si83418AFA-IF		Parallel/ SPI			No	No	No	No	
Contact Skyworks Sales for These Options									
Si83404ABA-IF	Sourcing	Parallel	4	0.7 A	Yes	No	Yes	No	1.5 kVrms
Si83404ACA-IF						No	No	Yes	
Si83414ABA-IF	Sinking	Parallel	4	0.7 A	Yes	No	Yes	No	
Si83414ACA-IF						No	No	Yes	

Note:

1. Output switch can source current in a high-side, open-source configuration or sink current in a low-side, open-drain configuration.
2. SPI provides access to all diagnostic, configuration, and channel status information. Devices without a parallel interface allow output channel control through the SPI as well.
3. "Si" and "SI" are used interchangeably.
4. An "R" at the end of the Ordering Part Number indicates tape and reel option.

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2. System Overview

A single channel of the Si834x Isolated Smart Switch is analogous to that of an optocoupler and a relay driver, except that an RF carrier is modulated across the isolation barrier instead of light. This simple architecture provides a robust isolation path and requires no special considerations or initialization at startup. The RF carrier is modulated using methods that optimize fault tolerance and propagation delay across the isolation barrier.

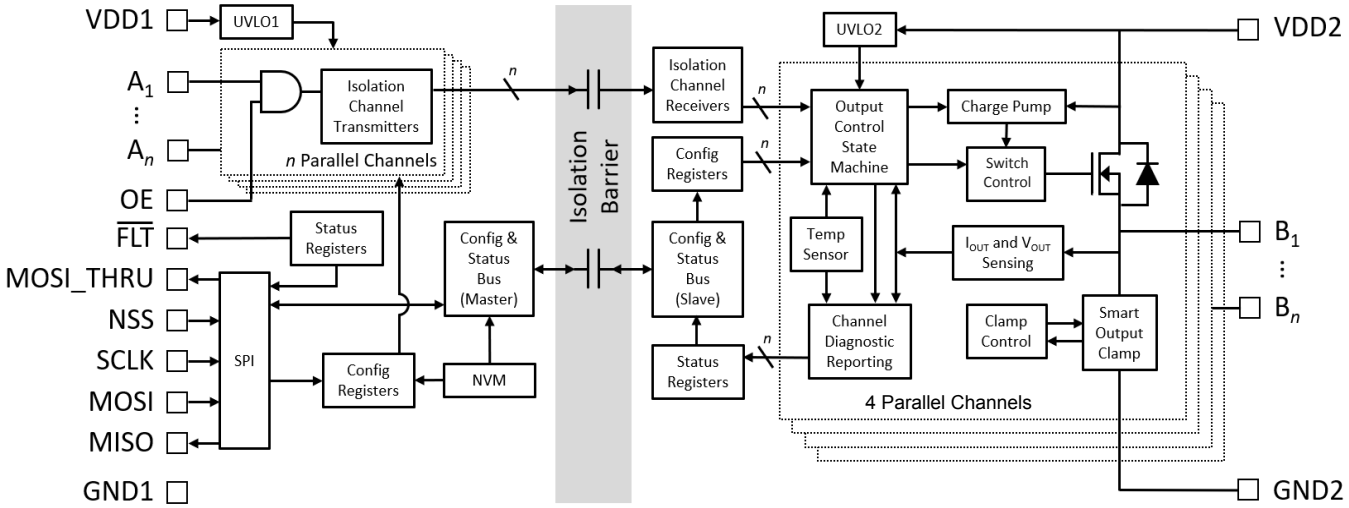


Figure 2.1. Parallel/SPI Sourcing Device System Diagram

The fundamental channel structure described above is augmented using a number of innovative technologies. The output switch is a low ON-State Resistance (R_{ON}) device capable of driving inductive and resistive loads at continuous currents of 700 mA. It includes precise voltage, current, and temperature sensors that continuously monitor the switch and load conditions, protecting the device by reducing driver performance or forcing a controlled shutdown when necessary.

The switch uses a sophisticated multi-voltage output clamp, called a “smart output clamp”, that both protects the switch from harmful inductive kickback voltage (or back EMF) while still offering fast demagnetization of inductors to reduce contact arcing and increase switching speed.

Four identical channels are packaged together into an Si834x device, each with its own set of sensors. Switches are controlled using dedicated isolation channels which increase reliability and timing performance. A bidirectional, fault-tolerant isolation channel is also implemented between the switch and logic interface, allowing the host controller to configure, monitor, and diagnose the switches and their loads.

The logic interface offers dedicated parallel input channels and an asynchronous output enable (OE) pin for high speed switch control as well as a rich SPI for diagnostics and monitoring. Eight different diagnostic reports are available in the device status registers accessed via SPI which provide a complete picture of device and load condition. See Diagnostics and Monitoring for more information on the available reports.

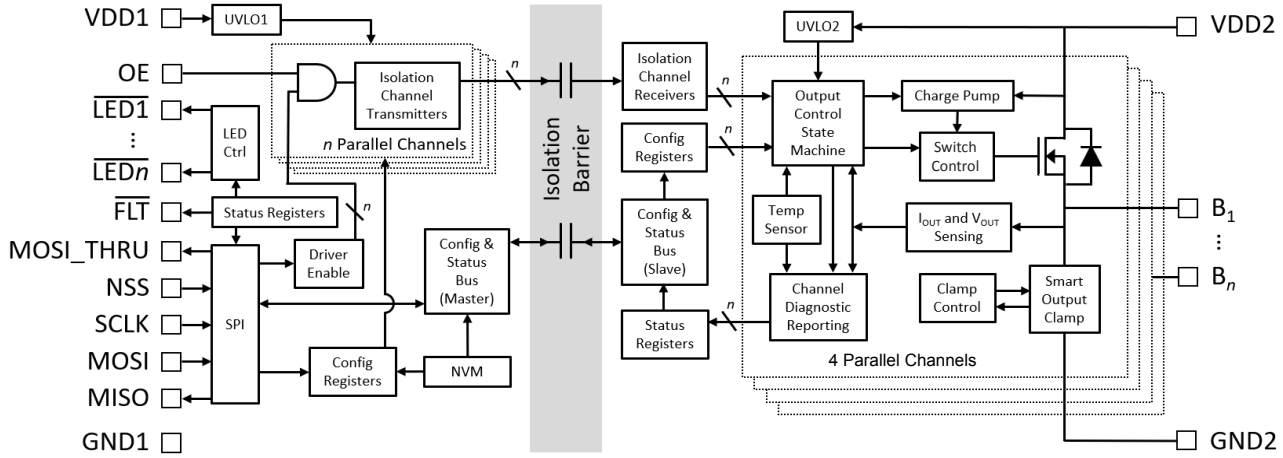


Figure 2.2. SPI Sourcing Device System Diagram

The true status of each switch output is communicated across the isolation barrier to the logic interface and can be monitored by the controller through the status registers. On some product options, such as the one depicted in the figure above, the channel status is also indicated by open-drain, active-low LED output pins that can quickly provide end-user feedback on switch status.

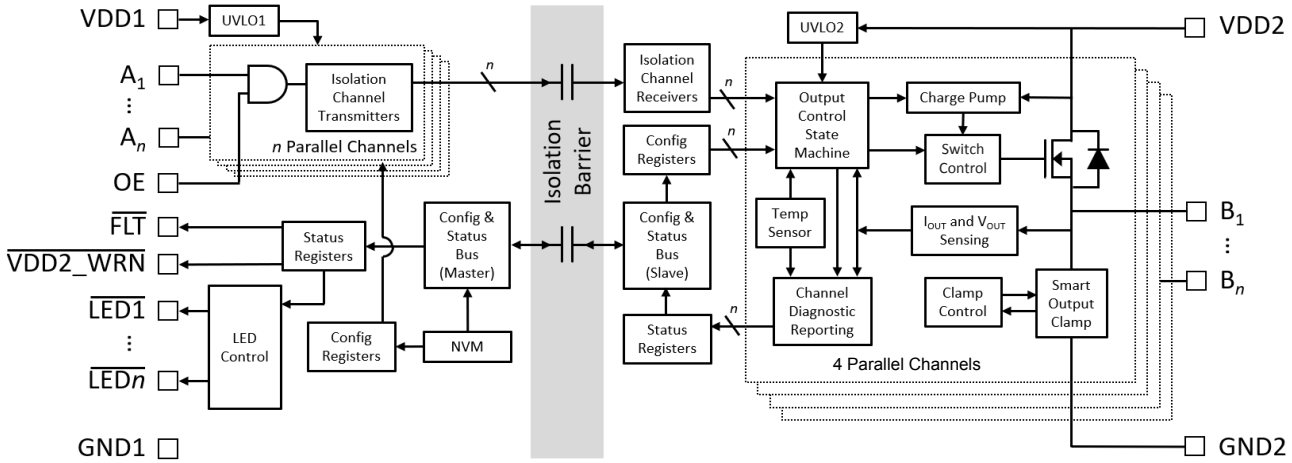


Figure 2.3. Parallel Interface Device System Diagram

The Si834x is also offered without the SPI to simplify designs and provide an easy migration path from existing optocoupler-based solutions, as illustrated in the figure above. Depending on the device selection, different switch diagnostics are exposed using additional indicator pins, such as a switch supply voltage low indicator (VDD2_WRN\).

3. Device Operation

This section describes the capabilities of the Si834x Isolated Smart Switch devices and how they should be used to achieve different goals within a design. Refer to the Ordering Guide and Recommended Application Circuits for information on each device and how they are designed into different applications.

3.1 Truth Tables

The following tables describe the logical behavior of the Si834x Isolated Smart Switch devices. Use these tables to determine the state of a specific channel's outputs on a specific Si834x device, based on the device's current and past state, and its current inputs. The state of other device channels also impacts some channel output states. When applicable, this is described in the table's footnotes.

Table 3.1. Si834xxxAx Truth Table

Mode	Inputs[1]		State[2]				Outputs			
	An	OE	$VDD1_Q$[3]	$VDD2_Q$[4]	$VDD2_{Q-1}$[4]	$Fault_Q$[5]	VDD2_WRN\[6, 7]	FLT\[6]	LEDn\[6]	Bn[8]
Fault	X	X	NP	–	–	–	OFF	U	OFF	OFF
	X	X	P	NP	NP	D	OFF	ON	OFF	OFF
	X	X	P	NP	W	D	ON	ON	OFF	OFF
	X	X	P	W	–	D	ON	ON	OFF[9]	OFF[9]
	X	X	P	P	–	D	OFF	ON	OFF[9]	OFF[9]
Normal	L	X	P	W	–	ND	ON	OFF	OFF	OFF
	X	L	P	W	–	ND	ON	OFF	OFF	OFF
	H	H	P	W	–	ND	ON	OFF	ON	ON
	L	X	P	P	–	ND	OFF	OFF	OFF	OFF
	X	L	P	P	–	ND	OFF	OFF	OFF	OFF
	H	H	P	P	–	ND	OFF	OFF	ON	ON

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. "NP" is the "not powered" state, "P" is the "powered" state, "W" is the "warning" state, "ND" is the "not detected" state, "D" is the detected state, and "–" is an irrelevant state. The current state (Q) and the previous state (Q-1) of the device, as well as the current inputs to the device, define the current outputs of the device.
3. "Not powered" (NP) state is defined as VDD1 < $VDD1_{UV}$. "Powered" (P) state is defined as VDD1 > $VDD1_{UV}$. Logic inputs can power VDD1 through an internal diode if its source has adequate current. See Power Supply Characteristics for details.
4. "Not powered" (NP) state is defined as VDD2 < $VDD2_{UV9}$. "Warning" (W) state is defined as $VDD2_{UV9}$ < VDD2 < $VDD2_{UV18}$. "Powered" (P) state is defined as VDD2 > $VDD2_{UV18}$. See Power Supply Characteristics and Protection and Diagnostics for details.
5. The $VDD2_Q$ "not powered" (NP) state forces a $Fault_Q$ "detected" state. $Fault_Q$ state automatically changes to "not detected" (ND) when all fault conditions are removed. Faults are defined in Diagnostics and Monitoring.
6. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See Recommended Application Circuits for more information.
7. VDD2 must remain within a state long enough to be measured for this output to change. If VDD2 changes states sufficiently quickly, this output will remain unchanged. See Diagnostics and Monitoring for more information.
8. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See Switch Types and Switch Protection for more information.
9. If an Over-Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over-Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally. See Switch Protection for more information.

Table 3.2. Si834xxxBx Truth Table

Mode	Inputs[1]		State[2]						Outputs			
	An	OE	$VDD1_Q$[3]	$VDD2_Q$[4]	$VDD2_{Q-1}$[4]	$Fault_Q$[5]	Bn $Load_Q$	Bn $Load_{Q-1}$	OPEN_CH\[6, 7]	FLT\[6]	LEDn[6]	Bn[8]
Fault	X	X	NP	–	–	–	–	–	OFF	U	OFF	OFF
	X	X	P	NP	NP	D	–	–	OFF	ON	OFF	OFF
	X	X	P	NP	P	D	–	ND	ON	ON	OFF	OFF
	X	X	P	P	–	D	ND	–	ON	ON	OFF[9]	OFF[9]
	X	X	P	P	–	D	D	–	OFF	ON	OFF[9]	OFF[9]
Normal	L	X	P	P	–	ND	ND	–	ON	OFF	OFF	OFF
	X	L	P	P	–	ND	ND	–	ON	OFF	OFF	OFF
	L	X	P	P	–	ND	D	–	OFF	OFF	OFF	OFF
	X	L	P	P	–	ND	D	–	OFF	OFF	OFF	OFF
	H	H	P	P	–	ND	–	–	OFF	OFF	ON	ON

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. "NP" is the "not powered" state, "P" is the "powered" state, "ND" is the "not detected" state, "D" is the detected state, and "–" is an irrelevant state. The current state (Q) and the previous state (Q-1) of the device, as well as the current inputs to the device, define the current outputs of the device.
3. "Not powered" (NP) state is defined as VDD1 < $VDD1_{UV}$. "Powered" (P) state is defined as VDD1 > $VDD1_{UV}$. Logic inputs can power VDD1 through an internal diode if its source has adequate current. See Power Supply Characteristics for details.
4. "Not powered" (NP) state is defined as VDD2 < $VDD2_{UV9}$. "Powered" (P) state is defined as VDD2 > $VDD2_{UV9}$. See Power Supply Characteristics for details.
5. The $VDD2_Q$ "not powered" (NP) state forces a $Fault_Q$ "detected" state. $Fault_Q$ state automatically changes to "not detected" (ND) when all fault conditions are removed. Faults are defined in Diagnostics and Monitoring.
6. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See Recommended Application Circuits for more information.
7. All channels are assumed to have the same load state. A "not detected" (ND) load state on any channel will turn ON this output. The load must remain within a state long enough to be measured for this output to change. If the load changes state sufficiently quickly, this output will remain unchanged. See Diagnostics and Monitoring for more information.
8. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See Switch Types and Switch Protection for more information.
9. If an Over-Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over-Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally. See Switch Protection for more information.

Table 3.3. Si834xxxCx Truth Table

Mode	Inputs[1]			State[2]				Outputs		
	An	OE	FLT_CLR	$VDD1_Q$[3]	$VDD2_Q$[4]	$Fault_Q$[5]	$Fault_{Q-1}$[5]	FLT\[6]	LEDn\[6]	Bn[7]
Fault	X	X	X	NP	–	–	–	U	OFF	OFF
	X	X	X	P	NP	D	–	ON	OFF	OFF
	X	X	X	P	P	D	–	ON	OFF[8]	OFF[8]
Normal	L	X	L	P	P	ND	D	ON	OFF	OFF
	X	L	L	P	P	ND	D	ON	OFF	OFF
	H	H	L	P	P	ND	D	ON	ON[9]	ON[9]
	L	X	H	P	P	ND	D	OFF	OFF	OFF
	X	L	H	P	P	ND	D	OFF	OFF	OFF
	H	H	H	P	P	ND	D	OFF	ON	ON
	L	X	X	P	P	ND	ND	OFF	OFF	OFF
	X	L	X	P	P	ND	ND	OFF	OFF	OFF
	H	H	X	P	P	ND	ND	OFF	ON	ON

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. "NP" is the "not powered" state, "P" is the "powered" state, "ND" is the "not detected" state, "D" is the detected state, and "–" is an irrelevant state. The current state (Q) and the previous state (Q-1) of the device, as well as the current inputs to the device, define the current outputs of the device.
3. "Not powered" (NP) state is defined as VDD1 < $VDD1_{UV}$. "Powered" (P) state is defined as VDD1 > $VDD1_{UV}$. Logic inputs can power VDD1 through an internal diode if its source has adequate current. See Power Supply Characteristics for details.
4. "Not powered" (NP) state is defined as VDD2 < $VDD2_{UV9}$. "Powered" (P) state is defined as VDD2 > $VDD2_{UV9}$. See Power Supply Characteristics for details.
5. The "detected" (D) state will persist as a previous state (Q-1) until the current fault state (Q) is "not detected" (ND) and the FLT_CLR input is high. Faults are defined in Diagnostics and Monitoring.
6. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See Recommended Application Circuits for more information.
7. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See Switch Types and Switch Protection for more information.
8. If an Over-Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over-Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally. See Switch Protection for more information.
9. If a Communication Error Shutdown fault was previously detected and is currently reported, the output will be prevented from turning ON. See Diagnostics and Monitoring for more information.

Table 3.4. Si834xxxDx Truth Table

Mode	Inputs[1]		State[3]			Outputs		
	SW_EN[n][2]	OE	$VDD1_Q$[4]	$VDD2_Q$[5]	$Fault_Q$[6]	FLT\[7, 8]	LEDn\[8]	Bn[9]
Fault	X	X	NP	–	–	U	OFF	OFF
	X	X	P	NP	D	ON	OFF	OFF
	X	X	P	P	D	ON	OFF[10]	OFF[10]
Normal	L	X	P	P	ND	OFF	OFF	OFF
	X	L	P	P	ND	OFF	OFF	OFF
	H	H	P	P	ND	OFF	ON	ON

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. This input is supplied via the SPI from the SW_EN register. Bit addresses are zero indexed such that channel 1 (output B1) is supplied from the SW_EN[0] bit.
3. "NP" is the "not powered" state, "P" is the "powered" state, "ND" is the "not detected" state, "D" is the detected state, and "–" is an irrelevant state. The current state (Q) and the previous state (Q-1) of the device, as well as the current inputs to the device, define the current outputs of the device.
4. "Not powered" (NP) state is defined as VDD1 < $VDD1_{UV}$. "Powered" (P) state is defined as VDD1 > $VDD1_{UV}$. Logic inputs can power VDD1 through an internal diode if its source has adequate current. See Power Supply Characteristics for details.
5. "Not powered" (NP) state is defined as VDD2 < $VDD2_{UV9}$. "Powered" (P) state is defined as VDD2 > $VDD2_{UV9}$. See Power Supply Characteristics for details.
6. The $VDD2_Q$ "not powered" (NP) state forces a $Fault_Q$ "detected" (D) state. $Fault_Q$ state automatically changes to "not detected" (ND) when all fault conditions are removed. Faults are defined in Diagnostics and Monitoring.
7. The default behavior shown here can be modified through the SPI. See Serial Peripheral Interface for details.
8. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See Recommended Application Circuits for more information.
9. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See Switch Types and Switch Protection for more information.
10. If an Over-Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over-Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally. See Switch Protection for more information.

Table 3.5. Si834xxxFx Truth Table

Mode	Inputs[1]		State[2]			Outputs	
	An	OE	$VDD1_Q$[3]	$VDD2_Q$[4]	$Fault_Q$[5]	FLT\[6]	Bn[7]
Fault	X	X	NP	–	–	U	OFF
	X	X	P	NP	D	ON	OFF
	X	X	P	P	D	ON	OFF[8]
Normal	L	X	P	P	ND	OFF	OFF
	X	L	P	P	ND	OFF	OFF
	H	H	P	P	ND	OFF	ON

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. "NP" is the "not powered" state, "P" is the "powered" state, "ND" is the "not detected" state, "D" is the detected state, and "–" is an irrelevant state. The current state (Q) and the previous state (Q-1) of the device, as well as the current inputs to the device, define the current outputs of the device.
3. "Not powered" (NP) state is defined as VDD1 < $VDD1_{UV}$. "Powered" (P) state is defined as VDD1 > $VDD1_{UV}$. Logic inputs can power VDD1 through an internal diode if its source has adequate current. See Power Supply Characteristics for details.
4. "Not powered" (NP) state is defined as VDD2 < $VDD2_{UV9}$."Powered" (P) state is defined as VDD2 > $VDD2_{UV9}$. See Power Supply Characteristics for details.
5. The $VDD2_Q$ "not powered" (NP) state forces a $Fault_Q$ "detected" (D) state. $Fault_Q$ state automatically changes to "not detected" (ND) when all fault conditions are removed. Faults are defined in Diagnostics and Monitoring.
6. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See Recommended Application Circuits for more information. It's default behavior shown here can be modified through the SPI. See Serial Peripheral Interface for details.
7. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See Switch Types and Switch Protection for more information.
8. If an Over-Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over-Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally. See Switch Protection for more information.

3.2 Switch Timing Behavior

The Si834x exhibits different timing behavior depending on the state of the power supplies, as well as the switch inputs. In the figure below, the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed. It is important to note that the analog behavior of the Si834x device changes based on the switch type selected. See Switch Types for details.

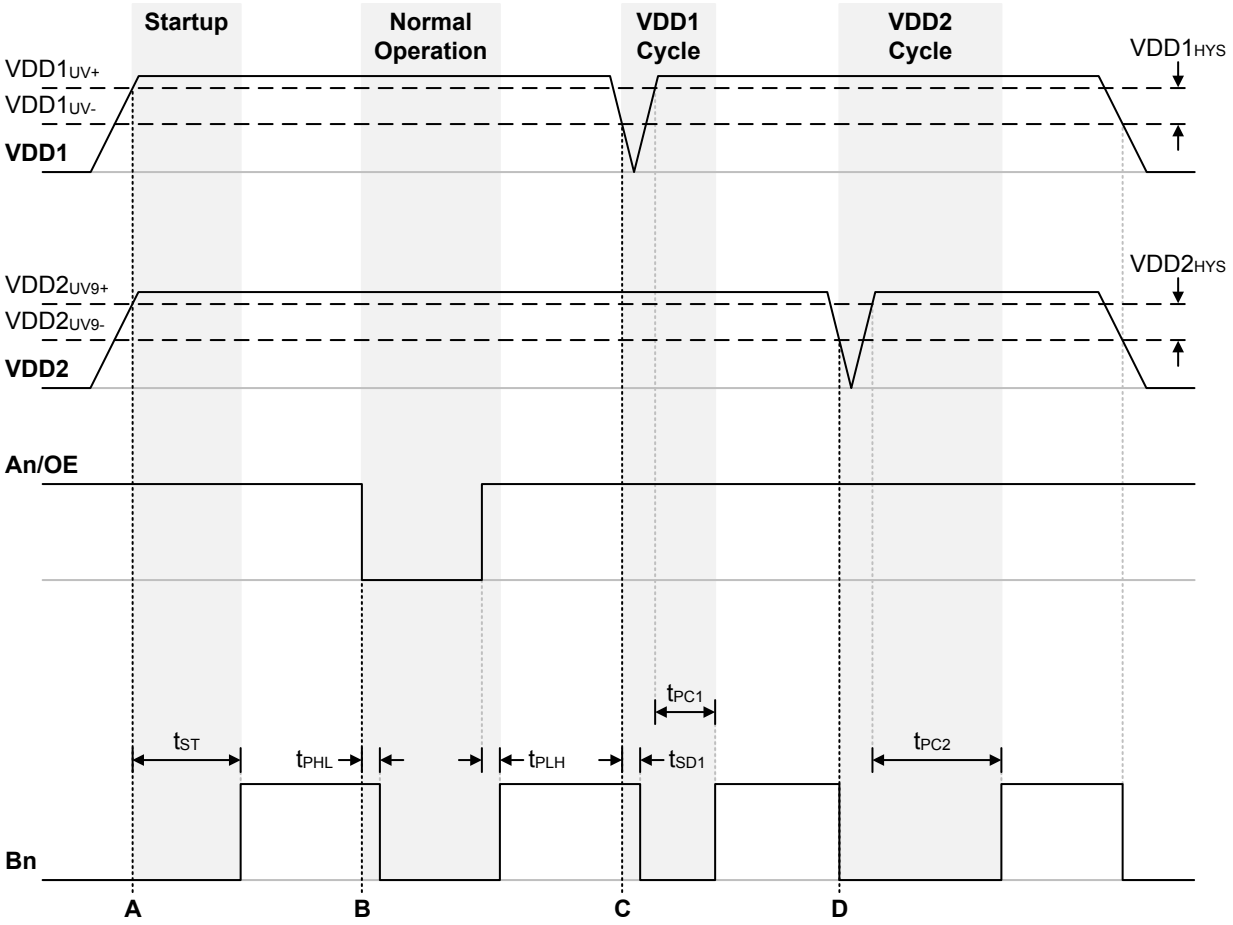


Figure 3.1. Switch Timing Behavior

At marker A in the figure above, both power supplies, though unpowered initially, exceed the undervoltage threshold ($VDD1_{UV}$ and $VDD2_{UV9}$). At this point, the device begins to start up. Until the Device Startup Time (t_{ST}) elapses, the output remains off. After t_{ST}, the output state begins to track the input state. Note that the analog timing behavior from device input to device output is depicted in Figure 5.1 on page 47.

At marker B, the input control signal is turned off. After the Turn OFF Propagation Delay (t_{PHL}) elapses, the output will turn off. When the input is turned back on, an additional Turn ON Propagation Delay (t_{PLH}) must elapse before the output returns to the ON state.

At marker C, the logic interface power supply is turned completely off to begin a power cycle. When VDD1 drops below $VDD1_{UV}$, the device begins to shutdown. After the Logic Interface Shutdown Time (t_{SD1}) elapses, the output is turned off. When VDD1 exceeds the $VDD1_{UV}$ threshold again, the Logic Interface Power Cycle Time (t_{PC1}) must elapse before the output will again track the input and turn back on.

At marker D, the switch power supply is turned completely off to begin a power cycle. When VDD2 drops below $VDD2_{UV9}$, the output immediately turns off. When VDD2 exceeds $VDD2_{UV9}$ again, the Switch Power Cycle Time (t_{PC2}) must elapse before the output will again track the input and turn back on.

3.3 Switch Types

The Si834x Isolated Smart Switch is available in two switch configurations to meet a broad range of application requirements.

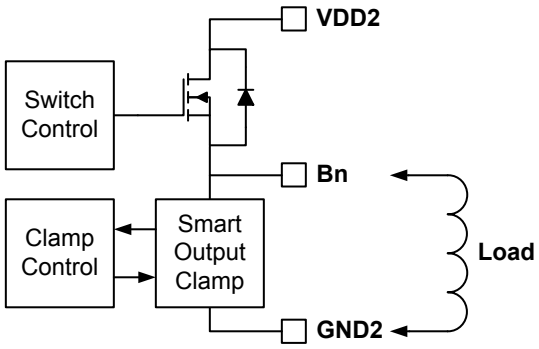


Figure 3.2. Sourcing Device

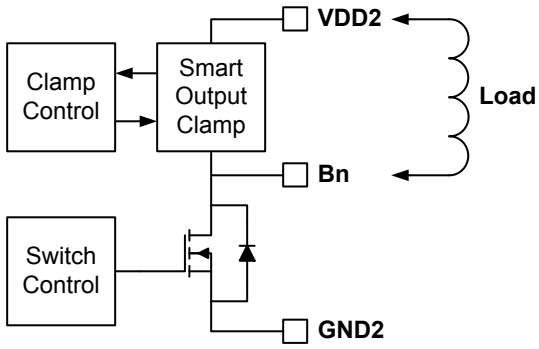


Figure 3.3. Sinking Device

As shown in the figures above, the sourcing configuration operates as an open-source output for high-side switching. It connects to VDD2 when the switch is turned ON. The sinking configuration uses an open-drain output for low-side switching. It connects to GND2 when the switch is turned ON. Both the sourcing and sinking output configurations are IEC61131-2 compliant. Each switch can source or sink 700 mA of continuous current.

Additionally, the Si834x devices offer an Inrush Current Mode which can briefly provide up to 8 A of current. This is ideal for driving loads with low startup impedance like lamps. To reliably achieve continuous currents of 700 mA, follow the circuit design and layout recommendations in this document. See Layout Considerations and Recommended Application Circuits for details on how to design for high continuous current devices.

All switches include a smart clamp output to quickly and safely demagnetize inductive loads, as well as advanced over-current protection, over-temperature protection, and open-circuit detection. When the switch is OFF, the output can be considered high impedance (Hi-Z). However, the demagnetization clamp will engage in the OFF state if the voltage on the output pin exceeds the Demagnetization Clamp High Voltage (V_{CLMPH}) specification. Also, there will be some OFF state current ($I_{O(OFF)}$) to facilitate open circuit detection. See Figure 5.10 on page 57 and Figure 5.11 on page 58 for details on the output behavior when the switch is OFF.

3.4 Switch Protection

The Si834x Isolated Smart Switch contains sophisticated protection technology. It is designed to operate for decades driving a broad range of loads. It can seamlessly recover from faults ranging from a simple switch supply overvoltage, to a dead short on a driven output channel. The following sections detail individual methods of protection, and how they behave in common scenarios.

3.4.1 Demagnetization Energy Protection

The Si834x Isolated Smart Switch includes a high efficiency, multi-voltage “smart” output clamp used to protect the switch from harsh demagnetization voltage, commonly referred to as back EMF, flyback voltage, inductive voltage “kick-back”, or sometimes just as a “voltage kick.” The smart clamp is actively controlled based on the current through the switch, the switch supply voltage, and the switch temperature. By dynamically adjusting the clamp voltage based on device and load conditions, the Si834x balances safety with performance. It limits device power dissipation to safe levels, while still delivering fast turn-off performance that allows inductors to switch quickly and reduces arcing and arc welding failures in relays.

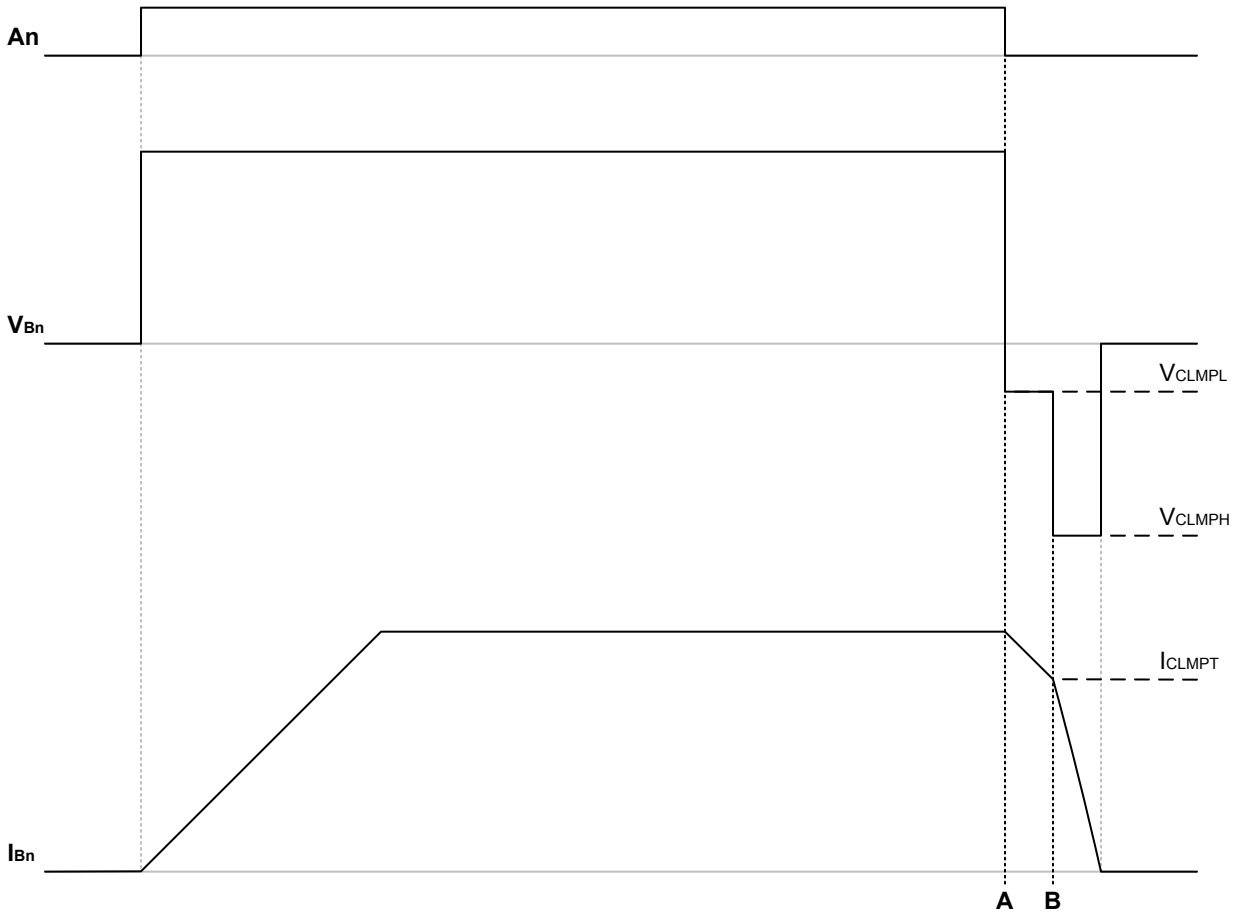


Figure 3.4. Demagnetization Protection Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si834x switch when driving an inductor at the switches’ typical ON State Load Current ($I_{O(ON)}$) and under normal operating conditions. It plots the digital input to the switch (An) as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number.

At marker A, the switch, driving a fully charged inductor, is turned off. The inductor resists a change in current by generating a very large negative voltage at the switch output (Bn) and across the smart output clamp. Initially, because the current through the smart clamp exceeds the Demagnetization Clamp Current Threshold (I_{CLMPT}), the clamp voltage is constrained to the Demagnetization Clamp Low Voltage (V_{CLMPL}). At this clamp voltage, demagnetization occurs slowly, but power dissipation in the channel is limited to a safe level.

At marker B, current through the clamp falls below I_{CLMPT} and the clamp voltage is changed to Demagnetization Clamp High Voltage (V_{CLMPH}). The higher clamp voltage will rapidly demagnetize the inductor. The increased power dissipation during this phase of protection will cause a small temperature rise in the channel, but with inductor current sufficiently constrained below I_{CLMPT}, this rise is easily tolerated by the Si834x device.

This two-step approach when turning off an inductor gives the Si834x the ability to demagnetize an unlimited amount of energy from a single turn-off pulse, on a single channel ($E_{AS(1CH)}$). See Table 5.12 on page 53 for maximum energy dissipation under other conditions.

3.4.2 Over-Current Protection with Inrush Current Mode

The Si834x Isolated Smart Switch includes short-circuit-proof, over-current protection with automated restart. Unlike other over-current-protected switches, the Si834x rapidly samples current through the switch, disabling the output while an over-current condition remains present, rather than depending on an increased switch resistance and thermal protection alone to limit current through the switch. This approach drastically reduces the power dissipation through the switch during an over-current condition, eliminating the need for thermal independence of separate channels, increasing the lifespan of the switch, simplifying the thermal requirements of the end-system, and still ensuring safe operation of the switch even with a dead short present for an indefinite amount of time.

The Si834x devices also include an Inrush Current Mode, which enables them to drive loads with low startup impedance like lamps by providing a brief high current when the channel is initially turned on.

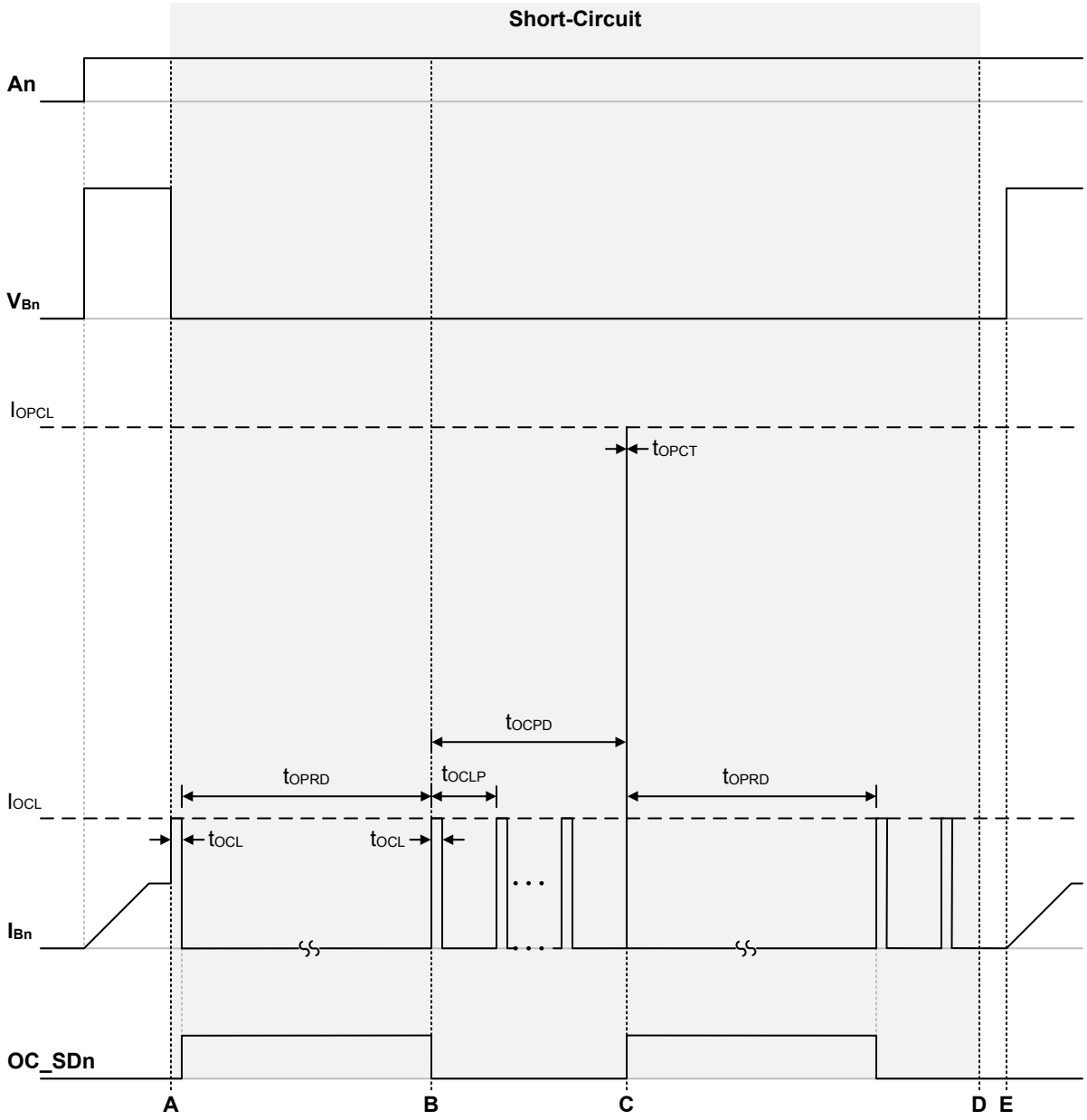


Figure 3.5. Over-Current Shutdown Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si834x switch when driving an inductor at the switches' typical ON State Load Current ($I_{O(ON)}$) under normal operating conditions initially, but then experiencing a short-circuit. Note that marker B depicts the Si834x switches' behavior when it is turned on in a short-circuit state. The figure plots the digital input to the switch (An) as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the Over-Current Shutdown diagnostic register value for the channel (OC_SDn) when the enable mask for auto-clearing of diagnostics (ACLR_EN) is set to true. This is the default diagnostic report clearing behavior.

Initially, the switch channel is turned on and the load inductor is fully charged. The current must exceed the Output Current Limit Threshold (I_{OCLT}), which is similar to the Output Current Limit (I_{OCL}) in the figure above, for the switch to detect an over-current condition and engage its over-current protection. At marker A, a dead short (0 Ω resistance) is placed on the output to the switch channel which causes an immediate voltage drop and current rise well above I_{OCLT}. The Si834x device will immediately engage its over-current protection and limits the current to the Output Current Limit (I_{OCL}) by altering the resistance of the switch. If the over-current condition is not removed within the Output Current Limit Pulse time (t_{OCL}), the output is immediately shutdown and OC_SDn is set to true. The channel will remain shutdown for the duration of the Over-Current Protection Retry Delay (t_{OPRD}).

At marker B, after the Over-Current Protection Retry Delay has expired, OC_SDn is set to false, and the channel is turned on again. If the over-current condition is once again detected on the output, the resistance of the switch will once again be altered to limit the current to I_{OCL} for no longer then t_{OCL}, at which point the channel will shut down again, protecting itself from high power dissipation. The switch will attempt to turn on again in the same way, multiple times, at a retry period equal to Output Current Limit Period (t_{OCLP}), and for up to the Over-Current Protection Duration (t_{OCPD}). If the over-current condition is no longer detected at any time during an Over Current Limit Pulse, the switch resistance is immediately reduced to normal ON-State Output Resistance (R_{ON}).

At marker C, the Si834x tests the load to determine if it requires high inrush current for normal operation. The current limit is increased to Output Peak Current Limit (I_{OPCL}), and the pulse time is reduced to Output Peak Current Test Pulse (t_{OPCT}). See the figure below for details on switch behavior when driving a load that requires a high inrush current. In the case of a short-circuit or other over-current condition that cannot be resolved with high inrush current, after t_{OPCT} passes, the output is shutdown again for t_{OPRD}, and OC_SDn is set to true. This cycle will repeat indefinitely as long as the over-current condition remains detected.

At marker D, the dead short is removed. However, during the time the channel is shutdown, no changes in the over-current condition are detected. This is true for any period of time the channel is shutdown. Therefore, the channel remains shutdown until t_{OCLP} expires, at which time the channel is turned on, and normal operation resumes.

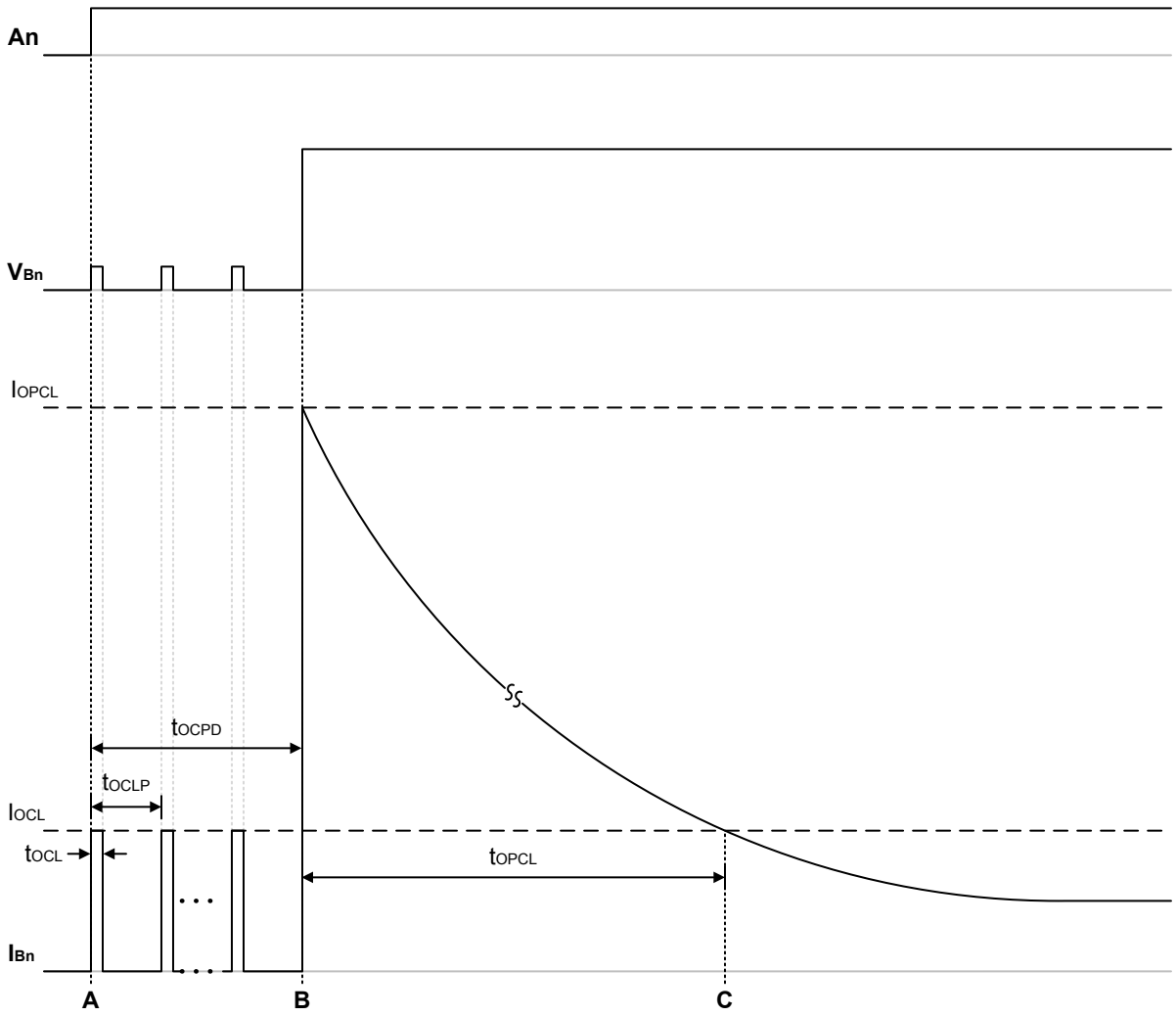


Figure 3.6. Inrush Current Mode Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si834x switch when driving a load that requires a high inrush current such as an incandescent lamp. The figure plots the digital input to the switch (An) as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number.

At marker A, the channel is turned on and the current through the switch is immediately detected above the Output Current Limit Threshold (I_{OCLT}), which engages the over-current protection and limits the current to the Output Current Limit (I_{OCL}). See Figure 3.5 on page 15 for details on typical over-current protection.

At marker B, similar to the over-current condition depicted in Figure 3.5 on page 15, the Si834x switch alters its resistance to allow for a higher Output Peak Current Limit (I_{OPCL}). Unlike the over-current condition, if the current through the switch remains less than I_{OPCL}, the switch will maintain the increased current limit for a time up to the Output Peak Current Limit Pulse (t_{OPCL}). The current through the switch must reduce to a level below I_{OCLT}, which is similar to I_{OCL} depicted in the figure above, before t_{OPCL} passes. Otherwise, the channel is deemed to be in an over-current state, at which time it is shutdown and Over-Current Shutdown diagnostic register (OC_SDn) is set to true.

3.4.3 Over-Temperature Protection

The Si834x Isolated Smart Switch includes independent over-temperature protection for each channel. It has two levels of protection that balance device safety with switch performance. The Si834x will continue to operate safely with reduced performance when individual channels are over-temperature, only shutting down channels when all channels are detected to be over-temperature.

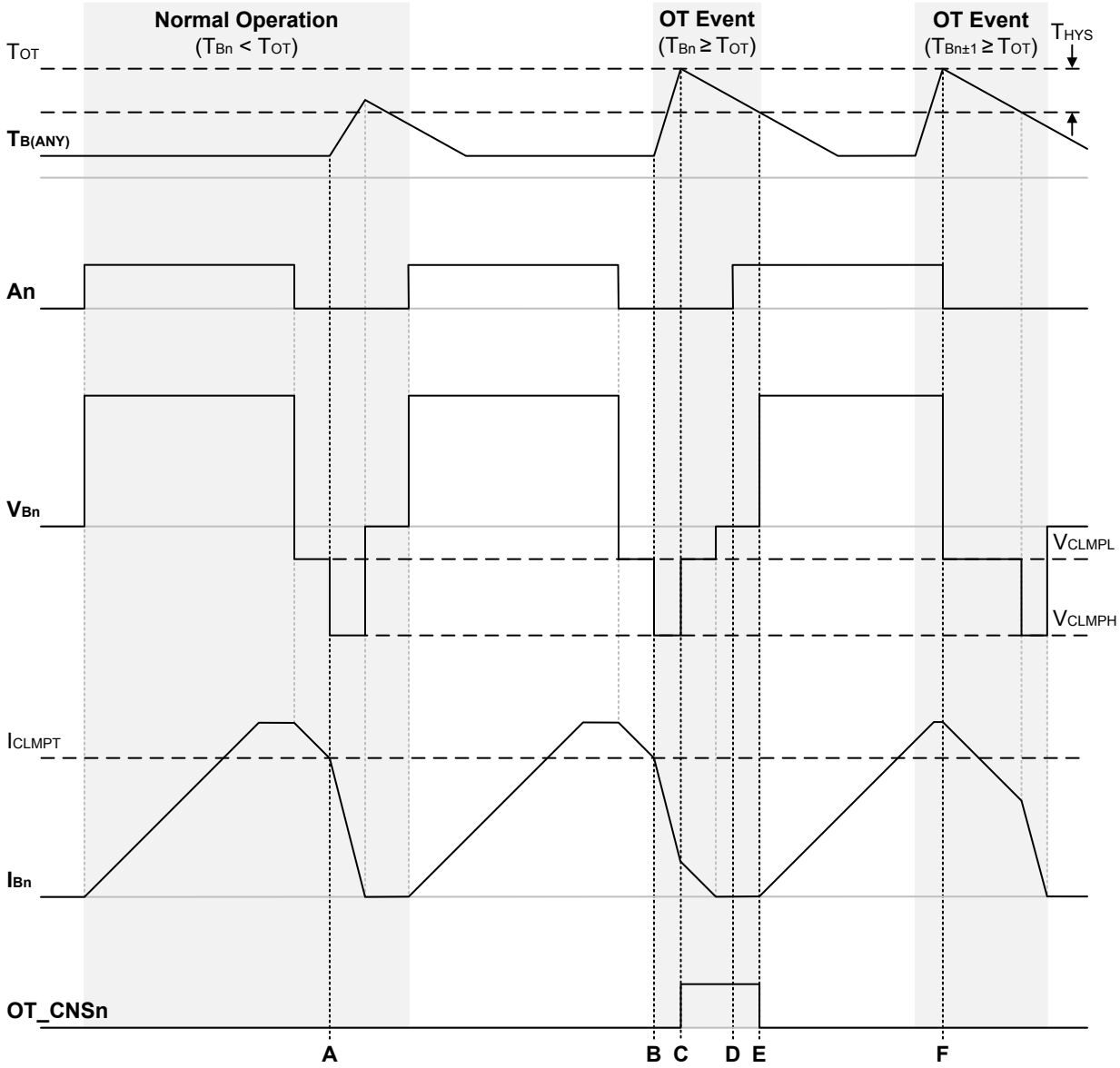


Figure 3.7. Over-Temperature Constraint Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si834x switch when driving an inductor at the switches' typical ON State Load Current ($I_{O(ON)}$), but then experiencing two different over-temperature events (OT Event). The "Normal Operation" section is identical to Figure 3.4 on page 14 and is included for reference. The figure plots the digital input to the switch (An), the temperature of any output channel ($T_{B(ANY)}$), as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the Over-Temperature Constraint diagnostic register value for the channel (OT_CNSn) when the enable mask for auto-clearing of diagnostics (ACLR_EN) is set to true. This is the default diagnostic report clearing behavior.

Under normal conditions where ambient temperature is limited to the Derated Ambient (T_{AD}), calculated in Power Dissipation Considerations, the most likely cause of over-temperature is demagnetizing a large inductor (E_{AS}). Specifically, when the smart clamp is set to the Demagnetization Clamp High Voltage (V_{CLMPH}) and power dissipation is at its peak. This temperature rise is illustrated in the figure above at marker A for an E_{AS}, which falls below the maximum specification of the device. See Table 5.12 on page 53 for more details on the absolute maximum specifications.

Marker B illustrates the switch behavior when the dissipated E_{AS} is too large for the current ambient temperature. When the Si834x smart clamp transitions to V_{CLMPH}, the switch temperature rises quickly until it reaches the Over-Temperature Threshold (T_{OT}) at marker C. At this point, the smart clamp for each Si834x channel is constrained to the Demagnetization Clamp Low Voltage (V_{CLMPL}), and OT_CNSn is set to true. This protects the device by reducing power dissipation and forcing all inductors attached to the Si834x to demagnetize more slowly.

While the Si834x is over-temperature on any channel, all channels are prevented from turning on in order to further reduce power dissipation and recover quickly, as illustrated at marker D. Note that a channel in inrush current mode, or experiencing an Over-Current Shutdown will also have it's retry attempts suppressed during its Over-Current Protection Duration (t_{OCPD}) period. Once the temperature of the channel falls below the Over-Temperature Hysteresis (T_{HYS}) level, as illustrated by marker E, OT_CNSn is set to false, and all channels resume normal operation.

It is important to note that an over-temperature condition on any channel will cause all channels to be constrained in the manner described above, not just the channel with the over-temperature diagnostic report. This is illustrated at marker F where a different channel, not illustrated, exceeds T_{OT}, forcing the illustrated channel to remain at V_{CLMPL} and constraining its demagnetization performance.

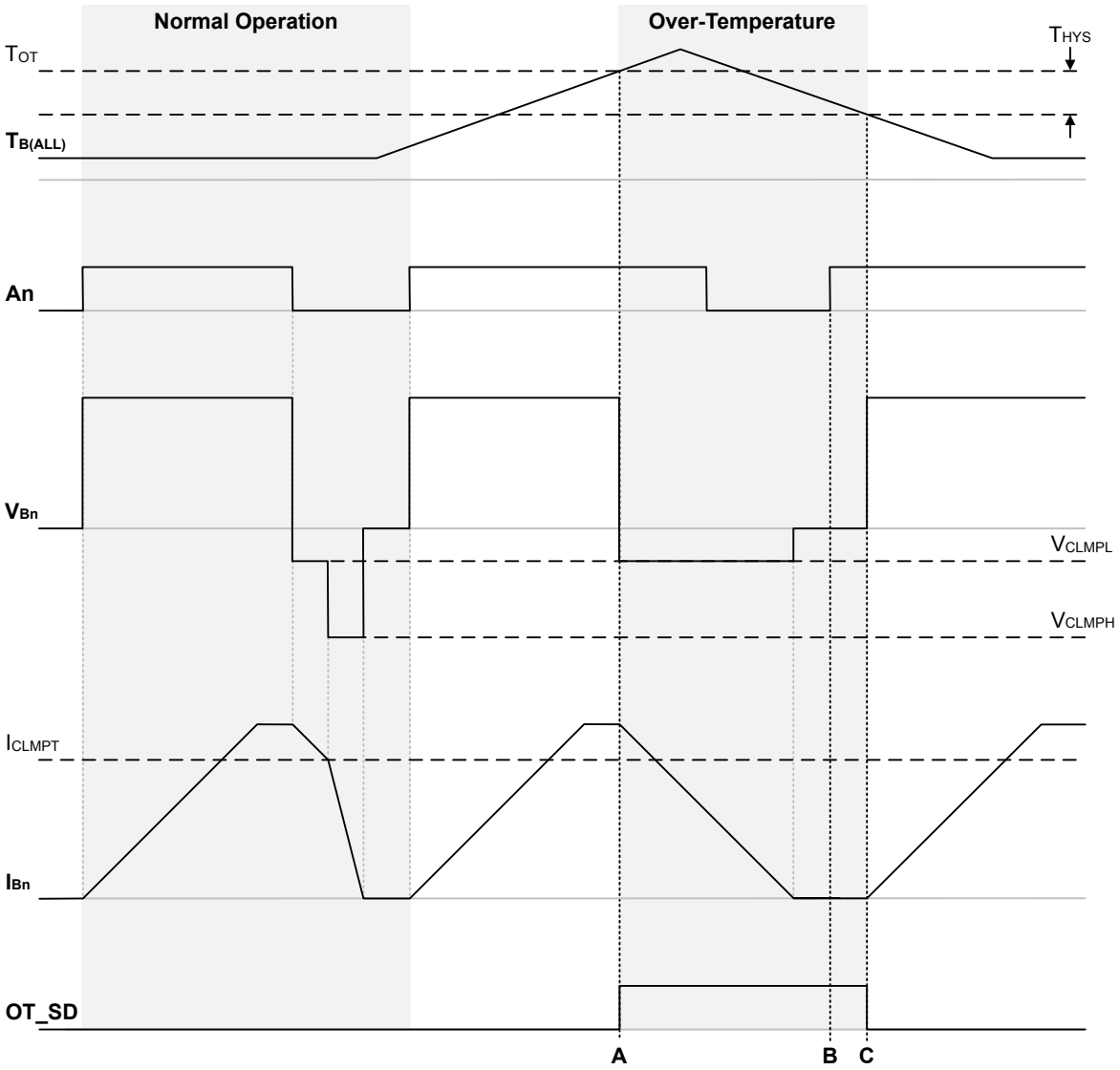


Figure 3.8. Over-Temperature Shutdown Behavior

If ambient temperature is not limited to T_{AD}, or if E_{AS} is much larger than the specified maximum, it is possible that the temperature of all channels ($T_{B(ALL)}$) will exceed T_{OT}, as illustrated in the figure above. In this event, as illustrated at marker A, all channels are immediately shutdown, and the Over-Temperature Shutdown register (OT_SD) will be set to true. If a channel is driving an inductor, the smart clamp will be constrained to V_{CLMPL} and demagnetization time will be increased to help reduce power dissipation. All channels will be prevented from turning on (marker B) until the temperature of all channels falls below T_{HYS}, as depicted at marker C, at which time the OT_SD register will be set to false and all channels will resume normal operation.

3.4.4 Power Supply Protection

The Si834x Isolated Smart Switch monitors both the logic interface and switch power supplies, protecting the device and load when the power supplies are out of specification. Like the over-temperature protection, the Si834x balances performance with safety by constraining switch performance under some power supply conditions, and safely shutting down under others.

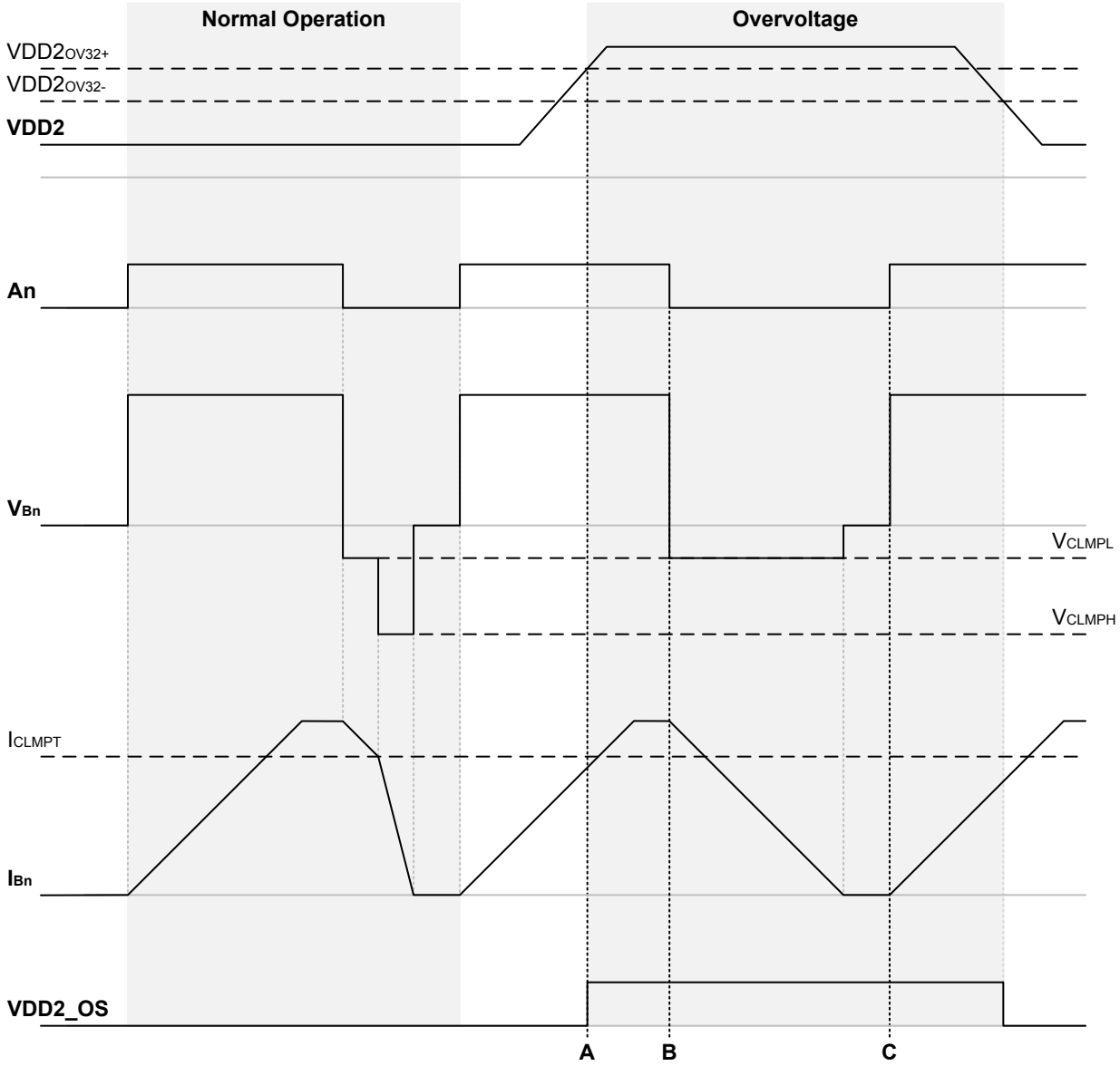


Figure 3.9. VDD2 Overvoltage Constraint Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si834x switch when driving an inductor at the switches' typical ON State Load Current ($I_{O(ON)}$), but then experiences an overvoltage condition on the switch power supply (VDD2). The "Normal Operation" section is identical to Figure 3.4 on page 14 and is included for reference. The figure plots the digital input to the switch (An), the VDD2 supply voltage (VDD2), as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the VDD2 Out of Specification register value (VDD2_OS) when the enable mask for auto-clearing of diagnostics (ACLR_EN) is set to true. This is the default diagnostic report clearing behavior.

At marker A, VDD2 exceeds the VDD2 Overvoltage Threshold ($VDD2_{OV32}$). In order to reduce power dissipation to a safe level, the smart clamp for each channel is constrained to Demagnetization Clamp Low Voltage (V_{CLMPL}), and the VDD2_OS register is set to true. While the smart clamp for each channel is limited to V_{CLMPL}, demagnetization performance is constrained and all inductive loads turn off more slowly, as illustrated at marker B. Unlike an Over-Temperature Constraint, the output channels are not prevented from turning on (marker C). Once VDD2 falls below $VDD2_{OV32}$ again, the smart clamp returns to "Normal Operation", and the VDD2_OS register is set back to false.

It is important to note that overvoltage is not prevented from damaging the device if VDD2 remains above $VDD2_{OV32}$ or exceeds the absolute maximum specification. It only protects the device from higher power dissipation when demagnetizing an inductive load at higher voltages, and generates a diagnostic report. If VDD2 exceeds the VDD2 ESD Clamp Threshold ($VDD2_{CLMP}$), the VDD2 ESD clamp will engage, damaging the device.

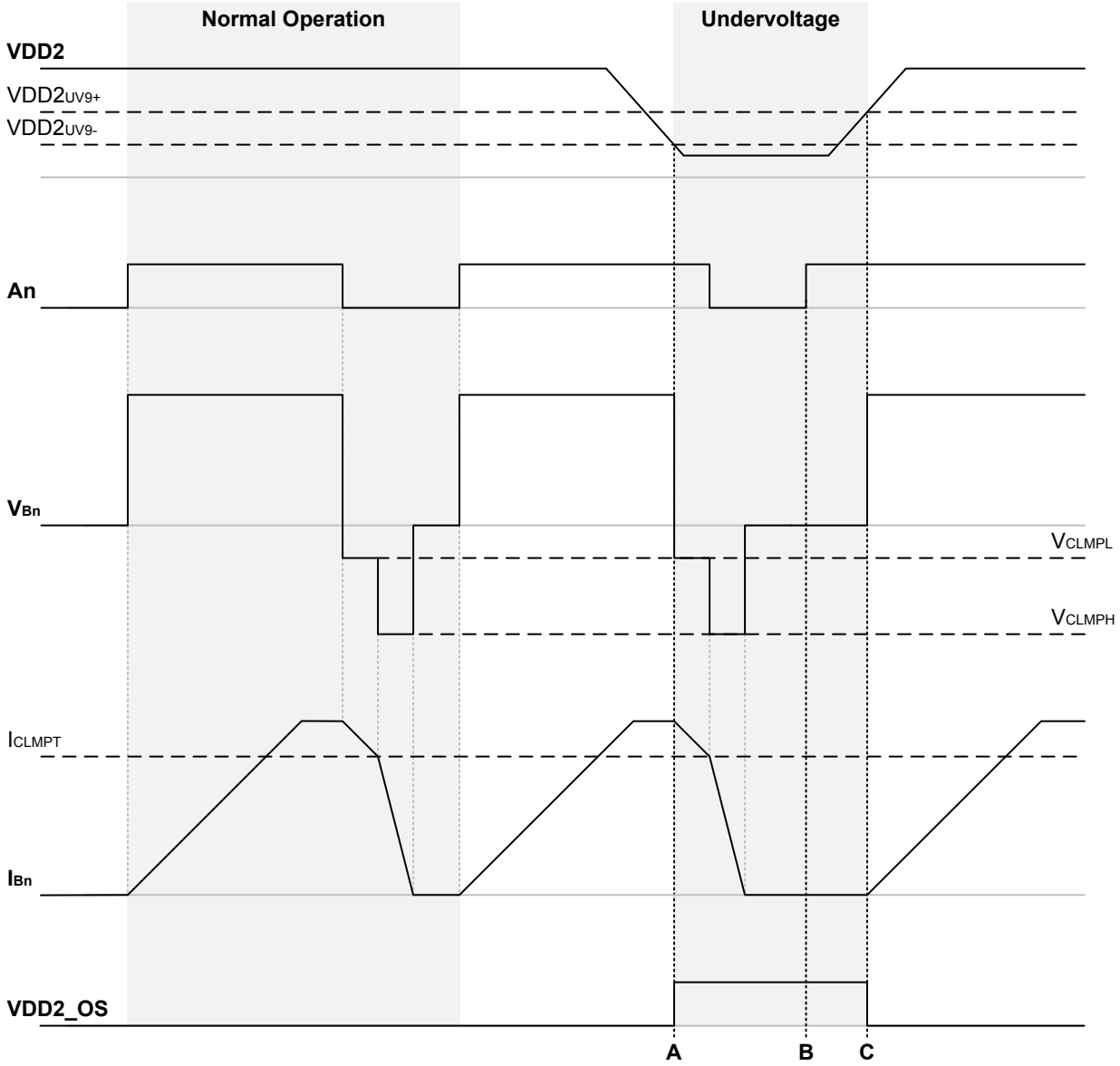


Figure 3.10. VDD2 Undervoltage Shutdown Behavior

The switch is protected against a VDD2 undervoltage condition in a very similar manner to VDD2 overvoltage conditions, as illustrated by the figure above. At marker A, VDD2 falls below the VDD2 Undervoltage Threshold ($VDD2_{UV9}$). All channels are immediately shutdown, and the VDD2_OS register is set to true. Note that the smart clamp operates normally during shutdown. While VDD2 is undervoltage, all channels are prevented from turning on (marker B). Only after VDD2 rises above $VDD2_{UV9}$ again will all channels be allowed to return to normal operation, and the VDD2_OS register set back to false, as illustrated at marker C.

It is important to note that VDD2 must remain powered to offer undervoltage protection in the manner described above. If VDD2 is completely unpowered (0 V), the smart clamp voltage is not well defined. Also, the Master Diagnostic register (MASTER_DIAG) may not accurately report the VDD2 state. In this condition, if the switch is undamaged, the Communication Error register value (COMM_ERR) will be set to true, denoting a loss of communication with the unpowered switch. Finally, when power is restored to VDD2, the device must wait for VDD2 Switch Power Cycle Time (t_{PC2}) to pass before normal operation will resume. See Switch Timing Behavior for details.

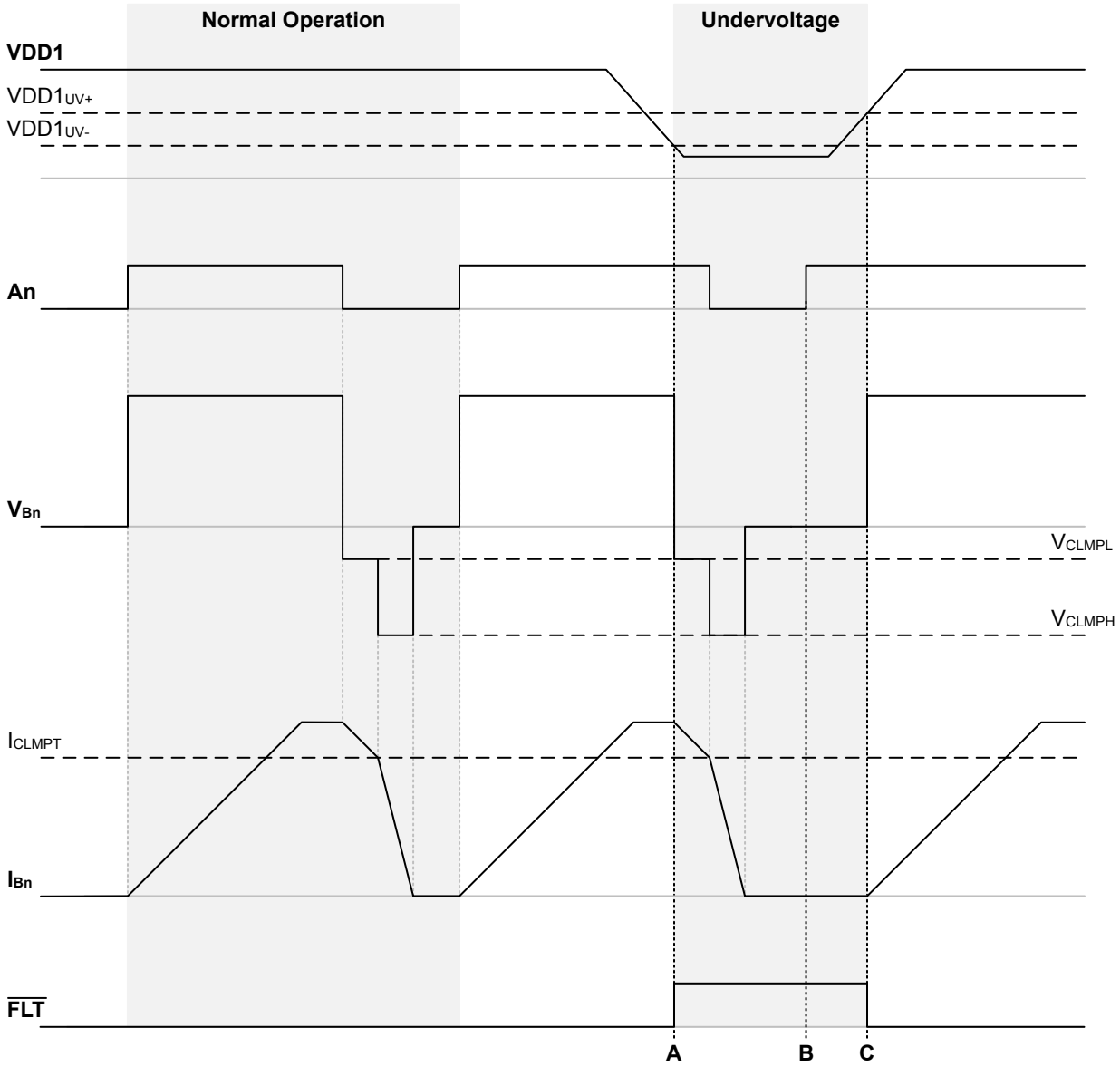


Figure 3.11. VDD1 Undervoltage Shutdown Behavior

The logic interface is also protected against a VDD1 undervoltage condition in the same way as VDD2, illustrated by the figure above. Unlike the VDD2 undervoltage condition, the VDD1 undervoltage condition is only reported on the FLT\ pin, not through a diagnostic register. Like the VDD2 undervoltage protection, all channels are immediately shutdown when VDD1 falls below VDD1 Undervoltage Threshold ($VDD1_{UV}$), as illustrated at marker A. All channels are prevented from turning on while VDD1 remains undervoltage (marker B), and normal operation immediately resumes when VDD1 rises above $VDD1_{UV}$, as illustrated by marker C.

Like VDD2 undervoltage protection, VDD1 must remain powered to offer undervoltage protection in the manner described above. If VDD1 is completely unpowered (0 V), the FLT\ pin may be in an undetermined state and may show a logic high value if connected to VDD1 through a pull-up resistor. When power is restored to VDD1, the device must wait for VDD1 Logic Interface Cycle Time (t_{PC1}) to pass before normal operation will resume. See Switch Timing Behavior for details.

3.5 Diagnostics and Monitoring

The Si834x Isolated Smart Switch communicates rich diagnostic and monitoring information to the host controller including the condition of the load, power supplies, and built-in protection. Eight separate diagnostic reports are available, as well as channel status reports.

Table 3.6. Diagnostics Overview

Scope	Diagnostic	Severity[1]	Description
Per Channel	Open-Circuit	Warning	Channel has no load detected. Output is operating normally.
	Over-Current	Shutdown	Channel is overloaded. Output is immediately turned off.
	Over-Temperature	Constraint	Channel is too hot. Inductors demagnetize slowly. Output will not turn back on.
All Channels		Shutdown	All channels are too hot. All outputs are immediately turned off.
	VDD2 Low-Voltage	Warning	VDD2 is under $VDD2_{UV18}$. All outputs operating normally.
	VDD2 Overvoltage	Constraint	VDD2 is over $VDD2_{OV32}$. Inductors demagnetize slowly.
	VDD2 Undervoltage	Shutdown	VDD2 is over $VDD2_{UV9}$. All outputs are turned off.
	VDD1 Undervoltage	Shutdown	VDD1 is under $VDD1_{UV}$. All outputs are turned off.
	Communication Error	Shutdown	Communication across the isolation barrier is lost. All outputs are turned off.

Note:

1. Diagnostics with a severity of "Constraint" or "Shutdown" are defined as faults and exposed on the FLT\ output. The configuration for FLT\ can be modified using the SPI, if available. See Serial Peripheral Interface for details.

Diagnostics and monitoring information is reported in different ways depending on the device selected (see the Ordering Guide for device options.) Devices with the SPI allow access to all diagnostic and monitoring information via diagnostic registers. One active-low, open-drain indicator pin (FLT\) is available on SPI devices and provides immediate diagnostic report feedback to the user, or can be used as a fast diagnostic interrupt for the controller. The diagnostic reports exposed on this indicator pin are configurable via the SPI. By setting a true value in the Fault Enable Mask (FLT_EN) register at the desired diagnostic's bit field, the indicator pin will be turned ON when the corresponding diagnostic report is true. See Serial Peripheral Interface for more details.

Devices without the SPI have a fixed configuration and expose diagnostics and monitoring information on active-low, open-drain indicator pins only. These pins can drive an LED to provide end-user feedback, they can be combined with a pull-up resistor and read by the controller, or multiple pins can be combined to simplify diagnostics and monitoring across devices. Like SPI devices, an FLT\ indicator pin is always provided. It is configured to report any diagnostic which represents an abnormal switch behavior. This is also the default configuration for SPI devices. Contact Skyworks for custom device configurations not available in the Ordering Guide.

A diagnostic report can be cleared from the Si834x device once the condition that caused the report is removed from the device. If a report is cleared while the condition remains, a new report will be automatically generated. See Switch Protection for details on the conditions that cause diagnostic reports.

For SPI devices, all diagnostics are set to have their reports automatically cleared when the conditions that caused the report are removed. However, this can be controlled for each diagnostic, except for the VDD1 Undervoltage Shutdown diagnostic, through the Automatic Diagnostic Clear Enable Mask (ACLR_EN) register. If a bit field in this enable mask is set to false, the corresponding diagnostic report will remain until it is cleared by setting a true value in the Clear Diagnostic (CLR_DIAG) register at the corresponding diagnostic's bit field.

It is important to note that the operation of an output channel is not affected by the presence of a diagnostic report. For example, if the device is not configured to automatically clear a diagnostic report, then the diagnostic report will persist after the condition that caused the report is removed. Once the condition that caused the report is removed, the channel will resume normal operation regardless of diagnostic report state. The Communication Error diagnostic is an exception to this behavior. See Communication Error Diagnostic for details.

For parallel interface only devices, a device with a Clear Fault Input pin (Si834xxxCx) is required to manually clear diagnostic reports on the FLT\ pin. It operates the same way as setting a true value in the CLR_DIAG register for all diagnostics. All other parallel interface only devices are configured to automatically clear diagnostic reports when the conditions that caused the report are removed.

3.5.1 Power Supply Diagnostics

The Si834x Isolated Smart Switch offers complete power supply diagnostics for both power supplies, including overvoltage, low-voltage, and undervoltage conditions.

Table 3.7. Switch Power Supply Diagnostics

Diagnostic	Supply Voltage[1]	FLT\[2]	VDD2_WRN\[3]	MASTER_DIAG[5:4]		Output Behavior[4]	
				VDD2_OS	VDD2_LOW	Switch	Clamps
VDD2 Voltage OK	$VDD2_{UV18}$ < VDD2 < $VDD2_{OV32}$	–	OFF	0	0	Normal	Normal
VDD2 Low-Voltage Warning	$VDD2_{UV9}$ < VDD2 < $VDD2_{UV18}$	–	ON	0	1	Normal	Normal
VDD2 Overvoltage Constraint	VDD2 > $VDD2_{OV32}$	ON	OFF	1	0	Normal	V_{CLMP} = V_{CLMPL}
VDD2 Undervoltage Shutdown	VDD2 < $VDD2_{UV9}$	ON	ON[5]	1[5]	1[5]	Turns OFF	Normal

Note:

1. Supply voltage must remain within this voltage range long enough to be measured for a change to be reported. If supply voltage changes sufficiently quickly, the diagnostic state will remain unchanged.
2. The output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. The default configuration for FLT\ is depicted, but can be modified using the SPI, if available. See Serial Peripheral Interface for details.
3. The output is both active-low and open drain. It is only available on specific product offerings. See the Ordering Guide for more details.
4. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here. See Switch Protection for more information. Clamp behavior applies to all smart output clamps, for all channels.
5. If the supply is unpowered, this value may not be accurately reported. Assuming there is no damage to the device, a COMM_ERR (MASTER_DIAG bit 7 = 1) will also be reported when VDD2 is unpowered and can be queried via the SPI. See Switch Protection for more information.

The table above describes the switch power supply diagnostic reports, where they are reported by default, and provides a brief overview of how the output behavior changes with each report. Note that the two bit fields in the Master Diagnostic register (MASTER_DIAG[5:4]) can be read separately or as a two-bit field. If read separately, bit 5 reports when VDD2 voltage is out of device specifications and the output behavior is abnormal. Bit 4 simply reports a warning when VDD2 voltage is low. If read as a two-bit field, all four possible power supply states can be discerned.

Table 3.8. Logic Interface Power Supply Diagnostics

Diagnostic	Supply Voltage[1]	FLT\[2]	Output Behavior[3]	
			Switch	Clamps
VDD1 Voltage OK	VDD1 > $VDD1_{UV}$	–	Normal	Normal
VDD1 Undervoltage Shutdown	VDD1 < $VDD1_{UV}$	ON	Turns OFF	Normal

Note:
1. Supply voltage must remain within this voltage range long enough to be measured for a change to be reported. If supply voltage changes sufficiently quickly, the diagnostic state will remain unchanged.
2. The output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might.
3. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here. See Switch Protection for more information. Clamp behavior applies to all smart output clamps, for all channels.

The table above describes the undervoltage shutdown diagnostic report for the logic interface power supply, where it is reported, and provides a brief overview of how the output behavior changes with the report. A VDD1 Undervoltage Shutdown is only reported on the FLT\ pin and has no corresponding SPI register entry. If VDD1 is completely unpowered (0 V), the FLT\ output is in an unknown state. A short glitch may be observed on the FLT\ pin when it is connected to VDD1 via a pull-up resistor, until the logic interface is powered. See Switch Protection for more details.

3.5.2 Over-Temperature Diagnostics

The Si834x Isolated Smart Switch reports over-temperature in different levels of severity allowing the controller to take different actions depending on how the switch output behavior is changing.

Table 3.9. Over-Temperature Diagnostics

Diagnostic	Switch Temperature[1]	Channels	FLT\[2]	OT_SD	OT_CNSn[3]	Output Behavior[4]	
						Switch	Clamps
Temperature OK	$T_{Bn} < T_{OT}$	Any Channel	–	0	0	Normal	Normal
Over-Temperature Constraint	$T_{Bn} > T_{OT}$	Any Channel	ON	0	1	Stays OFF	$V_{CLMP} = V_{CLMPL}$
Over-Temperature Shutdown		All Channels	ON	1	1	Turns OFF	$V_{CLMP} = V_{CLMPL}$

Note:
1. Channel must remain above this temperature long enough to be measured for a change to be reported. If the temperature changes sufficiently quickly, the diagnostic state will remain unchanged.
2. The output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. The default configuration for FLT\ is depicted, but can be modified using the SPI, if available. See Serial Peripheral Interface for details.
3. Reported in Diagnostic registers (DIAG), depending on the channel. See Serial Peripheral Interface for details.
4. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here. See Switch Protection for more information. Clamp behavior applies to all smart output clamps, for all channels.

The table above describes the over-temperature diagnostic reports, where they are reported by default, and provides a brief overview of how the output behavior changes with each report. An Over-Temperature Constraint is reported in the Diagnostic (DIAG) registers on a per-channel basis where *n,* in OT_CNS*n,* describes the specific channel that has exceeded the Over-Temperature Threshold (T_{OT}). An Over-Temperature Shutdown is reported in the MASTER_DIAG SPI register in bit field OT_SD when all channels have exceeded T_{OT}.

3.5.3 Over-Current Diagnostics

The Si834x Isolated Smart Switch reports over-current diagnostics on a per-channel basis so the controller can take action on a specific channel without disrupting operation on other channels.

Table 3.10. Over-Current Diagnostics

Diagnostic	An or SW_EN[n][1]	Output Current	FLT\[2]	OC_SDn[3]	Output Behavior[4]	
					Switch	Clamp
Current OK	L	–	–	0	Normal	Normal
	H	$I_{Bn} < I_{OCLT}$	–	0	Normal	Normal
Over-Current Shutdown	H	$I_{Bn} > I_{OCLT}$	ON	1	Turns OFF	Normal

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Bit addresses are zero-indexed such that channel 1 (output B1) is enabled by the SW_EN[0] bit.
2. The output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. The default configuration for FLT\ is depicted, but can be modified using the SPI, if available. See Serial Peripheral Interface for details.
3. Reported in Diagnostic registers (DIAG), depending on the channel. See Serial Peripheral Interface for details.
4. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here. See Switch Protection for more information.

The table above describes the over-current diagnostic report, where it is reported by default, and provides a brief overview of how the output behavior changes with the report. An Over-Current Shutdown can only be reported when the channel input is high (true). Over-Current Shutdown is reported in the Diagnostic (DIAG) registers on a per-channel basis where *n,* in OC_SD*n,* describes the specific channel that has exceeded the Output Current Limit Threshold (I_{OCLT}).

3.5.4 Open-Circuit Diagnostics

The Si834x Isolated Smart Switch can detect and report an open-circuit on each switch channel allowing the controller to easily detect the condition of individual loads.

Table 3.11. Open-Circuit Diagnostic

Diagnostic	An or SW_EN[n][1]	Load Resistance[2]	OPEN_CH\[3]	OPEN_WRNn[4]	Output Behavior[5]	
					Switch	Clamp
Open-Circuit Undetected	H	–	OFF	0	Normal	Normal
	L	$R_L < R_{LMAX}$	OFF	0	Normal	Normal
Open-Circuit Warning	L	$R_L > R_{LMAX}$	ON	1	Normal	Normal

Note:

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Bit addresses are zero-indexed such that channel 1 (output B1) is enabled by the SW_EN[0] bit.
2. "–" denotes that load resistance R_L is not measured. Open-Circuit is only detected during channel OFF.
3. The output is both active-low and open drain. It is only available on specific product offerings. See the Ordering Guide for more details.
4. Reported in Diagnostic registers (DIAG), depending on the channel. See Serial Peripheral Interface for details.
5. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here. See Switch Protection for more information.

The table above describes the open-circuit diagnostic report, where it is reported by default, and provides a brief overview of how the output behavior changes with the report. An Open-Circuit Warning can only be reported when the channel input is low (false). Open-Circuit Warning is reported in the Diagnostic (DIAG) registers on a per-channel basis where *n,* in OPEN_WRN*n,* describes the specific channel with a load resistance that exceeds the Load Resistance Threshold for Open-Circuit Diagnostic ($_{RLMAX}$).

3.5.5 Communication Error Diagnostics

The Si834x Isolated Smart Switch includes a bidirectional communication channel between the logic interface and the switch, across the isolation barrier. This communication channel is used for diagnostics, monitoring, and reporting. The channel input signals, which turn switches on and off are sent across the isolation barrier using their own dedicated unidirectional isolation channels to maximize reliability and performance.

The bidirectional diagnostic and configuration channel is continually monitored for faults or loss of communication from both the logic interface and the switch, like a bidirectional communication channel watchdog. If any error or loss of communication is detected by either the logic interface or the switch, a Communication Error (COMM_ERR) is reported in the Master Diagnostic (MASTER_DIAG) register, and the switches are safely shut down until the error is cleared. Unlike other diagnostic reports, when a Communication Error induces a diagnostic report, the outputs will be immediately disabled. All outputs will remain disabled until the Communication Error condition is removed and the diagnostic report is cleared.

If the switch is damaged or completely unpowered (VDD2 = 0 V), the logic interface will set COMM_ERR to true and disable all switch outputs. Likewise, if the logic interface is damaged or completely unpowered (VDD1 = 0 V), the switch will disable all switch outputs. In this way, the switch is ensured to never operate unless bidirectional communication is continually verified and both logic interface and switch appear in good condition.

3.5.6 Channel Status Monitoring

The Si834x Isolated Smart Switch simplifies end-user feedback by providing active-low, open-drain, output channel status indicator pins (LEDn) on select product options (see Ordering Guide for details.) The channel status indicator pins are on the logic interface side of the device and protected by the isolation barrier. Moreover, by implementing channel status indicators on the low-voltage logic interface, the power consumed by the indicator circuits is lower then an equivalent circuit on the high-voltage switch side of the device. This design choice also maximizes the current supplied to a load from the switches.

The LEDn pins show the same information as the Switch Status (SW_STAT) register, not the Switch Enable (SW_EN) register, which is equivalent to the parallel input (An) signals. This distinction is important. By indicating the switch status, the indicators will reflect the true output state, not just the output state commanded by the host controller.

For example, using a device with the SPI and channel status indicators (like the Si83408ADA-IF), if the controller attempts to turn on the B1 switch by setting the SW_EN1 bitfield to true but the output is in an over-current condition, B1 will instead shut-down (see Switch Protection for details.) In this scenario, the SW_STAT1 bit will be set to false and LED1 will turn OFF. If the over-current condition is removed and the B1 switch recovers and turns ON, the LED1 will immediately turn ON as well.

3.6 Serial Peripheral Interface

The Si834x includes a Serial Peripheral Interface (SPI) on select product options. It provides diagnostics, monitoring, and configuration capabilities for both the switch and logic interface. The direct-mapped registers allow an external master SPI controller to monitor the status of the switches, collect and clear diagnostic reports, configure how the switches operate, and how reports are indicated. Additionally, support is provided to easily daisy-chain up to thirty-two Si834x devices. Each of these daisy-chained devices may be uniquely addressed by one master SPI controller.

3.6.1 SPI Register Map

The addressable SPI registers are listed below and include descriptions for each field or bit.

Table 3.12. Si834x SPI Register Map

Register Name	SPI Address	Read/ Write	Reset Value	Description		
MASTER_DIAG	0x0	R	8'h0	Master diagnostic register		
				7	COMM_ERR	Communication Error (all channels shutdown)
				6	OT_SD	All Channels Over-Temperature (all channels shutdown)
				5	VDD2_OS	VDD2 Out of Specification
				4	VDD2_LOW	VDD2 Low-Voltage (warning)
				3	CHAN_DIAG4	Diagnostic reported on channel B4
				2	CHAN_DIAG3	Diagnostic reported on channel B3
				1	CHAN_DIAG2	Diagnostic reported on channel B2
				0	CHAN_DIAG1	Diagnostic reported on channel B1
DIAG_B21	0x1	R	8'h0	Diagnostic register for switch channels B2 and B1		
				7	OC_SD2	Channel B2: Over-Current Shutdown
				6	RSVD	Reserved
				5	OT_CNS2	Channel B2: Over-Temperature Constraint
				4	OPEN_WRN2	Channel B2: Open-Circuit Warning
				3	OC_SD1	Channel B1: Over-Current Shutdown
				2	RSVD	Reserved
				1	OT_CNS1	Channel B1: Over-Temperature Constraint
				0	OPEN_WRN1	Channel B1: Open-Circuit Warning
DIAG_B43	0x2	R	8'h0	Diagnostic register for switch channels B3 and B4		
				7	OC_SD4	Channel B4: Over-Current Shutdown
				6	RSVD	Reserved
				5	OT_CNS4	Channel B4: Over-Temperature Warning
				4	OPEN_WRN4	Channel B4: Open-Circuit Constraint
				3	OC_SD3	Channel B3: Over-Current Shutdown
				2	RSVD	Reserved
				1	OT_CNS3	Channel B3: Over-Temperature Constraint
				0	OPEN_WRN3	Channel B3: Open-Circuit Warning

Register Name	SPI Address	Read/ Write	Reset Value	Description		
SW_STAT	0x3	R	8'h0	Switch status and switch enable for channels B4 to B1		
				7	SW_STAT4	Switch B4: Output State (1 = On, 0 = Off)
				6	SW_STAT3	Switch B3: Output State (1 = On, 0 = Off)
				5	SW_STAT2	Switch B2: Output State (1 = On, 0 = Off)
				4	SW_STAT1	Switch B1: Output State (1 = On, 0 = Off)
SW_EN		R/W[1]		3	SW_EN4	1 = Turn on switch B4 0 = Turn off switch B4
				2	SW_EN3	1 = Turn on switch B3 0 = Turn off switch B3
				1	SW_EN2	1 = Turn on switch B2 0 = Turn off switch B2
				0	SW_EN1	1 = Turn on switch B1 0 = Turn off switch B1
RSVD	0x4	N/A	N/A	Reserved		
CLR_DIAG	0x5	W	N/A	A 1'b1 in a bit field clears the corresponding diagnostic registers		
				7	CLR_COMM_ERROR	Clear: Communication Error Shutdown
				6	CLR_OT_SD	Clear: All Channels Over-Temperature Shutdown
				5	CLR_VDD2_OS	Clear: VDD2 Out of Specification
				4	CLR_VDD2_LOW	Clear: VDD2 Low-Voltage Warning
				3	CLR_OC_SD	Clear all channels: Over-Current Shutdown
				2	RSVD	Reserved
				1	CLR_OT_CNS	Clear all channels: Over-Temperature Constraint
				0	CLR_OPEN_WRN	Clear all channels: Open-Circuit Warning
FLT_EN	0x6	R/W	8'hEA	Enable mask for diagnostic types reported on FLT\ pin		
				7	EN_COMM_ERROR	Enable: Communication Error Shutdown
				6	EN_OT_SD	Enable: All Channels Over-Temperature Shutdown
				5	EN_VDD2_OS	Enable: VDD2 Out of Specification
				4	EN_VDD2_LOW	Enable: VDD2 Low-Voltage Warning
				3	EN_OC_SD	Enable: Any Channel: Over-Current Shutdown
				2	RSVD	Reserved
				1	EN_OT_CNS	Enable: Any Channel: Over-Temperature Constraint
				0	EN_OPEN_WRN	Enable: Any Channel: Open-Circuit Warning

Register Name	SPI Address	Read/ Write	Reset Value	Description		
ACLR_EN	0x7	R/W	8'hFF	Enable mask for auto-clearing diagnostic reports (1 = auto-clear enabled, 0 = auto-clear disabled)		
				7	ACLR_COMM_ERROR	Auto-clear: Communication Error Shutdown
				6	ACLR_OT_SD	Auto-clear: Over-Temperature Shutdown
				5	ACLR_VDD2_OS	Auto-clear: VDD2 Undervoltage Shutdown
				4	ACLR_VDD2_LOW	Auto-clear: VDD2 Low-Voltage Warning
				3	ACLR_OC_SD	Auto-clear all channels: Over-Current Shutdown
				2	RSVD	Reserved
				1	ACLR_OT_CNS	Auto-clear all channels: Over-Temperature Constraint
				0	ACLR_OPEN_WRN	Auto-clear all channels: Open-Circuit Warning
RSVD	0x8	N/A	N/A	Reserved		
RSVD	0x9	N/A	N/A	Reserved		

Note:

1. Register is read only for all devices with a parallel input interface.

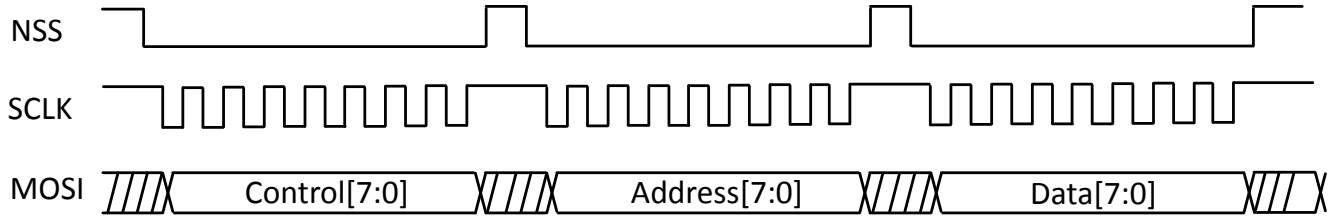
3.6.2 SPI Communication Transactions

SPI communication is performed using a four wire control interface. The four Si834x device pins utilized for SPI include:

- SCLK (input) the SPI clock
- NSS (input) active low device select
- MOSI (input) master-out-slave-in
- MISO (output) master-in-slave-out

Additionally, a fifth wire MOSI_THRU (output) is provided as an Si834x device pin to facilitate daisy chaining.

An Si834x SPI communication packet is composed of three serial bytes. In this sequence, byte0 is the control byte, and specifies the operation to be performed as well as the device to be selected in a daisy chain organization. The CID[4:0] field should be set to all zeros by the SPI master in non-daisy-chained operation. Next, byte1 specifies the address of the internal Si834x SPI register to be accessed. The final byte in the packet consists of either the data to be written to the addressed Si834x SPI register (using MOSI), or the data read from the addressed Si834x SPI register (using MISO). Details of the SPI communication packet are presented in the following figure for an Si834x SPI write transaction.



Control Byte							
7	6	5	4	3	2	1	0
BRCT	R/Wb	0	CID[0]	CID[1]	CID[2]	CID[3]	CID[4]
Address Byte							
7	6	5	4	3	2	1	0
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Data Byte							
7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

BRCT 1 - broadcast (write)
0 - only addressed part (write)
Ignored on reads

R/Wb 1 - read
0 - write

CTL[5] Reserved (set to 0)

CID[4:0] Daisy-chained part ID (0) is closest to the master MOSI. Accomplished by decrementing the CID as it passes through to the next Si834x device in the daisy chain on MOSI_THRU

Figure 3.12. SPI Communication Packet Structure, Write Operation and Control Byte Structure

The SPI master will provide the timing of the signals and framing of the communication packets for all Si834x SPI inputs: NSS, SCLK, and MOSI. Data is communicated from the SPI master to the Si834x using the MOSI signal. The NSS and SCLK signals provide the necessary control and timing reference allowing the Si834x to discern valid data on the MOSI signal. Data is returned to the SPI master by the Si834x utilizing the MISO signal only during the final byte of a three byte SPI read communication packet. At all other times, the MISO signal is tri-stated by the Si834x. Each of the eight bits for these three packets is captured by the Si834x on eight adjacent rising edges of SCLK. Each frame of eight bits is composed within bounding periods where the device select, NSS, is deasserted. Upon the reception of the eight bits within a byte transaction, the deassertion of NSS advances the byte counter within the internal Si834x SPI state machine. Should the transmission of an eight bit packet be corrupted, either with the deassertion of NSS before the eighth rising edge of SCLK, or with the absence of the deassertion of NSS after the eighth rising edge of SCLK, the internal SPI state machine may become unsynchronized with the master SPI controller.

To re-establish SPI synchronization with the Si834x, the SPI master may, at any time, deassert the SPI device select signal NSS, and force a clock cycle on SCLK. When unsynchronized, the rising edge of SCLK when NSS is deasserted (high) re-initializes the internal SPI state machine. The Si834x will then treat the immediately following eight bit SPI transaction after NSS is once again asserted as the first byte in a three byte SPI communication packet.

Any preceding communication packet will be abandoned by the Si834x at the point synchronization is lost, and the NSS signal is deasserted. This could occur at any point in the three byte sequence of a SPI communication packet. One should note that abandoning a SPI write operation early, even during the last byte of the three byte SPI communication packet, will leave the destination register unchanged. However, if the number of SCLK cycles exceeds eight during the last byte of the three byte SPI write packet, the destination Si834x register may be corrupted. To remedy both of these situations, it is recommended that such a corrupted write operation be repeated immediately following resynchronization of the SPI.

3.6.3 SPI Read Operation

Referring to Figure 3.12 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 32, in the SPI read operation the control byte will only have bit 6 set to a 1 in a single Si834x device organization (no daisy chaining). Bit 7 (the broadcast bit) is ignored during a read operation since only one device may be read at a time in either a single or daisy-chained organization.

The second byte in the three byte read packet is provided by the SPI master to designate the address of the Si834x internal register to be queried. If the read address provided does not correspond to a physically available Si834x internal register, all zeroes will be returned as the read value by the Si834x.

The read data is provided during the final byte of the three byte read communication packet to the querying master SPI device utilizing the Si834x's MISO output, which remains tristated at all other times.

The SPI read operation timing diagram is illustrated in the figure below.

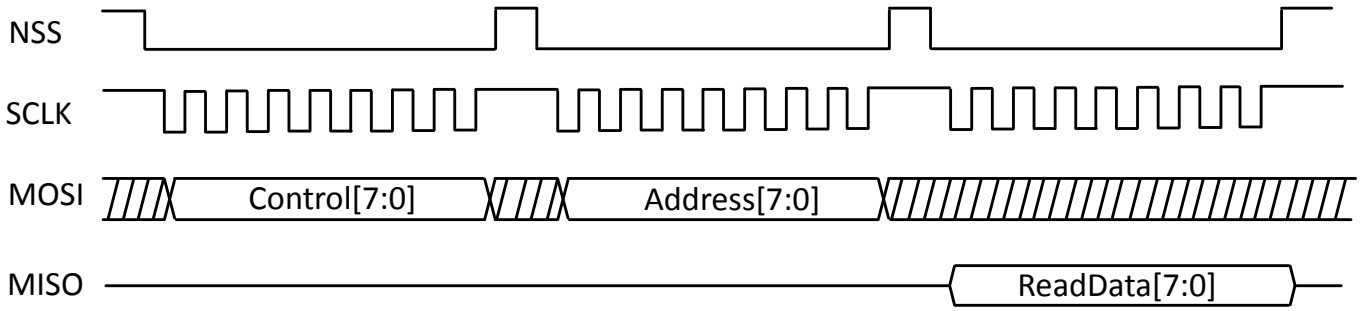


Figure 3.13. SPI Read Operation

3.6.4 SPI Write Operation

Again referring to Figure 3.12 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 32, in the SPI write operation the control byte may optionally have bit 7 (the broadcast bit) set to 1. During the SPI write operation, the broadcast bit forces all daisy-chained Si834x devices to update the designated internal SPI register with the supplied write data, regardless of the Si834x device being addressed using the CID[4:0] field of the control word.

The second byte in the three byte write packet is provided by the SPI master to designate the address of the Si834x internal register to be updated. If the write address provided does not correspond to a physically available Si834x internal register, no internal Si834x SPI register update will occur.

The write data is provided by the SPI master during the final byte of the three byte write communication packet. The Si834x MISO output remains tristated during the entire SPI write operation.

The SPI write operation timing diagram is illustrated in the figure below.

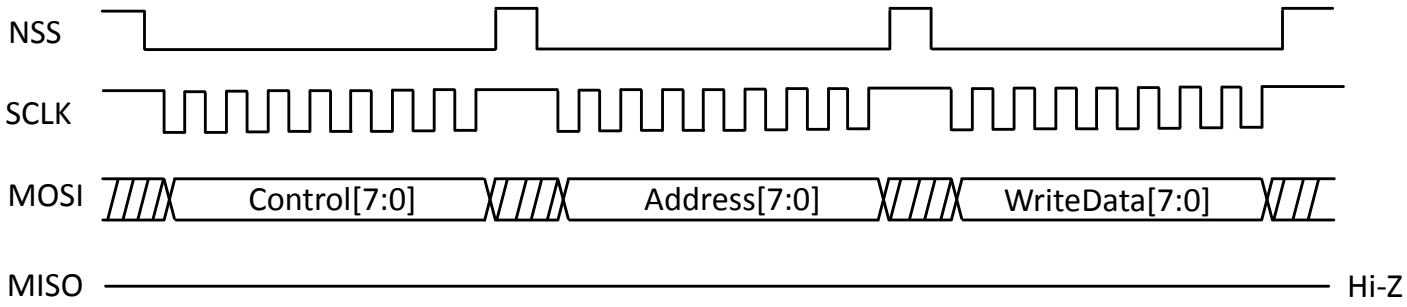


Figure 3.14. SPI Write Operation

3.6.5 SPI Daisy Chain Organization

The Si834x provides the capability to easily interconnect multiple Si834x devices on a common SPI administered by a single SPI master requiring no additional control signals. To accomplish this, the Si834x includes the additional SPI device output pin MOSI_THRU. Connecting together multiple Si834x devices in this manner utilizes the MOSI_THRU pin of one Si834x device to feed the MOSI pin of the next Si834x device in the daisy chain. All bits composing the SPI communication packet from the SPI master are passed directly through by the Si834x from the MOSI input to the MOSI_THRU output unchanged, except for the CID[4:0] field of the control byte.

The least significant five bits of the control byte in the SPI communication packet, CID[4:0], are dedicated to addressing one of up to thirty-two Si834x devices connected in a daisy chain, with 00000 indicating the device whose MOSI pin is fed directly by the SPI master, 00001 the following Si834x device, etc. As this bit field is passed through the Si834x, it is decremented by one. This five bit field is placed in the control word by the SPI master in reverse order, allowing the carry of the decrement to ripple into the next bit in the CID field as the bits of the control word proceed: CID[0] is placed at bit 4 and CID[4] placed at bit 0 of the control word. When a given Si834x device in the daisy chain is presented with the CID[4:0] code of 00000, it is activated as the one to be addressed. All remaining operations between the SPI master and the Si834x activated in this manner proceed as previously discussed in Serial Peripheral Interface for the case of a single Si834x slave. The organization of a system with Si834x devices daisy-chained in this manner is depicted in the figure below.

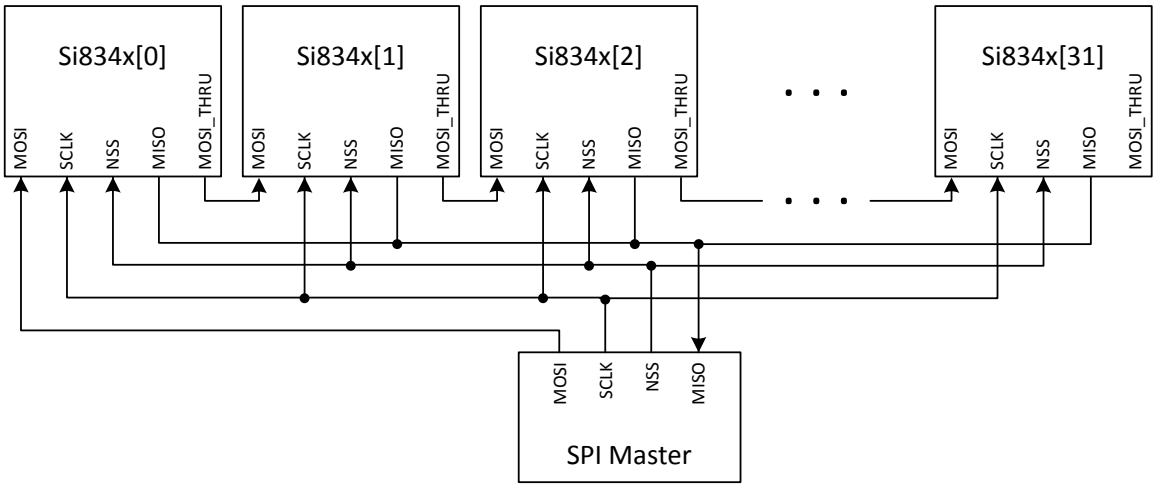


Figure 3.15. SPI Daisy-Chain Organization

From the preceding figure, and referring to Figure 3.12 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 32, in order to read from Si834x[1], the control word would be:

Control[7:0] = 0101_0000.

Similarly, in order to write to Si834x[12], the control word would be:

Control[7:0] = 0000_0110.

Finally, if it were desired to update an internal SPI register of all daisy-chained Si834x devices, the control word would be:

Control[7:0] = 1000_0000.

If the broadcast bit is zero during a write operation, only the Si834x device being addressed using the CID[4:0] field of the control word in a daisy-chain organization will be updated. If the broadcast bit is one during a write operation, the CID[4:0] field is ignored, and all Si834x devices connected in a daisy chain will be updated. For non-daisy-chain operations, the CID[4:0] field should always be all zeros.

Note that there is a finite combinational delay associated with passing the MOSI input pin of a given Si834x to the MOSI_THRU output pin. As a result, the maximum possible SCLK frequency will be reduced based on the number of Si834x devices connected in a daisy-chain organization.

3.6.6 SPI Timing Behavior

The timing diagram for the Si834x SPI is presented in the figure below.

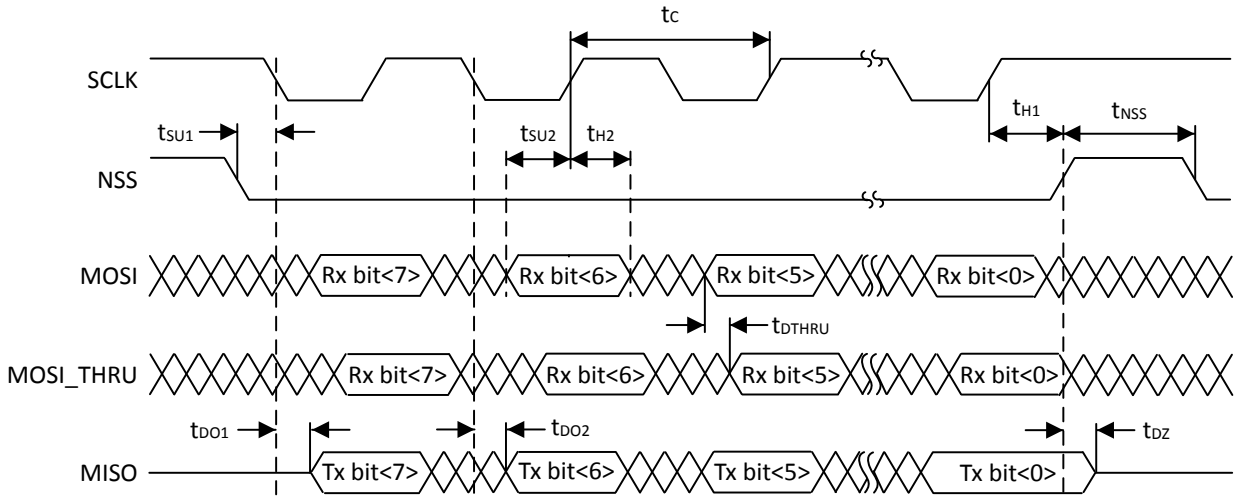


Figure 3.16. SPI Timing Diagram

The timing specifications depicted in this figure apply to each byte of the three byte Si834x SPI communications packet. Refer to the SPI timing specifications in Table 5.3 SPI Timing Characteristics on page 46.

Although this discussion of the Si834x SPI has focused on a preferred organization (separate MISO/MOSI wires), other options are available with regard to the Si834x control interface. Possible Si834x organizations include:

- MISO/MOSI wired operation
  - MISO/MOSI may be two separate wires, or may be connected together if the SPI master is capable of tristating its MOSI pin during the data byte packet transfer of a read operation.
- Multiple Si834x devices interfaced in a non-daisy-chain format
  - The SPI master provides multiple NSS signals, one for each of a multiple of Si834x slaves.
  - Every Si834x shares a single trace from its MOSI input back to the SPI master (the Si834x MOSI_THRU signal is not utilized).

4. Application Information

The Si834x is designed to be both flexible and robust to meet a wide range of application requirements, safely survive unexpected loads, and rapidly recover normal operation. To achieve these objectives, the appropriate Si834x device must be selected and its circuit carefully designed.

4.1 Recommended Application Circuits

The following examples illustrate typical circuit configurations using the Si834x Isolated Smart Switch.

4.1.1 Isolated Switch with Parallel Inputs and Diagnostic Indicators

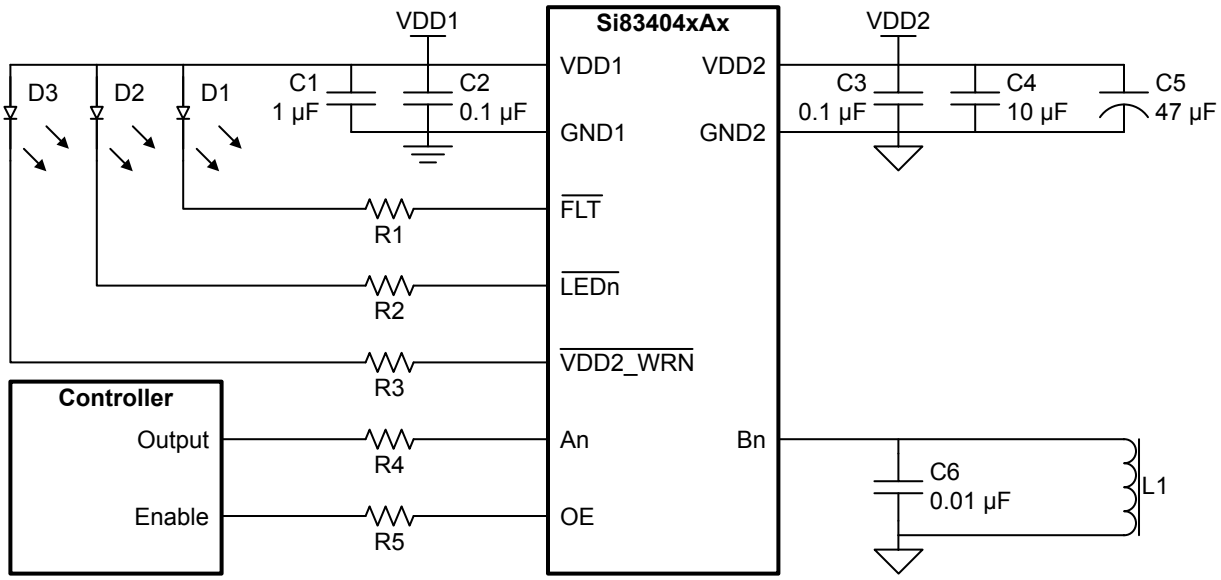


Figure 4.1. Recommended Si83404xAx Application Circuit

In the figure above, the Si834x is controlled via a simple set of digital outputs from the controller. An output enable signal is also supplied from the controller for increased fault tolerance, safety, and state control. R4 and R5 are added to improve signal integrity, especially for applications with long traces. They should be placed near the controller. Indicator LEDs D1, D2, and D3 are connected to the Si834x through current limiting resistors R1, R2, and R3 for end-user diagnostic feedback. If indicators are not desired, the indicator outputs can be connected directly to the controller with a pull-up resistor on the pin to send channel status information. The bypass capacitors, C1 through C5, on the logic interface (VDD1) and switch (VDD2) power supplies should be located as close to the chip as possible. Be sure to correctly size the decoupling capacitors based on the load and switching requirements. See Layout Considerations for more information on sizing the decoupling capacitors. Due to the sophisticated built-in switch protection of the Si834x, connecting and switching channels in parallel to increase the continuous current capability is not supported.

The figure above illustrates an Si83404xAx high-side sourcing device, however, the circuit is similar when using other Si834x devices, and the guidance given around placement and sizing of components, like current limiting resistors, remains the same for all devices. For example, VDD2_WRN is replaced with OPEN_CH when using an Si83404xBx device.

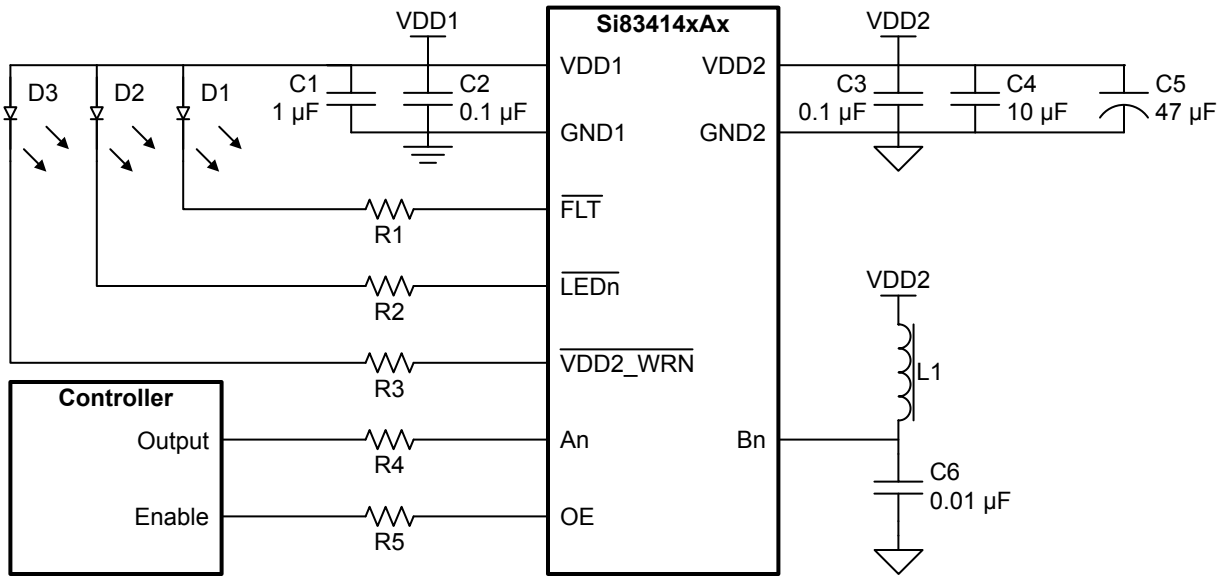


Figure 4.2. Recommended Si83414xAx Application Circuit

In the figure above, a low-side (sinking) Si83414xAx device is illustrated. It is identical to Figure 4.1 on page 36, with the exception of the circuit attached to the switch output Bn. Note that a high-side switch must source current into a load, such as the inductor L1 in Figure 4.1 on page 36. A low-side switch must sink current from a load, such as the inductor L1 in Figure 4.2 on page 37. The recommended sinking output circuit is identical for all low-side (sinking) Si834x devices.

Note that, under normal conditions, the Si834x Isolated Smart Switch requires no additional components to protect the switch output circuit such as fuses for short-circuit protection or diodes for demagnetization voltage protection (back EMF or voltage kick-back). If the application must meet a surge specification, additional protection may be required.

4.1.2 Isolated High-Side Switch with Parallel Inputs and Fault Control

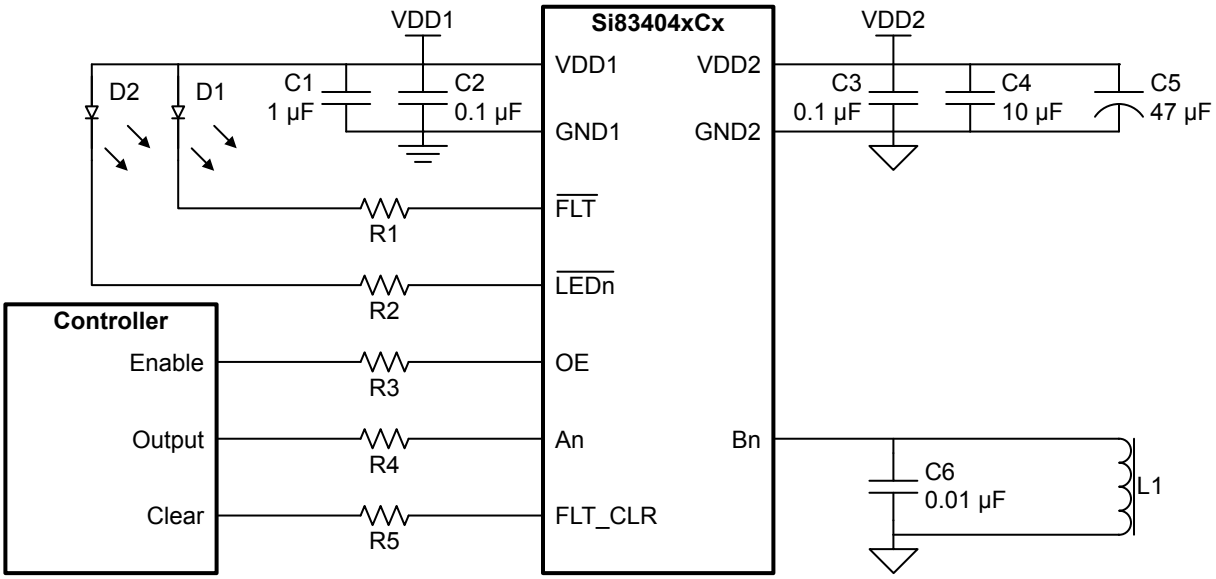


Figure 4.3. Recommended Si83404xCx Application Circuit

In the figure above, the Si834x has an additional input signal from the controller used to clear any faults reported by the device. Once a fault is reported, the FLT\ output will turn ON until both the fault condition is removed and the FLT_CLR pin is given a logic high value, manually clearing the fault report from the device. Controlled restart of the outputs after a fault can be achieved by connecting the FLT\ output to the OE input with a pull-up resistor. In this configuration, when a fault is reported, all outputs will be disabled until the fault is cleared.

4.1.3 Isolated High-Side Switch with SPI

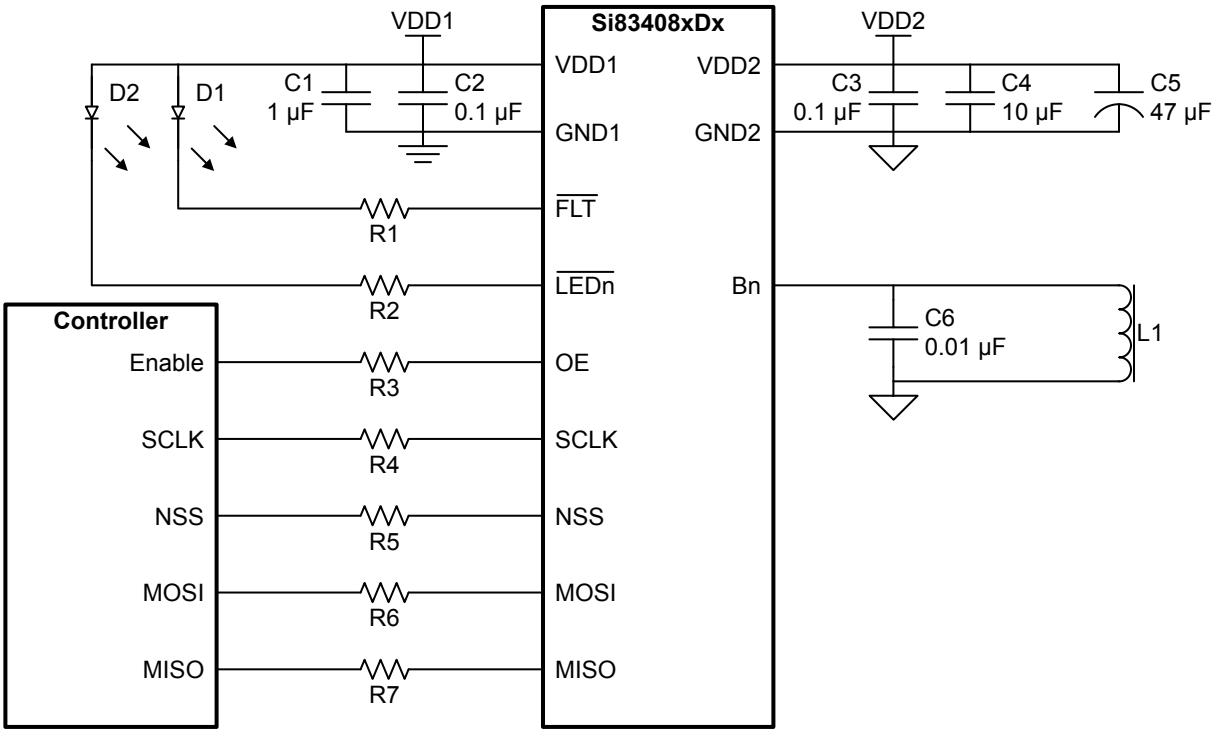


Figure 4.4. Recommended Si83408xDx Application Circuit

In the figure above, the Si834x is monitored and controlled through the SPI from the controller. Control signals to turn ON or OFF a switch, as well as device configuration signals, are communicated via the SPI only, reducing required controller pins.

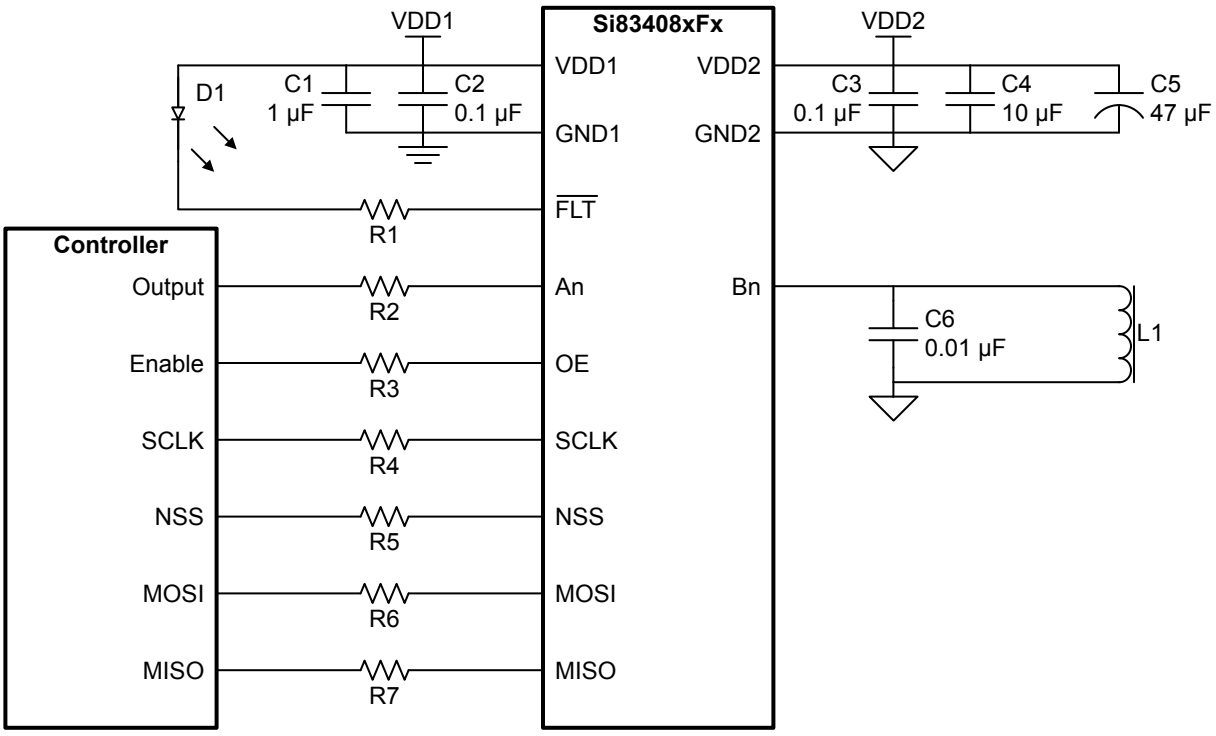


Figure 4.5. Recommended Si83408xFx Application Circuit

The Si83408xFx retains the efficient parallel input interface, while adding the SPI for configuration and diagnostics, by eliminating channel status indicator pins. This device is illustrated above. When using this device, it is recommended that channel status indicators be implemented using additional controller output pins, or by adding them to the switch output circuit.

4.2 Layout Considerations

High voltage circuits (i.e., circuits with > 30 VAC or > 60 VDC) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with < 30 VAC or < 60 VDC) by a certain distance (creepage/clearance) to ensure safety in the end-user application. If a component, such as the Si834x, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5.7 Insulation and Safety-Related Specifications on page 50 and Table 5.9 VDE 0884-10 Insulation Characteristics on page 51 provide details about the creepage/clearance and working voltage capabilities of the Si834x. These tables also detail the component standards (UL1577, VDE 0884, CSA and CQC), which are readily accepted by certification bodies to provide proof for end-system specification requirements. Refer to the end-system specification requirements before starting any design that uses the Si834x.

Several additional layout recommendations should be taken into consideration when designing for the Si834x Isolated Smart Switch device. These recommendations improve signal integrity, mitigate inrush current concerns, optimize heat dissipation, and improve the manufacturability of the end-system.

1. Place a pair of bypass capacitors as close as possible to the VDD1 power supply pin. A 0.1 µF capacitor, and a 1 µF or larger capacitor are recommended. It is important that the decoupling capacitors are selected such that the maximum VDD1 Slew Rate specification found in Table 5.12 Absolute Maximum Ratings on page 53 is not exceeded. Add a 10 Ω resistor in series with the bypass capacitor pair to form a low-pass filter for applications where VDD1 may experience a high slew rate, such as a hot-pluging event.
2. An entire PCB plane should be dedicated to the GND1 reference to improve signal integrity. If an entire PCB plane is not dedicated to the GND1 reference, be cautious of a signal's ground path when connected to the Si834x logic interface.
3. It is recommended to use a resistor on to each logic interface pin to improve signal integrity and reduce EMI concerns, especially for long traces. They should be placed as close to the controller as possible. See the Recommended Application Circuits for details.
4. To improve heat dissipation, add multiple thermal relief vias extending from the PCB pads connected to ePAD1 and ePAD2 and their appropriate ground planes, through the PCB, and exposed on the opposite side of the board. Use small-diameter vias, as large-diameter vias may reduce manufacturability.
5. Open board space surrounding the Si834x device, on the opposite side of the PCB from the Si834x device and around the thermal relief vias, further improves heat dissipation.
6. Place a pair of bypass capacitors as close as possible to the VDD2 switch power supply pin. A 0.1 µF capacitor, and a 10 µF or larger capacitor are recommended. An additional 47 µF capacitor is recommended if Inrush Current Mode will be used. It is important that the decoupling capacitors are selected such that the maximum VDD2 Slew Rate specification found in Table 5.12 Absolute Maximum Ratings on page 53 is not exceeded.
7. Bulk bypass capacitance can be added to the existing bypass capacitors on the VDD2 switch power supply. Size the bulk capacitor based upon end-system load requirements and the specified maximum VDD2 slew rate.
8. Use the widest traces possible for the switch output pins in order to handle large inrush currents.
9. To reduce EMI concerns and channel crosstalk, minimize the current return path for switch outputs. Be sure to consider the additional current return path through the bulk capacitor, especially when using a low-side (sinking) device.

4.3 Power Dissipation Considerations

When the Si834x device is operating within the rated ambient temperature range, the only significant source of temperature rise is the demagnetization of inductive loads. The Si834x was designed to drive and demagnetize 1.15 H loads on all channels simultaneously without exceeding the thermal limitations of the device. If the user exceeds the temperature limitations of the device, it will reduce the demagnetization clamp voltage to V_{CLMPL} for all channels, which will extend the turn-OFF time of all inductive loads, and all channels will be prevented from turning on again. This reduces power dissipation until the device temperature is reduced to acceptable levels. See Over-Temperature Protection for details on this process.

Due to the innovative Over-Temperature Protection feature, the designer should only be concerned about the switch temperature at the beginning of the load switching cycle. The switch temperature must be maintained below the Over-Temperature Threshold. Therefore, the Derated Ambient temperature (T_{AD}) is dependent on device power dissipation and thermal impedance. The estimated device power dissipation is composed of quiescent power dissipation (P_Q) and power dissipation for each channel (P_{CH}) as shown in Equation 4.3.1 and supported by Equations 4.3.2 and 4.3.3.

$$T_{AD} < T_{OT} - T_{HYS} - \theta_{JA}(P_Q + n_{CH} \cdot P_{CH}) \quad \textbf{Equation 4.3.1}$$

Where:

T_{OT} is the Over-Temperature Threshold (˚C).

T_{HYS} is the Over-Temperature Hysteresis (˚C).

$ø_{JA}$ is the Junction-to-Ambient thermal resistance (˚C/W).

n_{CH} is the number of channels actively driving a load.

The logic interface contributes a negligible amount of power to the total device power dissipation. To simplify the estimate, it has been removed from both P_Q and P_{CH} in the equations below.

$$P_Q = IDD2_Q \cdot VDD2 \quad \textbf{Equation 4.3.2}$$

Where:

$IDD2_Q$ is the VDD2 Supply Quiescent Current (A).

VDD2 is the VDD2 Supply Voltage (V).

For a conservative power dissipation estimate, the maximum quiescent current specification $IDD2_{Q(MAX)}$ should be used in Equation 4.3.2.

The power dissipated by a single channel is estimated by Equation 4.3.3 and supported by Equations 4.3.4 through 4.3.7. It is comprised of the power dissipation when the channel is ON (P_{ON}), the power dissipated when the channel is turning on (P_{SW}), and the power dissipated when the channel is turning off and demagnetizing an inductor (P_{CLMP}).

$$P_{CH} = P_{ON} + P_{SW} + P_{CLMP} \quad \textbf{Equation 4.3.3}$$

The estimated power dissipation when the channel is ON, given by Equation 4.3.4, is dependent on the current through the load, the switch's ON-State Resistance, and how long the load is driven.

$$P_{ON} = I_L^2 \cdot R_{ON} \cdot \frac{t_{ON}}{t_{SW}} \quad \textbf{Equation 4.3.4}$$

Where:

I_L is the current through the load (A).

R_{ON} is the ON-State Output Resistance (Ω).

t_{ON} is the time during a single switching period that the channel is ON (s).

t_{SW} is the switching period of the channel (s).

For a conservative power dissipation estimate, the maximum current through the load and the maximum ON-State Output Resistance should be used in Equation 4.3.4.

The estimated power dissipation when the channel is turning on, given by Equation 4.3.5, is dependent on the switch supply voltage, the load capacitance, and the switching period.

$$P_{SW} = VDD2^2 \cdot \frac{C_L}{2 \cdot t_{SW}} \quad \textbf{Equation 4.3.5}$$

Where:

VDD2 is the VDD2 Supply Voltage (V).

C_L is the load capacitance (C).

t_{SW} is the switching period of the channel (s).

Note that the load capacitance (C_L) should include any capacitance built into the circuit, such as the 10 nF capacitor recommended in Layout Considerations.

The estimated power dissipation when the channel is turning off and demagnetizing an inductor is dependent on the current through the load, the smart output clamp voltage, and the switching period. If the current through the load is greater than the Demagnetization Clamp Current Threshold ($I_L > I_{CLMPT}$), then use Equation 4.3.6 for the power dissipated by a single channel (P_{CH}).

$$P_{CLMP} = \begin{aligned} & V_{CLMPL} \cdot \frac{I_L + I_{CLMPT}}{2} \cdot \frac{L(I_L - I_{CLMPT})}{\left(R_L \frac{I_L + I_{CLMPT}}{2} + V_{CLMPL}\right) T_{sw}} \\ & + V_{CLMPH} \cdot \frac{I_{CLMPT}}{2} \cdot \frac{I_{CLMPT} \cdot L}{\left(\frac{I_{CLMPT} \cdot R_L}{2} + V_{CLMPH}\right) T_{SW}} \end{aligned} \quad \textbf{Equation 4.3.6}$$

Where:

V_{CLMPL} is the Demagnetization Clamp Low Voltage (V).

V_{CLMPH} is the Demagnetization Clamp High Voltage (V).

I_L is the current through the load (A).

I_{CLMPT} is the Demagnetization Clamp Current Threshold (A).

L is the inductance of the load (H).

R_L is the resistance of the load(Ω).

T_{SW} is the switching period of the channel (s).

For a conservative power dissipation estimate, the maximum current through the load should be used in Equation 4.3.6 and Equation 4.3.7. The time during a single switching period (T_{SW}) that the channel is OFF must be large enough to completely discharge the load inductance.

If the current through the load is less then the Demagnetization Clamp Current Threshold ($I_L < I_{CLMPT}$), then use Equation 4.3.7 for the power dissipated by a single channel (P_{CH}).

$$P_{CLMP} = V_{CLMPH} \cdot \frac{I_L}{2} \cdot \frac{I_L \cdot L}{\left(\frac{I_L \cdot R_L}{2} + V_{CLMPH}\right) T_{SW}} \quad \textbf{Equation 4.3.7}$$

Where:

V_{CLMPH} is the Demagnetization Clamp High Voltage (V).

I_L is the current through the load (A).

L is the inductance of the load (H).

R_L is the resistance of the load (Ω).

T_{SW} is the switching period of the channel (s).

5. Electrical Specifications

Table 5.1. Power Supply Characteristics

Operating range for the following specifications: VDD1 = 2.25 - 5.5 V; VDD2 = 9 - 32 V; T_A = –40 to +125 °C; Typical specs: VDD1 = 5 V; VDD2 = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD1 Supply Voltage	VDD1		2.25	—	5.5	V
VDD2 Supply Voltage	VDD2		9	24	32	V
VDD1 Undervoltage Threshold	$VDD1_{UV+}$	VDD1 rising	1.90	2.03	2.16	V
	$VDD1_{UV-}$	VDD1 falling	1.85	1.99	2.1	V
VDD1 Undervoltage Hysteresis	$VDD1_{HYS}$		—	50	—	mV
VDD2 Undervoltage Threshold	$VDD2_{UV9+}$	VDD2 rising	8.2	8.6	9.0	V
	$VDD2_{UV9-}$	VDD2 falling	8	8.35	8.7	
VDD2 Undervoltage Hysteresis	$VDD2_{UV9HYS}$		—	200	—	mV
VDD2 ESD Clamp Threshold	$VDD2_{CLMP}$	I_{CLMP} = 1 mA	—	48	—	V
VDD1 Supply Quiescent Current	$IDD1_Q$	All An = LOW	3.3	3.6	4.3	mA
VDD2 Supply Quiescent Current	$IDD2_Q$	All An = LOW	8	9.8	12	mA
VDD1 Supply Active Current						
1 Channel Active	$IDD1_{1CH}$	Active An inputs toggling at 1 kHz (50% duty cycle)	—	4.1	—	mA
All Channels Active	$IDD1_{ALL}$		3.5	4.2	5	
VDD2 Supply Active Current						
1 Channel Active	$IDD1_{1CH}$	Active Bn outputs toggling at 1 kHz (50% duty cycle), no load	—	10.2	—	mA
All Channels Active	$IDD1_{ALL}$		8	10	12	
Device Startup Time[1]	t_{ST}		—	2.0	—	ms
VDD1 Logic Interface Power Cycle Time[1]	t_{PC1}		—	80	—	µs
VDD2 Switch Power Cycle Time[1]	t_{PC2}		—	2.4	—	ms
VDD1 Logic Interface Shutdown Time[1]	t_{SD1}		—	2.9	—	µs

Note:

1. Startup, power cycle, and shutdown timing are detailed in Switch Timing Behavior.

Table 5.2. Logic Interface Characteristics

Operating range for the following specifications: VDD1 = 2.25 - 5.5 V; VDD2 = 9 - 32 V; T_A = –40 to +125 °C; Typical specs: VDD1 = 5 V; VDD2 = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IL}	VDD1 = 2.5 V ± 10%	—	—	VDD1 x 0.2	V
		VDD1 = 3.3 V ± 10%	—	—	0.8	
		VDD1 = 5.0 V ± 10%	—	—	1	
High Level Input Voltage	V_{IH}	VDD1 = 2.5 V ± 10%	VDD1 x 0.5	—	—	V
		VDD1 = 3.3 V ± 10%	2.0	—	—	
		VDD1 = 5.0 V ± 10%	2.3	—	—	
Input Hysteresis	V_{HYS}		—	0.25	—	V
Input Capacitance	C_I		—	2	—	pF
Input Leakage Current	$\lvert I_{LKG} \rvert$		—	—	1	µA
Low Level Output Voltage[1]	V_{OL}	I_{OH} = 4 mA	—	—	0.4	V
High Level Output Voltage[1]	V_{OH}	I_{OH} = -4 mA	VDD1 - 0.4	—	—	V
Output Impedance						
Logic Output[1]	Z_{OH}		—	50	—	Ω
	Z_{OL}		—	65	—	
Indicator Output[2]	Z_{OLED}		—	30	—	
Indicator Output Current[2]	I_{OLED}	V_{OLED} = 0.5 V	8	—	—	mA

Note:

1. Parameter applies to MOSI_THRU, and MISO logic output pins.
2. Parameter applies to FLT\, VDD2_WRN\, OPEN_CH\, LEDn\ indicator output pins. Indicator outputs use an active-low, open-drain configuration where current is sinked into the pin. See Recommended Application Circuits for more information.

Table 5.3. SPI Timing Characteristics

Operating range for the following specifications: VDD1 = 2.25 - 5.5 V; VDD2 = 9 - 32 V; T_A = –40 to +125 °C; Typical specs: VDD1 = 5 V; VDD2 = 24 V; T_A = 25 °C

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time (SCLK)[2]	t_C	100	—	—	ns
SCLK High or Low Time	t_{PW}	30	—	—	ns
Delay time, SCLK fall to MISO active	t_{DO1}	—	—	20	ns
Delay time, SCLK fall to MISO transition	t_{DO2}	—	—	20	ns
Delay time, NSS rise to MISO hi-Z	t_{DZ}	—	—	20	ns
Setup time, NSS fall to SCLK fall	t_{SU1}	25	—	—	ns
Hold time, SCLK rise to NSS rise	t_{H1}	20	—	—	ns
Setup time, MOSI to SCLK rise	t_{SU2}	25	—	—	ns
Hold time, SCLK rise to MOSI transition	t_{H2}	20	—	—	ns
Delay time between NSS active	t_{NSS}	200	—	—	ns
Propagation delay, MOSI to MOSI_THRU[2]	t_{DTHRU}	—	—	15	ns

Note:

1. See Figure 3.16 SPI Timing Diagram on page 35 for SPI timing characteristics test conditions.
2. When implementing a daisy chain, see SPI Daisy Chain Organization for cycle time considerations. Cycle time will increase according to $t_C(N) = t_{C(MIN)} + t_{DTHRU}(N-1)$ where N is the number of Si834x devices present in the daisy chain.

Table 5.4. Load Driving Characteristics

Operating range for the following specifications: VDD1 = 2.25 - 5.5 V; VDD2 = 9 - 32 V; T_A = –40 to +125 °C; Typical specs: VDD1 = 5 V; VDD2 = 24 V; T_A = 25 °C; C_L=10 nF; R_{LOAD} = 47 Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Recommended High or Low Pulse Width	MPW	An or OE pins	10	—	—	µs
Turn ON Propagation Delay[1]						
Si8340x Sourcing Devices	t_{PLH}		—	2.3	—	µs
Si8341x Sinking Devices			—	2.1	—	
Turn OFF Propagation Delay[2]						
Si8340x Sourcing Devices	t_{PHL}		—	2.9	—	µs
Si8341x Sinking Devices			—	2.2	—	
Channel-Channel Skew[3]	t_{PSK}		—	—	250	ns
Si8340x Sourcing Output Rise Time[4]	t_R		—	3.0	—	µs
Si8341x Sinking Output Fall Time[5]	t_F		—	3.0	—	µs
Turn ON Voltage Slope						
Si8340x Sourcing Devices	dV/dt_{ON}		—	8.3	—	V/µs
Si8341x Sinking Devices			—	8.3	—	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Turn OFF Voltage Slope						
Si8340x Sourcing Devices	dV/dt_{OFF}		—	7.6	—	V/µs
Si8341x Sinking Devices			—	10.2	—	
OFF State Output Current	$\lvert I_{O(OFF)} \rvert$	$V_{O(OFF)}$ = 0 V to VDD2	—	—	100	µA
ON State Load Current	$\lvert I_{O(ON)} \rvert$	Continuous operation	—	0.5	0.7	A
ON-State Output Resistance	R_{ON}	I_{OL} = 0.5 A, VDD2 = 24 V	—	145	280	mΩ
Load Capacitance	C_L		10	—	1000	nF
Demagnetization Current to Engage Clamp	$I_{CLMP(MIN)}$		1	—	—	mA

Note:

1. Turn ON propagation delay is measured from the time the input (An or OE) is 50% ON to the time the output (Bn) is 10% ON and rising. See Figure 5.1 Turn ON and Turn OFF Timing on page 47 for measurement details.
2. Turn OFF propagation delay is measured from the time the input (An or OE) is 50% ON to the time the output (Bn) is 90% ON and falling. See Figure 5.1 Turn ON and Turn OFF Timing on page 47 for measurement details.
3. Channel-channel skew is the magnitude of the difference in turn ON or turn OFF propagation delay times measured between different channels operating at the same supply voltages, load, and ambient temperature.
4. Output rise time is measured from the time the output is 10% ON to the time the output is 90% ON. For sinking output devices (Si8341x), rise time is determined by load conditions. See Figure 5.1 Turn ON and Turn OFF Timing on page 47 for measurement details.
5. Output fall time is measured from the time the output is 90% ON to the time the output is 10% ON. For sourcing output devices (Si8340x), fall time is determined by load conditions. See Figure 5.1 Turn ON and Turn OFF Timing on page 47 for measurement details.

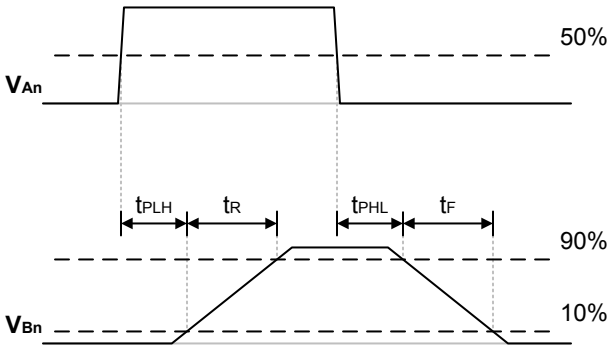


Figure 5.1. Turn ON and Turn OFF Timing

Table 5.5. Protection and Diagnostics

Operating range for the following specifications: VDD1 = 2.25 - 5.5 V; VDD2 = 9 - 32 V; T_A = –40 to +125 °C; Typical specs: VDD1 = 5 V; VDD2 = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode Transient Immunity	CMTI		100	—	—	kV/µs
Output Current Limit[1]	I_{OCL}		0.7	0.88	1.1	A
Output Current Limit Threshold[2]	I_{OCLT}		—	1.15	—	A
Output Current Limit Pulse[3]	t_{OCL}		—	155	—	µs
Output Current Limit Period[3]	t_{OCLP}		—	1	—	ms
Over-Current Protection Duration[3]	t_{OCPD}		—	6	—	ms
Output Peak Current Limit[4]	I_{OPCL}		—	8	—	A
Output Peak Current Test Pulse[4]	t_{OPCT}		—	11.5	—	µs
Output Peak Current Limit Pulse[4]	t_{OPCL}		—	20	—	ms
Over-Current Protection Retry Delay	t_{OPRD}		—	500	—	ms
Demagnetization Clamp High Voltage[5]						
Si8340x Sourcing Devices	V_{CLMPH}	I_O = 1 mA	—	-17.5	—	V
Si8341x Sinking Devices			—	VDD2+17.5	—	
Demagnetization Clamp Low Voltage[5]						
Si8340x Sourcing Devices	V_{CLMPL}	$I_O \geq I_{CLMPT}$	—	-2.1	—	V
Si8341x Sinking Devices			—	VDD2+2.1	—	
Demagnetization Clamp Current Threshold[5]	I_{CLMPT}		—	0.4	—	A

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Load Resistance Threshold for Open-Circuit Diagnostic	R_{LMAX}	9 V ≤ VDD2 < 16 V	40	—	—	kΩ
		VDD2 ≥ 16V	100	—	—	kΩ
VDD2 Low-Voltage Threshold	$VDD2_{UV18+}$	VDD2 rising	—	18.5	—	V
	$VDD2_{UV18-}$	VDD2 falling	—	18.0	—	
VDD2 Overvoltage Threshold[6]	$VDD2_{OV32+}$	VDD2 rising	—	33.5	—	V
	$VDD2_{OV32-}$	VDD2 falling	—	33	—	
Over-Temperature Threshold[7]	T_{OT}		159	167	175	°C
Over-Temperature Hysteresis	T_{HYS}		—	33	—	°C

Note:

1. The current limit is applied when an output is first turned ON, and when over-current conditions are present on the output. It is applied in a pulsed fashion for t_{OCL} and repeats for t_{OCPD}. See Switch Protection for details.
2. The current measured through the output must exceed this threshold in order to be detected as an over-current condition and for the Output Current Limit (I_{OCL}) to be enforced. See Switch Protection for details.
3. Period may be reduced during operation if over-current conditions are removed. See Switch Protection for details.
4. Peak output current is only available for a short time period t_{OPCL}, and only during a perceived over-current condition detected when the output is first turned ON or after the Over-Current Protection Retry Delay. See Switch Protection for details.
5. The demagnetization clamp voltage is V_{CLMPL} while the current through the output is equal to or above I_{CLMPT}. When current through the output is below I_{CLMPT}, the demagnetization clamp voltage is V_{CLMPH}. Under certain fault conditions, this behavior is modified and performance is constrained. See Switch Protection for details.
6. Inductive load demagnetization performance is constrained above this threshold. See Switch Protection for details.
7. Any channel that exceeds the Over-Temperature Threshold will have its demagnetization performance constrained. If all channels exceed the Over-Temperature Threshold, all channels will be unconditionally shutdown. By default, this behavior will persist until the Over-Temperature condition(s) are removed. See Switch Protection for details.

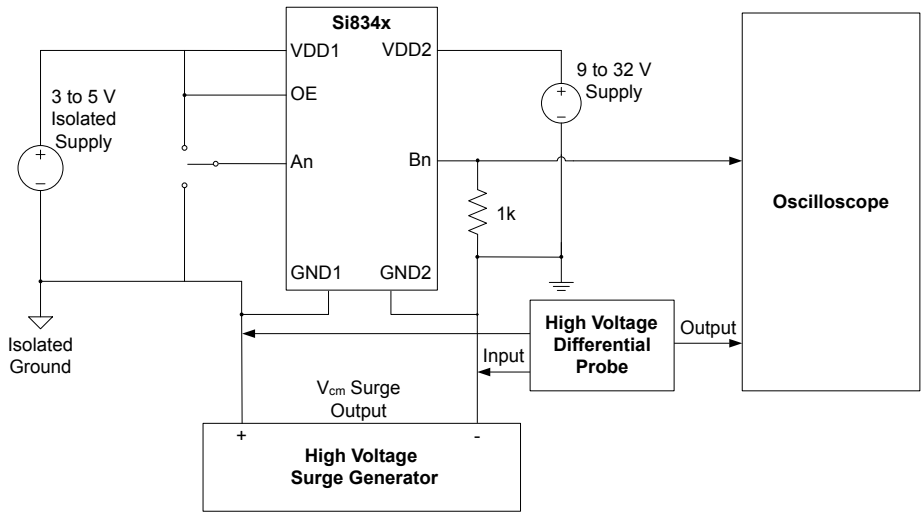


Figure 5.2. Common Mode Transient Immunity (CMTI) Test Circuit for Sourcing Device

Table 5.6. Regulatory Information (Pending)

CSA
Certified under IEC 60950-1, 62368-1. For more details, see Master Contract Number 232873.
VDE
Certified according to VDE-0884. For more details, see File 5006301-4880-0001.
Up to 560 V_{peak} for basic insulation working voltage.
UL
Certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to1500 V_{RMS} isolation voltage for basic insulation.
CQC
Certified under GB4943.1-2011.
Note: Regulatory Certifications apply to 1.5 kV_{RMS} rated devices which are production tested to 1.8 kV_{RMS} for 1 second. For more information, see Ordering Guide.

Table 5.7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	9x9 DFN-32	Unit
Nominal External Air Gap (Clearance)	CLR		3.5 min	mm
Nominal External Tracking (Creepage)	CPG		3.5 min	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.008	mm
Tracking Resistance	CTI	IEC60112	600	V
Erosion Depth	ED		0.040	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)	C_{IO}	f = 1 MHz	1	pF

Note:

1. To determine resistance and capacitance, the Si834x is converted into a 2-terminal device. Pins 1–16 are shorted together to form the first terminal, and pins 17 – 32 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 5.8. IEC 60664-1 Ratings

Parameter	Test Condition	9x9 DFN-32
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 50 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 100 V_{RMS}	I-III

Table 5.9. VDE 0884-10 Insulation Characteristics

Parameter	Symbol	Test Condition	9x9 DFN-32	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V_{PEAK}
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x1.875 = V_{PR}, 100% Production Test, t_m=1 sec, Partial Discharge < 5 pC)	1050	V_{PEAK}
Transient Overvoltage	V_{IOTM}	t = 60 sec	2000	V_{PEAK}
Surge Voltage	V_{IOSM}	Tested with 2000 V	1538	V_{PEAK}
Pollution Degree (DINVDE 0110, Table 1)			2	
Insulation Resistance at TS,VIO = 500 V	R_S		$>10^9$	Ω

Note: This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si834x provides a climate classification of 40/125/21.

Table 5.10. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max	Unit
			9x9 DFN-32	
Safety Temperature	T_S		150	°C
Safety Current	I_S	θ_{JA} = 30 °C/W, T_J = 150 °C, T_A = 25 °C, VDD2 = 32 V	130	mA
Output Power	P_S	θ_{JA} = 30 °C/W, T_J=150 °C, T_A = 25 °C	4	W

Note: Maximum value allowed in the event of a failure; for more information, see Thermal Derating Curve Figure 5.3 on page 52.

Table 5.11. Thermal Characteristics

Parameter	Sym-bol	Test Condition	Min	Max	Unit
Ambient Temperature[1]	T_A		-40	125	°C
9x9 DFN-32 Package Thermal Resistance					
Junction-to-Ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	—	30	ºC/W
		2-layer, Si834x-KIT evaluation board	—	25	ºC/W
Junction-to-Case (Exposed Pad)	θ_{JC}	4-layer, 2s2p JEDEC test board	—	1.5	ºC/W

Note:

1. The maximum ambient temperature is dependent on data frequency, output load conditions, fault conditions, number of operating channels, and supply voltages. See Power Dissipation Considerations for more details.

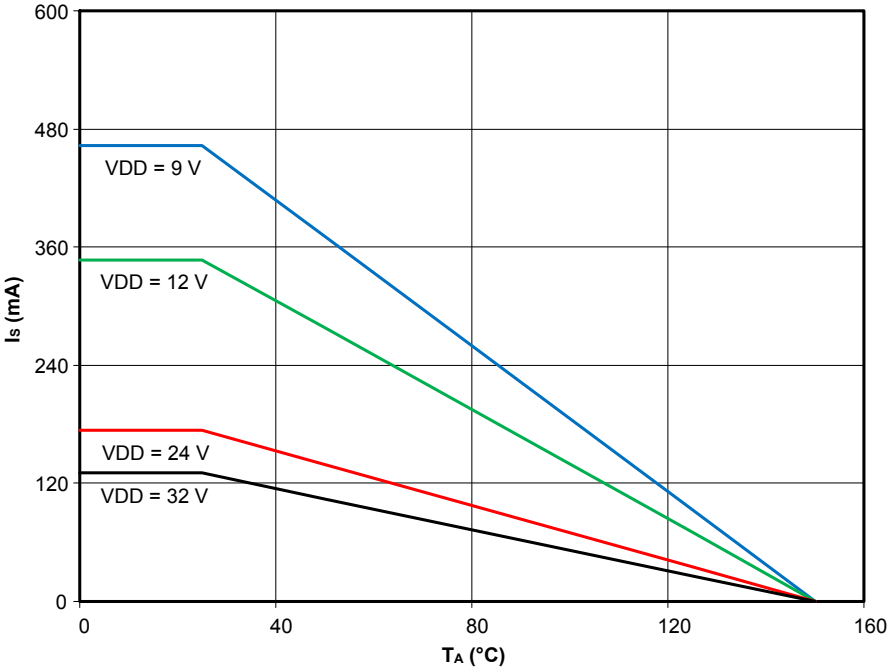


Figure 5.3. Safety Current (I_S) vs. Ambient Temperature (T_A) Derating Curve

Table 5.12. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
VDD1 Supply Voltage	VDD1	-0.3	7	V
VDD2 Supply Voltage	VDD2	-0.3	40	V
VDD1 Slew Rate	$VDD1_{\Delta}$	—	1	V/µs
VDD2 Slew Rate[2]	$VDD2_{\Delta}$	—	1	V/µs
Storage Temperature[3]	T_{STG}	-65	+150	°C
Junction Temperature	T_J	—	+175	°C
Voltage on Any Logic Pin with Respect to Ground	V_{IO-G}	-0.3	VDD1+0.3	V
One Channel Single Pulse Turn OFF Energy Dissipation[4]	$E_{AS(1CH)}$	—	Unlimited	J
All Channels Simultaneously Driven Single Pulse Turn OFF Energy Dissipation[4]				
Si8340x Sourcing Devices	$E_{AS(ALL)}$	—	8	J
Si8341x Sinking Devices		—	2.5	J
Lead Solder Temperature (10 s)		—	260	°C
Human Body Model (JEDEC JS-001) ESD Rating	ESD_{HBM}	5	—	kV
Charged Device Model (JEDEC JS-002) ESD Rating	ESD_{CDM}	1	—	kV

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at https://www.skyworksinc.com/Product_Certificate.aspx.
2. Absolute maximum slew rate only applies to supply voltage changes larger than 3 V.
3. VDE certifies storage temperature from –40 to 150 °C.
4. Tested at T_A = 125 ˚C and maximum Load Current $I_{O(ON)}$ for the channel. See Table 5.4 Load Driving Characteristics on page 46 for details.

5.1 Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in the Electrical Specifications for actual specification limits.

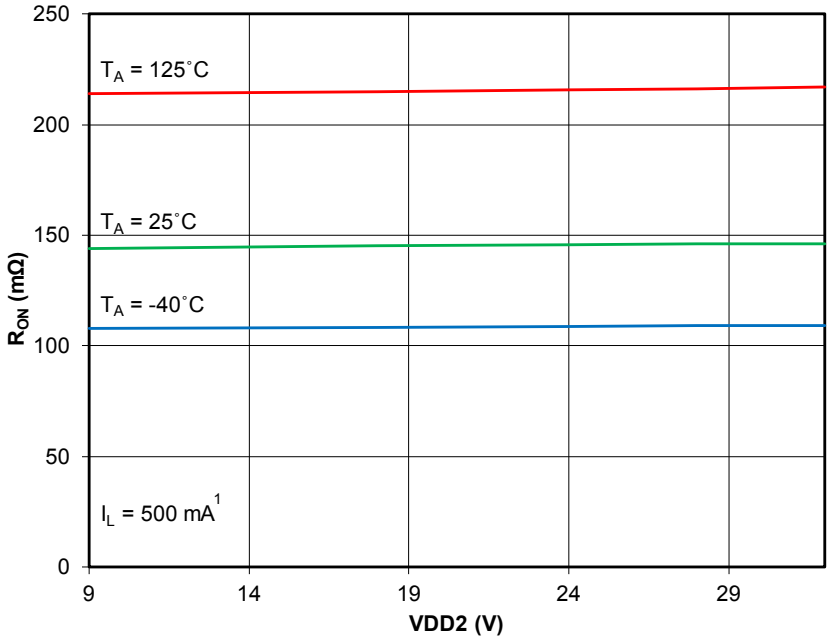


Figure 5.4. On Resistance (R_{ON}) vs. Switch Supply Voltage (VDD2)

Note:

1. I_L is the current sinking or sourcing through the output channel depending on the output channel configuration. See Switch Types for details.

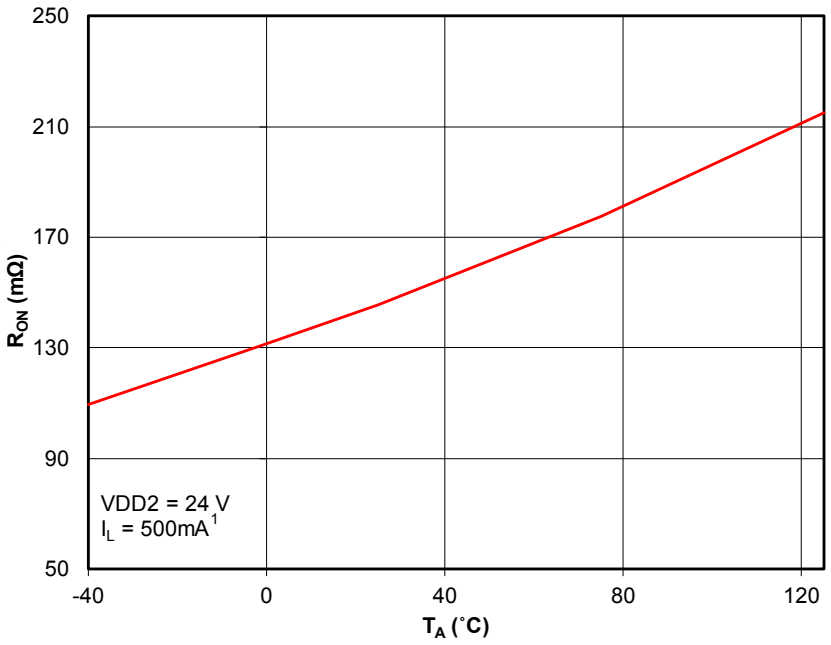


Figure 5.5. On Resistance (R_{ON}) vs. Ambient Temperature (T_A)

Note:

1. I_L is the current sinking or sourcing through the output channel depending on the output channel configuration. See Switch Types for details.

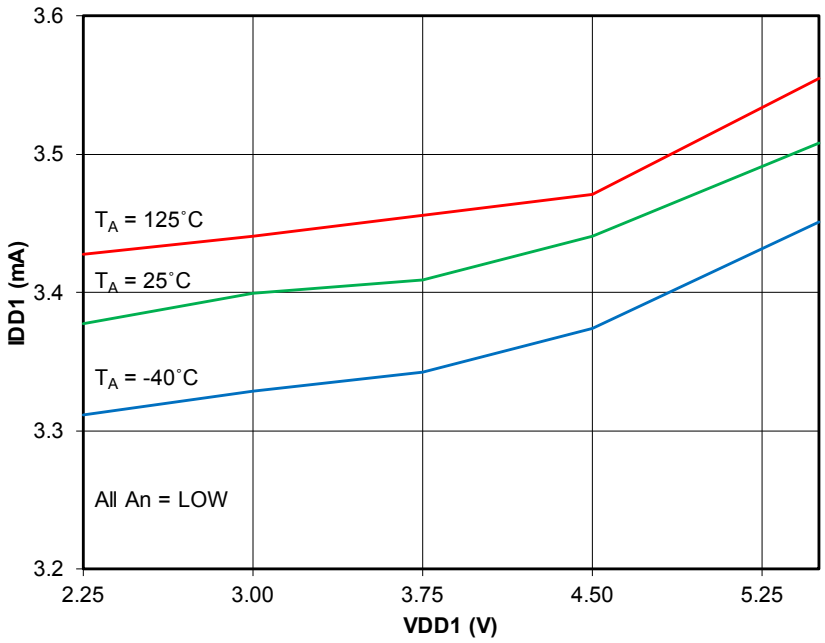


Figure 5.6. Logic Interface Supply Quiescent Current ($IDD1_Q$) vs. Logic Interface Supply Voltage (VDD1)

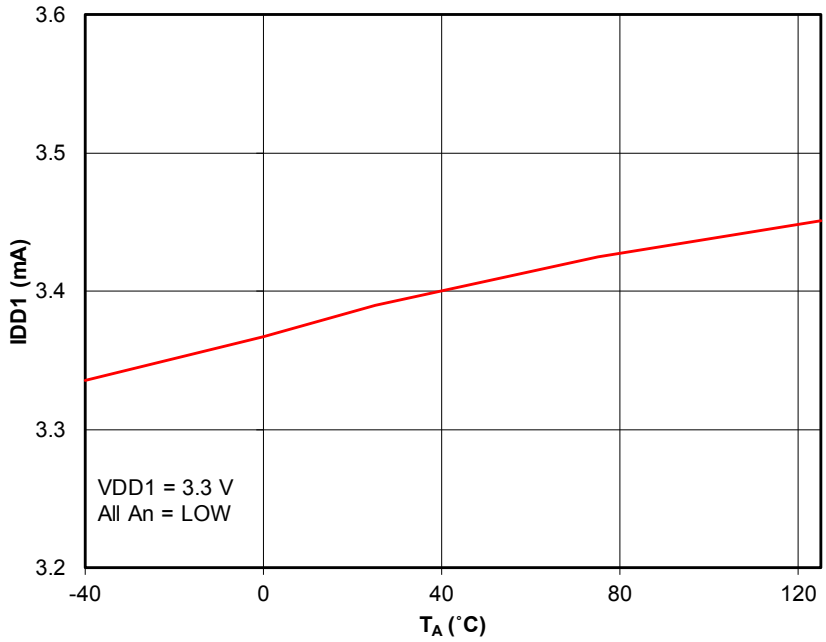


Figure 5.7. Logic Interface Supply Current Quiescent ($IDD1_Q$) vs. Ambient Temperature (T_A)

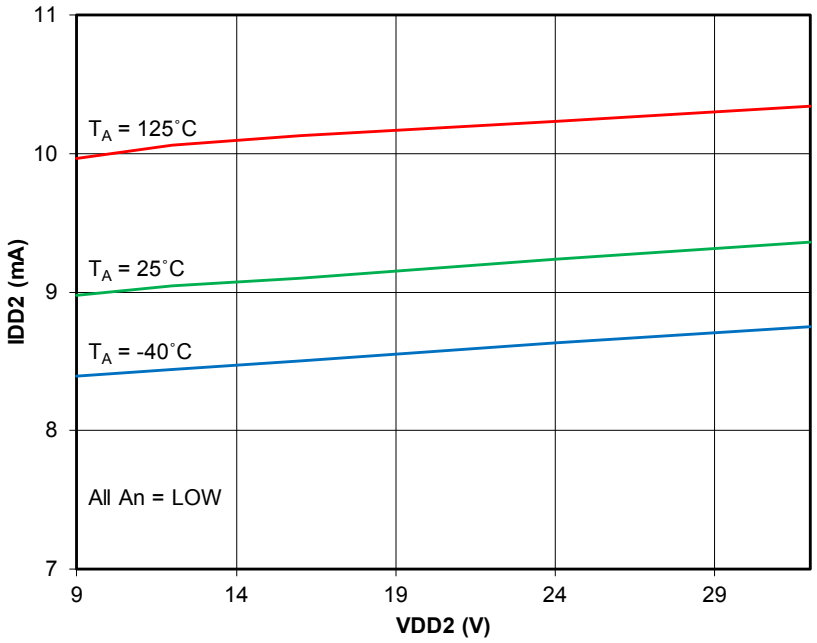


Figure 5.8. Switch Supply Quiescent Current ($IDD2_Q$) vs. Switch Supply Voltage (VDD2)

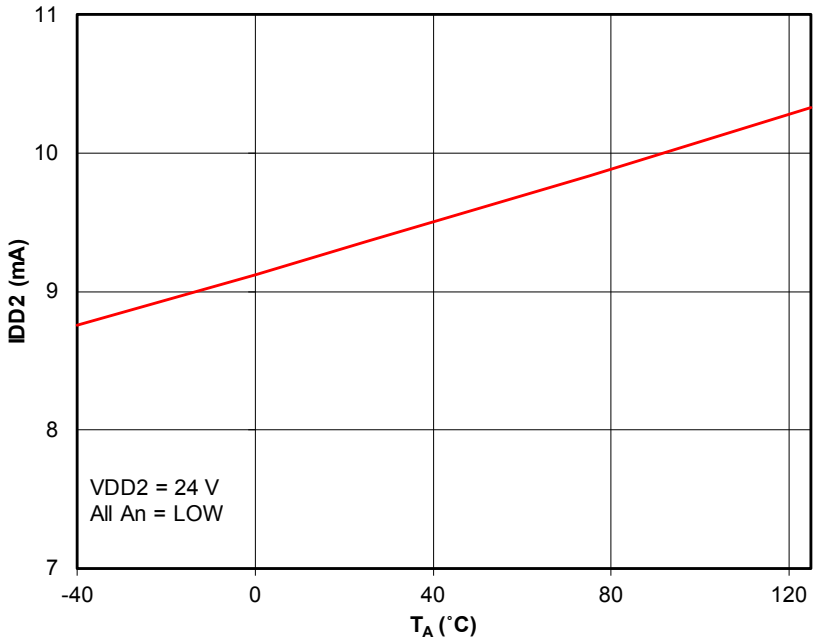


Figure 5.9. Switch Supply Quiescent Current ($IDD2_Q$) vs. Ambient Temperature (T_A)

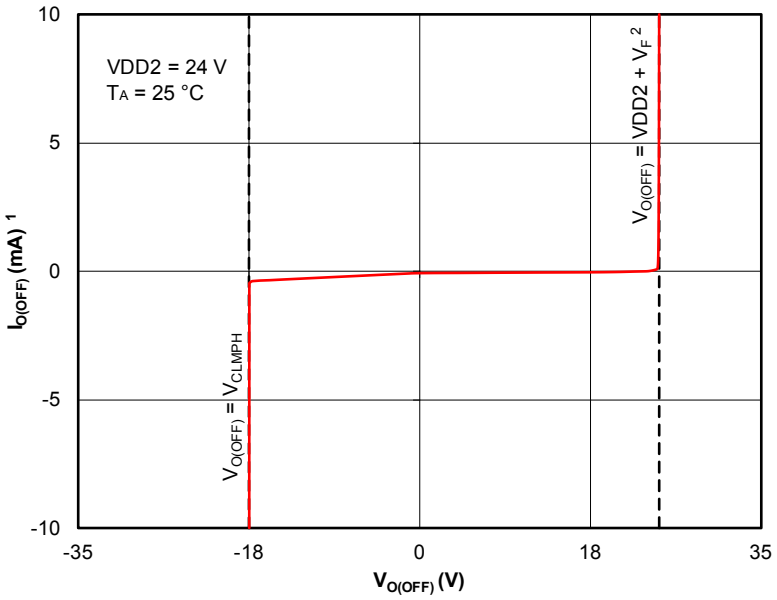


Figure 5.10. OFF State Output Current ($I_{O(OFF)}$) vs. Output Voltage ($V_{O(OFF)}$) for Sourcing Devices

Note:

1. $I_{O(OFF)}$ is considered positive when current is flowing into the output pin.
2. V_F denotes the voltage of a forward biased diode.

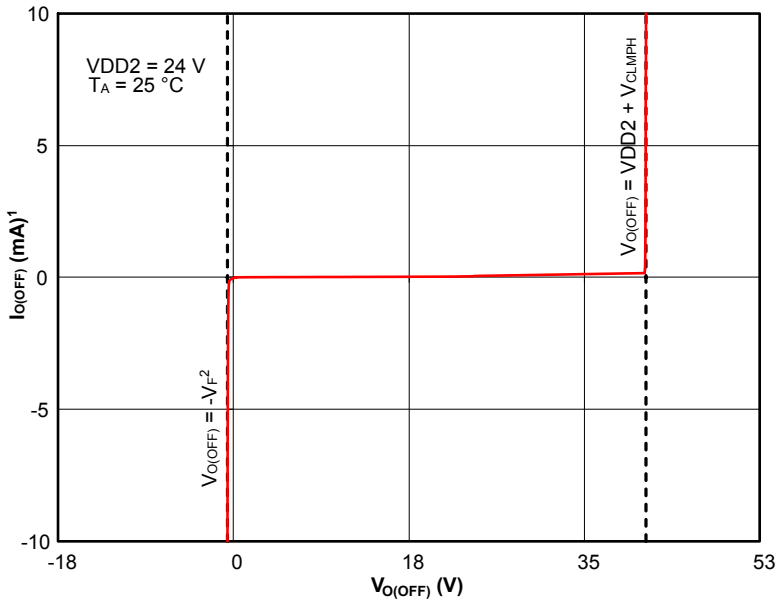


Figure 5.11. OFF State Output Current ($I_{O(OFF)}$) vs. Output Voltage ($V_{O(OFF)}$) for Sinking Devices

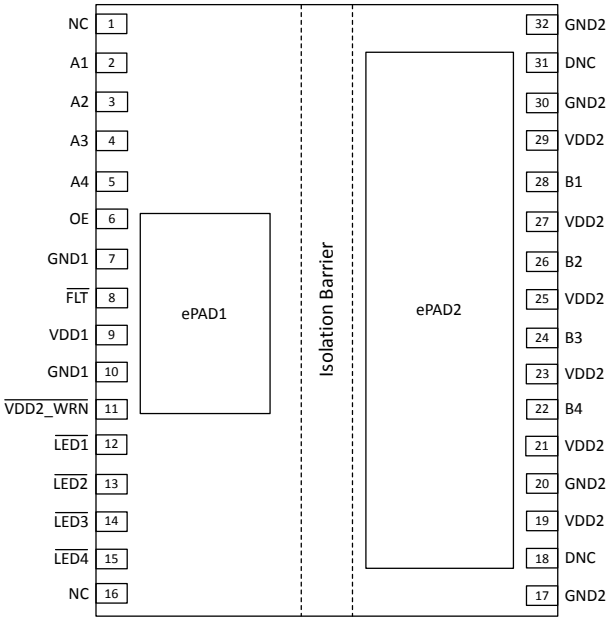
Note:

1. $I_{O(OFF)}$ is considered positive when current is flowing into the output pin.
2. V_F denotes the voltage of a forward biased diode.

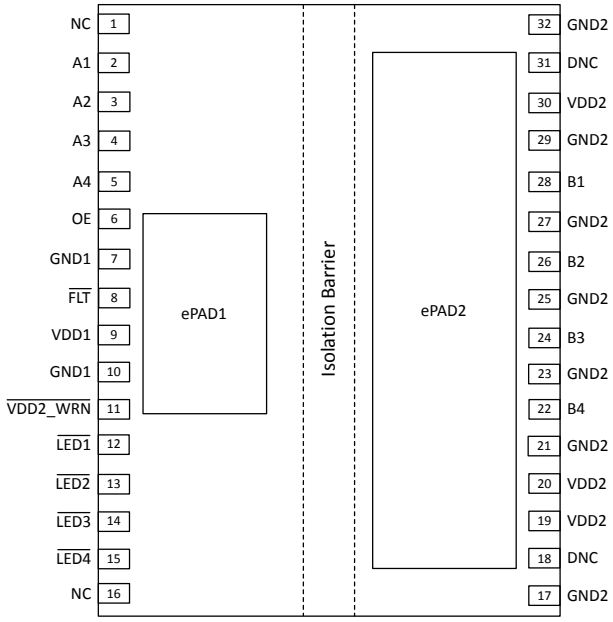
6. Pin and Package Descriptions

6.1 Pin Descriptions

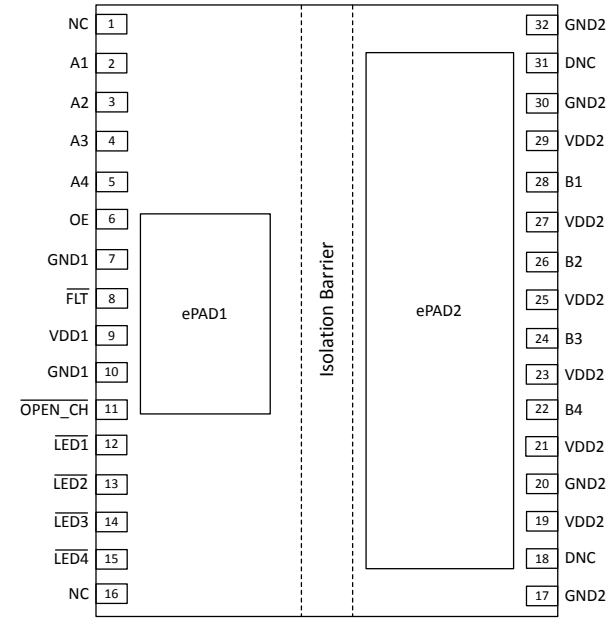
The Si834x consists of multiple die in a package with different bond-outs for different customer needs. Each bond-out is represented by a pin-out below. The Ordering Guide describes the part number and features for these products.



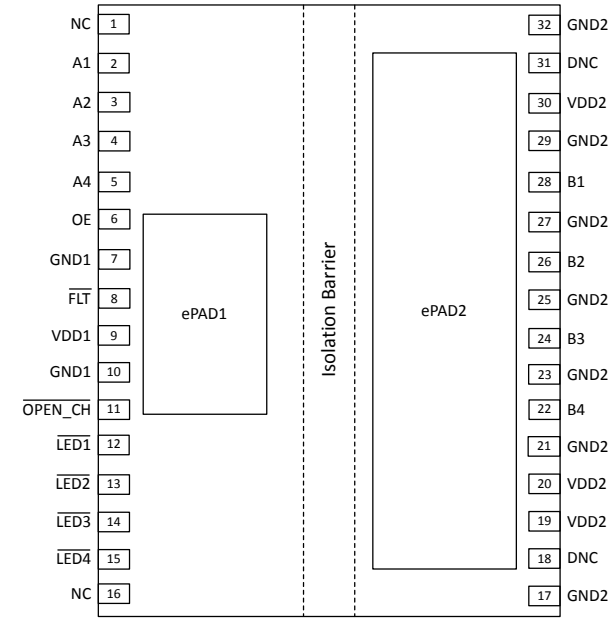
Si83404xAA-IF



Si83414xAA-IF



Si83404xBA-IF



Si83414xBA-IF

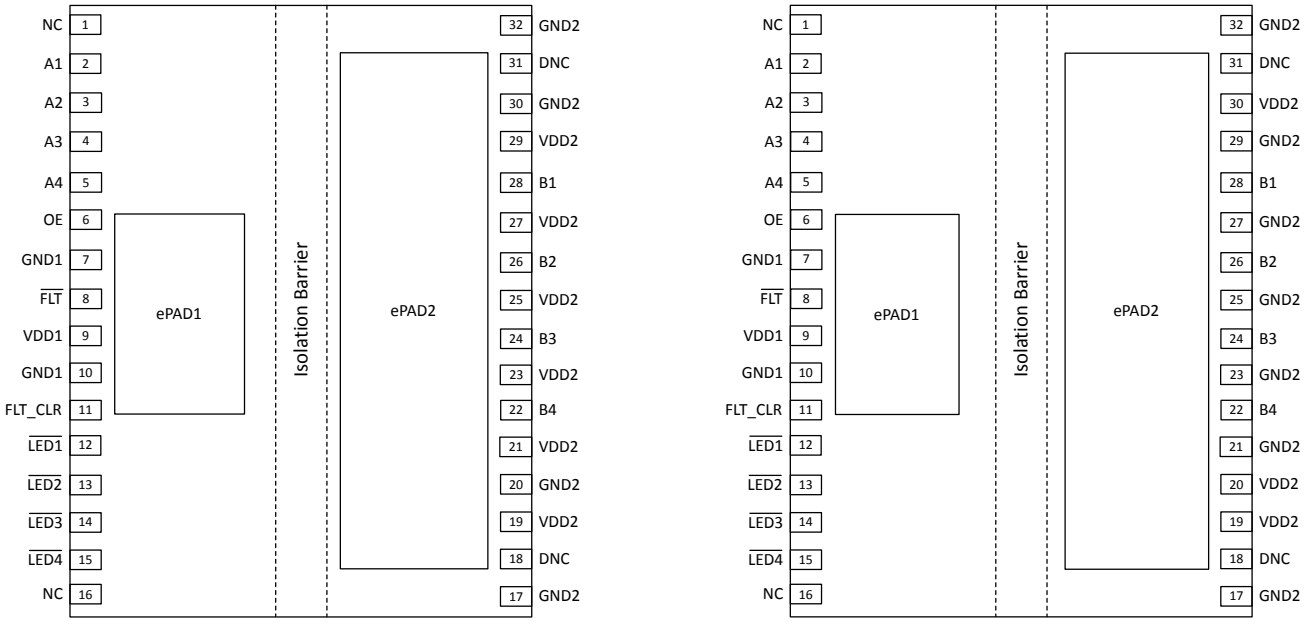


Figure 6.1. 4-Channel Parallel Interface Devices

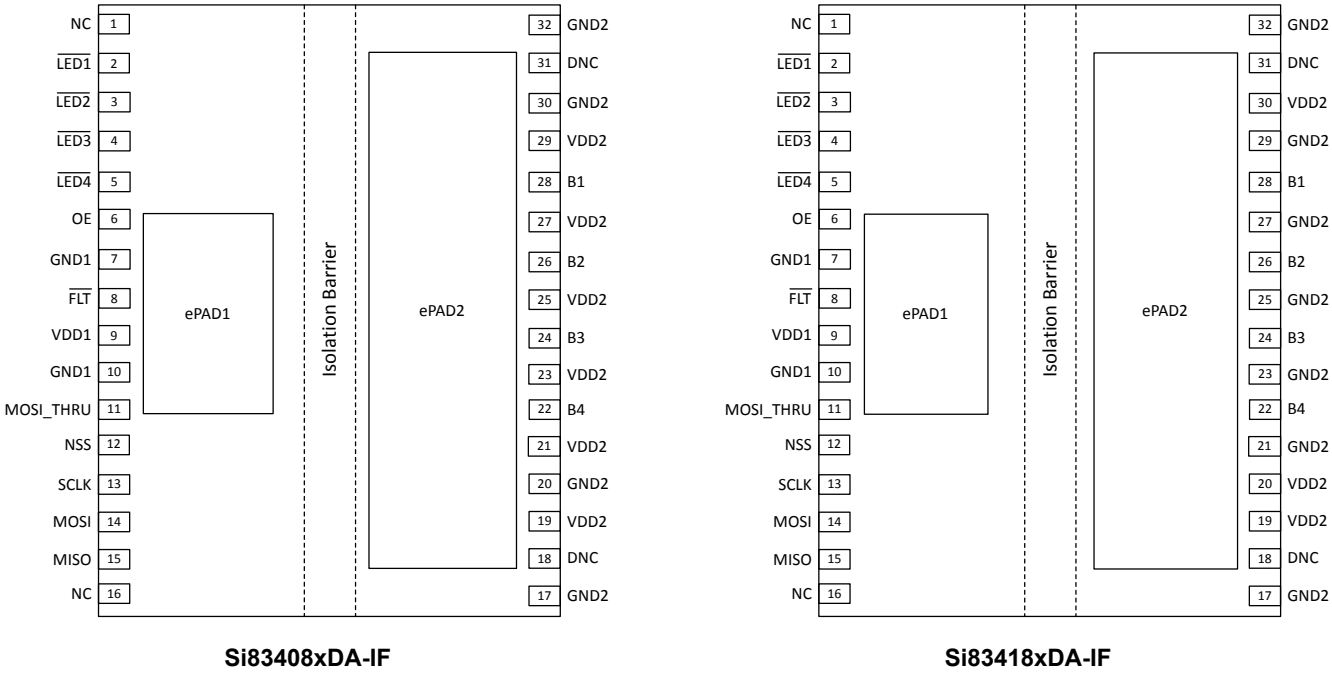


Figure 6.2. 4-Channel SPI Devices

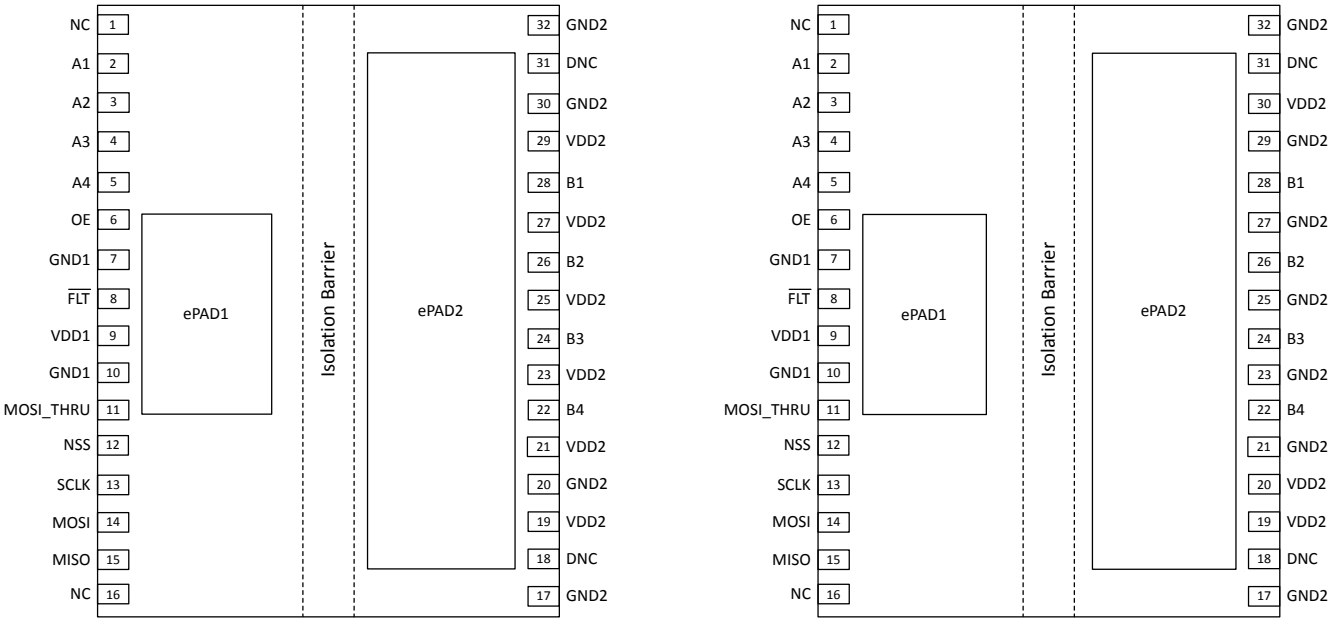


Figure 6.3. 4-Channel Parallel/SPI Devices

Table 6.1. Si834x Pin Descriptions

Pin Name	Type	Description
A1 – A4	Input	Input channels
B1 – B4	Sourcing/Sinking Output	Output channels
OE	Input	Output enable, active-high
FLT\	Open-drain Output	Active-low output that indicates diagnostic reports
LED1\ – LED4\	Open-drain Output	B1 – B4 output status indicators. Shows ON or OFF state of output
FLT_CLR	Input	Input to manually clear faults that are not cleared automatically
VDD2_WRN\	Open-drain Output	Active-low output that indicates a VDD2 Low-Voltage Warning
OPEN_CH\	Open-drain Output	Active-low output that indicates an open circuit on any output channel
MOSI_THRU	Push-pull Output	SPI data out for cascading multiple Si834x devices together
NSS	Input	SPI chip select
SCLK	Input	SPI clock
MOSI	Input	SPI input
MISO	Push-pull Output	SPI output
GND1	Ground	Isolated logic interface ground
GND2	Ground	Isolated switch ground. All GND2 pins must be used and tied together
VDD1	Supply	Isolated logic interface power supply
VDD2	Supply	Isolated switch power supply. All VDD2 pins must be used and tied together
NC	Other	Not connected. Pin is not used and should be tied to GND1
DNC	Other	Do not connect. Pin must be left floating
RSVD	Other	Reserved without specific function. Pin must be tied to GND1
ePAD1	Ground	Exposed thermal pad for logic interface. Pad must be tied to GND1
ePAD2	Ground	Exposed thermal pad for switches. Pad must be tied to GND2

6.2 Package Drawing

32-Pin 9x9 DFN (DFN-32)

The figure below illustrates the package details for the Si834x in a 32-pin 9x9 DFN package. The table below lists the values for the dimensions shown in the illustration.

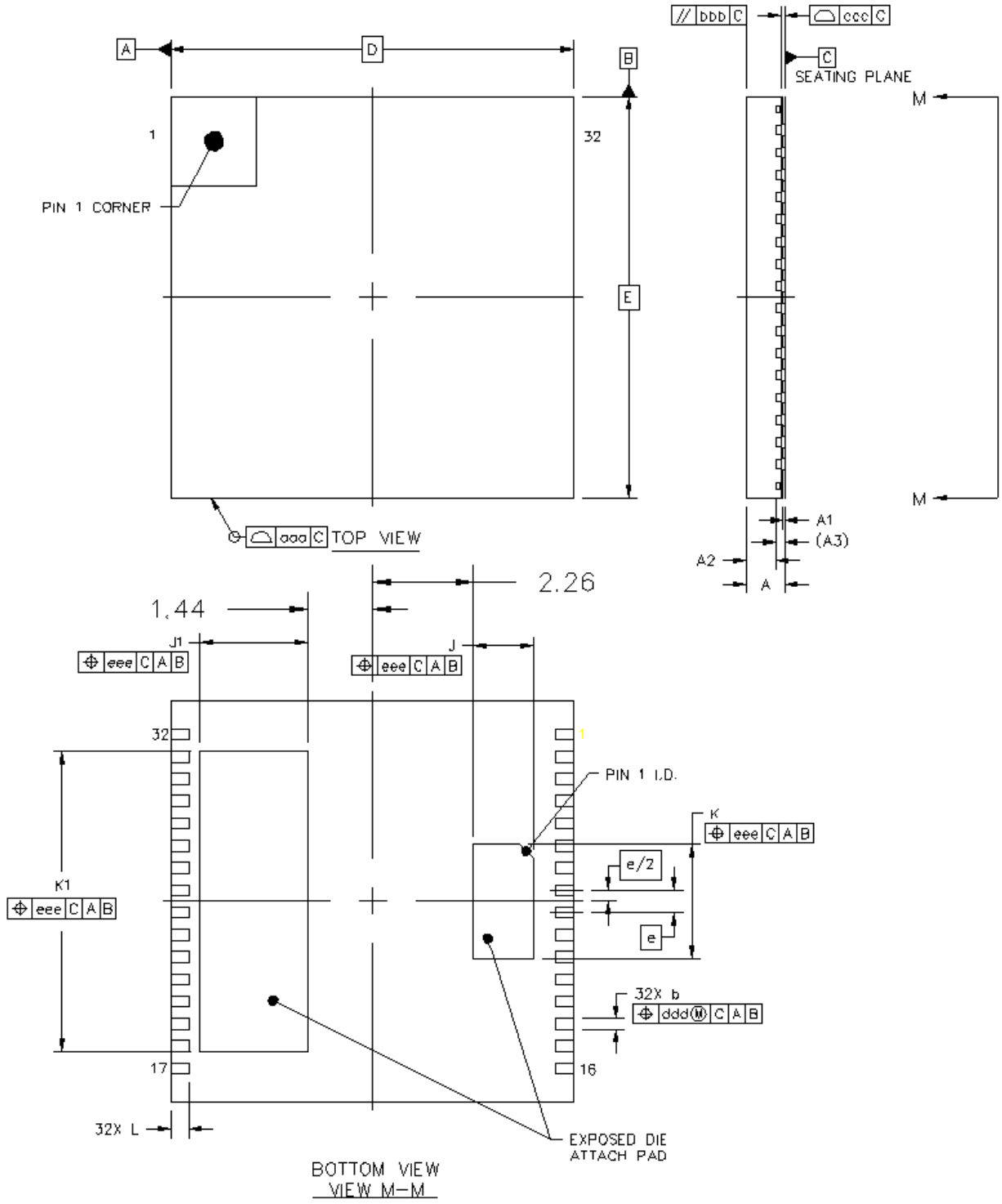


Table 6.2. 32-Pin 9x9 DFN Package Diagram Dimensions[1, 2, 3, 4]

Dimension	MIN	MAX
A	0.8	0.90
A1	0	0.05
A2	0.65 REF	
A3	0.203 REF	
b	0.2	0.30
D	9 BSC	
E	9 BSC	
e	0.50 BSC	
J	1.23	1.43
J1	2.31	2.51
K	2.45	2.65
K1	6.65	6.85
L	0.35	0.45
aaa	0.10	
bbb	0.10	
ccc	0.08	
ddd	0.10	
eee	0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.3 Land Pattern

32-Pin 9x9 DFN (DFN-32)

The figure below illustrates the recommended land pattern details for the Si834x in a 32-pin 9x9 DFN package. The table below lists the values for the dimensions shown in the illustration.

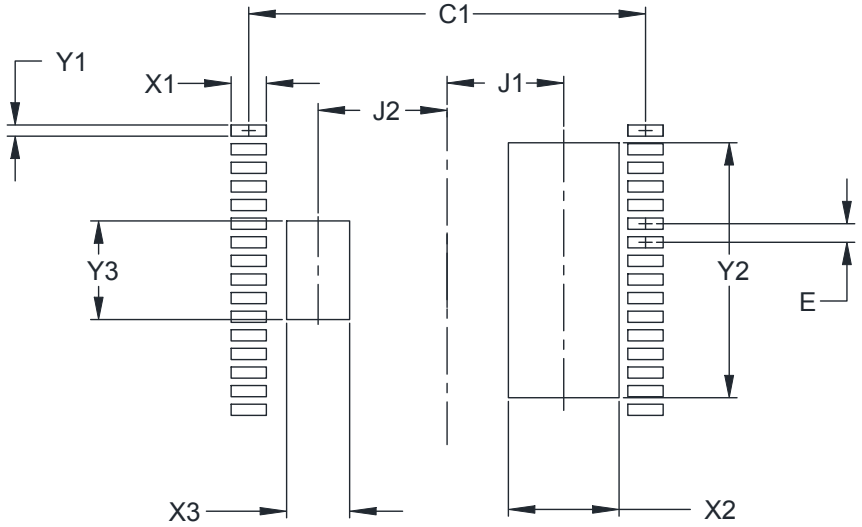


Table 6.3. PCB Land Pattern

Dimension	mm
C1	9.00
J1	2.64
J2	2.92
E	0.50
X1	0.30
Y1	0.80
X2	2.51
Y2	6.85
X3	1.43
Y3	2.65

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60mm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. An array of square openings with approximately 50% coverage may be used for each of the center ground pads (ePAD1 and ePAD2).
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4 Top Marking

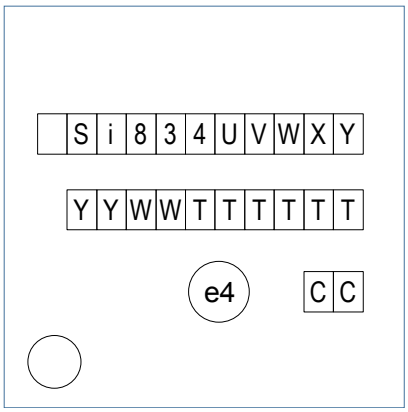


Table 6.4. 32-Pin 9x9 DFN Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information)	Si834 = Isolated Smart Switch series U = Switch Type 0 = Sourcing output (high-side) 1 = Sinking output (low-side) V = Input & Output Configuration 4 = 4 channel output, parallel input only 8 = 4 channel output, SPI programmable W = Switch Protection Configuration A = All protection methods enabled, default configuration X = Indicator Configuration A = LEDn\ indicators, FLT\ indicator, VDD2_WRN\ indicator B = LEDn\ indicators, FLT\ indicator, OPEN_CH\ indicator C = LEDn\ indicators, FLT\ indicator, FLT_CLR input D = LEDn\ indicators, FLT\ indicator F = FLT\ indicator Y = Isolation Rating A = 1.5 kVRMS
Line 2 Marking	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing code from the Assembly Purchase Order form
Line 3 Marking	CC = Country of Origin ISO Code Abbreviation	TW = Taiwan

7. Revision History

7.1 Revision 0.5

August 28, 2019

- Initial release.

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