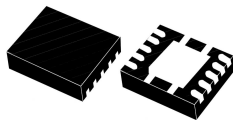


3.3 V RS485 compatible with 1.8 V I/Os and selectable speed 20 Mbps or 250 kbps



DFN10 3 x 3

Product status link

[STR485](#)

Features

- Half-duplex RS485 transceiver
- 1.65 V to 3.6 V supply for data and enable signals
- 3 V to 3.6 V supply for bus supply
- High speed: up to 20 Mbps data rate
- Low speed selected by SLR pin : 250 kbps
- Up to 256 transceivers on the bus
- Fail safe receiver (bus open, idle and shorted)
- Thermal shutdown protection
- Low quiescent current in shutdown mode
- Extended temperature range : -40 °C to +105 °C
- Available in industry standard DFN10
- Bus-pin protection more than:
 - ±4 kV HBM protection
 - ±8 kV IEC61000-4-2 contact discharge
 - ±16 kV IEC61000-4-2 air discharge
 - Compliant IEC61000-4-4 fast transient burst Class B

Description

The **STR485** is a low power differential line transceiver for data transmission standard RS485 applications in half-duplex mode. Data and enable signals are compatible with 1.8 V or 3.3 V supplies.

Two speeds are selectable through SLR pin: fast data rate up to 20 Mbps or slow data rate for extended cable running to 250 kbps.

Excessive power dissipation caused by bus contention or faults is prevented by thermal shutdown circuit that forces the driver outputs into a high impedance state. The receiver has a fail-safe feature, which guarantees a high output state when the inputs are left open, shorted or idle.

1 Pin connections

Figure 1. Pin connections

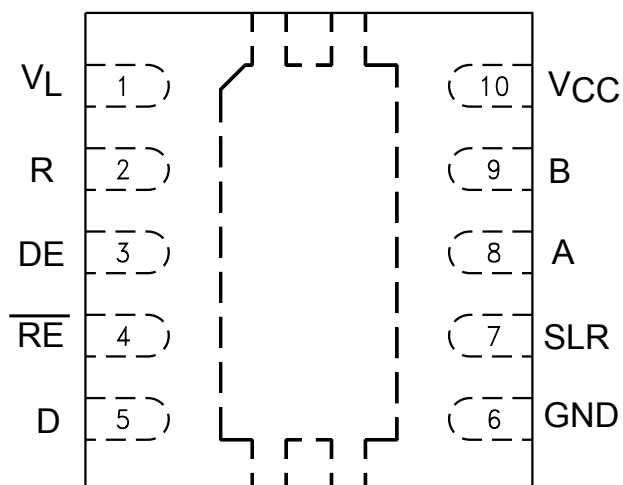
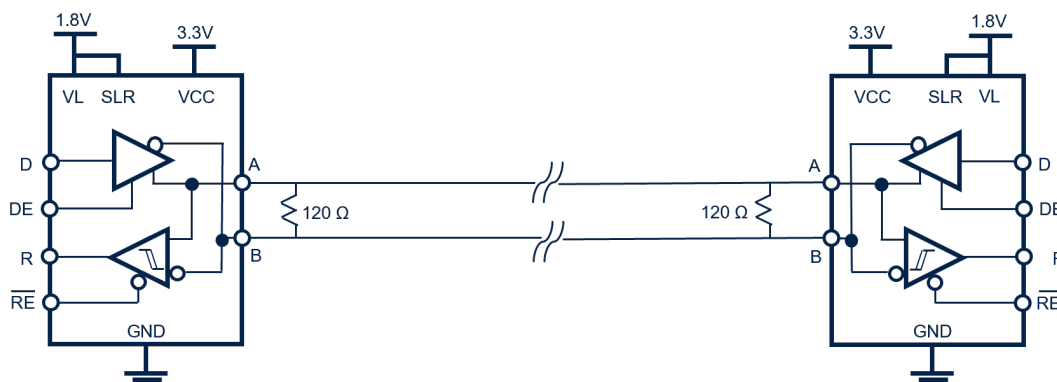
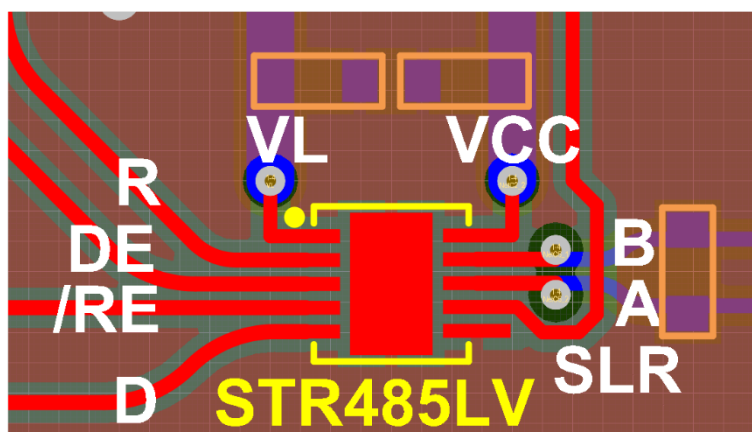


Table 1. Pin description

Name	Pin	I/O	Description
VL	1	Logic supply	1.65 V to 3.6 V supply for logic I/O signals
R	2	Digital output	Receiver data output
DE	3	Digital input	Driver enable input: serial resistors of 150 ohms followed by 2.5 Mohms/GND
nRE	4	Digital input	Receiver enable input: serial resistors of 150 ohms followed by 2.5 Mohms/VCC
D	5	Digital input	Transmission data input
GND	6	Ground	
SLR	7	Digital input	Slew rate select: low = 20 Mbps, high = 250 kbps. Default to 20 Mbps if SLR is left floating
A	8	Bus I/O	Digital bus I/O, A
B	9	Bus I/O	Digital bus I/O, B
VCC	10	Bus supply	3 V to 3.6 V supply for A and B bus lines

Figure 2. Typical application schematic

Figure 3. Example of implementation in a PCB


Adding an ESDA14V2BP6 or ETP01-2821 STMicroelectronics protection device can help the product to sustain an EFT perturbation level up to 4 kV.

2 Truth tables

The STR485 is a half-duplex differential driver/receiver compliant to the RS485 communication standard (ISO-IEC 8482). This product is perfectly adapted for low voltage application running with a low power supplies VL, generally set to 1.8 V and VCC set to 3.3 V.

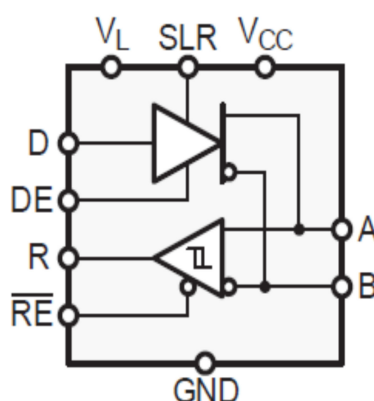
These voltages confer a low power consumption to the product.

SLR is the data rate selection, this pin could be let floating but it is not recommended; in that case the high speed rate is automatically selected.

The SLR pin must be connected to the ground to provide a high speed communication up to 20 Mbps.

When this pin is connected to VL power supply, the data rate is limited to 250 kbps more adapted for very long distance data transmission.

Figure 4. Block diagram



The product is perfectly adapted to run with 256 devices on the same bus thanks to the internal output resistance that is over 96 kΩ up to 105 °C; this resistance follows the RS485 condition that requests a minimum of 12 kΩ for 32 unit loads (UL).

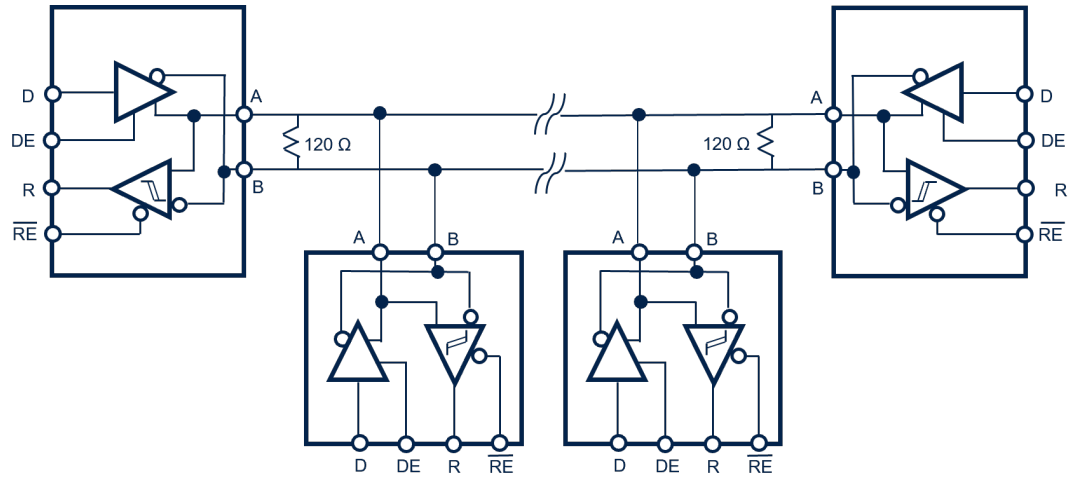
The STR485 has internal protection against ESD that protect each device driver output and receiver input. The limits have been tested up to ±4 kV electrostatic discharge (HBM) and ± 8 kV contact discharge and ± 16 kV air discharge shocks without latch-up.

Another external protection can be used to increase the communication robustness against different perturbations that can be seen on the application.

The power supplies must be well-decoupled by a minimal capacitor of 0.1 μF as close as possible to the device power supply input. Moreover, the capacitor should be higher on the application with a minimum of 1 μF around the device.

The device operating range is set from VL = 1.65 V to 3.6 V and for VCC = 3.0 V to 3.6 V. In any case VCC must be higher or equal than VL.

The applications should respect this voltage constraints to let the application communication device run to the best conditions.

Figure 5. Example of typical application

Table 2. Driver truth table

INPUT D	ENABLE DE	OUTPUT A	OUTPUT B	Function
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

Table 3. Receiver truth table

Differential input $V_{ID} = V_A - V_B$	ENABLE RE	OUTPUT R	Function
$V_{ID} > V_{IT+}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail safe high output
Short-circuit bus	L	H	Fail safe high output
Idle (terminated) bus	L	H	Fail safe high output

Table 4. Speed selection, SLR pin configuration

SLR	Data rate	Typical t_r / t_f
VL	250 kbps	200 ns
GND or OPEN	20 Mbps	7 ns

3 Absolute maximum ratings and operating conditions

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_L	Control supply voltage	-0.5	4	V
V_{CC}	Bus supply voltage	-0.5	4.8	V
	Voltage range at A or B inputs	-13	13	V
	Input voltage range at any logic pin	-0.3	$V_L+0.3$	V
	Receiver output current	-12	12	mA
T_J	Junction temperature		170	°C
T_{stg}	Storage temperature	-65	150	°C
ESD	IEC 61000-4-2 ESD (air-gap discharge), bus terminals and GND		± 16	kV
	IEC 61000-4-2 ESD (contact discharge), bus terminals and GN		± 8	kV
	IEC 61000-4-4 EFT (fast transient or burst) bus terminals and GND		± 2	kV
	JEDEC standard 22, test method A114, HBM, all terminals		± 4	kV
	JEDEC standard 22, test method C101, (charged device model), all pins		± 1.5	kV

Note: All voltage values, except the differential voltage, are with respect to network ground terminal.

Table 6. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_L	Control supply voltage	1.65		3.6	V
V_{CC}	Bus supply voltage	3	3.3	3.6	
V_I	Input level at any bus terminal (separately or common mode)	-7		12	
V_{IH}	High level input voltage (driver, driver enabled, receiver enable inputs, and slew rate select)	$0.7 \times V_L$		V_L	
V_{IL}	Low level input voltage (driver, driver enable, receiver enable inputs, and slew rate select)	0		$0.3 \times V_L$	
V_{ID}	Differential input voltage	-12		12	mA
IO	Output current / driver	-80		80	
	Output current / receiver	- 2		2	
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
D_R	Signaling rate / SLR = '0'			20	Mbps
	Signaling rate / SLR = '1'			250	kbps
T_A	Operating free-air temperature	-40		105	°C

Operation is specified for internal (junction temperature) up to 150 °C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down circuit which disables the driver outputs when the junction temperature reaches 165 °C.

Table 7. Thermal information

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{th-ja}	Thermal resistance, junction-to-ambient		40		°C/W
R_{th-jc}	Thermal resistance, junction-to-case		5.2		

4 Electrical characteristics

Table 8. Receiver: over recommended operating conditions (unless otherwise specified. Please, see "Operating conditions" table)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Receiver/DC						
V _{IT+}	Positive-going receiver differential input voltage threshold		(1)	-60	-20	mV
V _{IT-}	Negative-going receiver differential input voltage threshold		-200	-130	(1)	
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-}) ⁽¹⁾		40	70		
V _{OH}	Receiver high-level output voltage	V _L = 1.65 V, I _{OH} = - 2 mA	1.25	1.45		V
		V _L = 3 V, I _{OH} = - 2 mA	2.75	2.9		
V _{OL}	Receiver low-level output voltage	V _L = 1.65 V, I _{OL} = 2 mA		0.2	0.45	
		V _L = 3 V, I _{OL} = 2 mA		0.1	0.25	
C _{OD}	Differential output capacitance			15		pF
I _{OZ}	Receiver output high-impedance current	V _O = 0 V or V _L , nRE at V _L	-1		1	μA
R _{in}	Receiver input impedance	-7 V ≤ V _{inCM} ≤ +12 V -40 °C ≤ Temp ≤ 105 °C	96 ⁽²⁾			kΩ
I _I	Receiver input current (disabled driver)	1V65 < V _L < 3.3 V, V _{CC} = 3.3 V		85 ⁽²⁾		μA
		V _I = 12 V, -40 °C ≤ Temp ≤ 105 °			125 ⁽²⁾	
		V _I = -7 V, -40 °C ≤ Temp ≤ 105 °	-100 ⁽²⁾			
Receiver / switching characteristics, SLR = 'X'						
t _r , t _f	Receiver output rise/fall time	C _L =15 pF		5	15	ns
t _{PHL} , t _{PLH}	Receiver propagation delay time		15	25	60	
t _{SK(P)}	Receiver pulse skew, t _{PHL} – t _{PLH}				15	
t _{PLZ} , t _{PHZ}	Receiver disable time			12	20	
t _{PLZ} , t _{PZH} , t _{PZL} , t _{PZH}	Receiver enable time	Driver enabled C _L =15 pF with 1 kΩ		15	80	μs
		Driver disabled C _L =15 pF with 1 kΩ		2	8	

1. Under any specific conditions, V_{IT+} , is specified to be at least V_{HYS} higher than V_{IT-} .
2. Guaranteed by design simulation in temperature.

Table 9. Driver: over recommended operating conditions (unless otherwise specified. Please, see "Operating conditions" table)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC driver/ DC						
I _I	Driver input, driver enable, and receiver enable input current		-2		2	μA
V _{OD}	Driver differential output voltage magnitude	R _L = 60 Ω, 375 Ω on each output to −7 V to 12	1.5	2		V
		R _L = 54 Ω (RS-485)	1.5	2		
		R _L = 100 Ω (RS-422) T _J ≥ 0 °C, V _{CC} ≥ 3.2	2			
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω, C _L = 50 pF	-50	0	50	mV
V [°] C(SS)	Steady-state common-mode output voltage	Center of two 27-Ω load resistors	1	V _{CC} /2	3	V
ΔV [°] C	Change in differential driver output common-mode voltage		-50	0	50	mV
V [°] C(PP)	Peak-to-peak driver common-mode output voltage			500		
Driver/switching characteristics, SLR='1', 250 kbps, bit time ≥ 4 μs						
t _r , t _f	Driver differential output rise/fall time	R _L = 54 Ω, C _L = 50 pF	0.05	0.2	1	μs
t _{PHL} , t _{PLH}	Driver propagation delay time		0.4	1	1.5	
t _{SK(P)}	Driver pulse skew, t _{PHL} – t _{PLH}				0.3	
t _{PLZ} , t _{PHZ}	Driver disable time			0.017	0.035	
t _{PLZ} , t _{PZH}	Driver enable time	Receiver enabled C _L = 50 pF with 110 Ω		0.7	1.2	μs
		Receiver disabled C _L = 50 pF with 110 Ω		1.64	2.4	
Driver/switching characteristics, SLR= '0', 20 Mbps, bit time ≥ 50 ns						
t _r , t _f	Driver differential output rise/fall time	R _L = 54 Ω, C _L = 50 pF	4	7	15	ns
t _{PHL} , t _{PLH}	Driver propagation delay		6	12	25	
t _{SK(P)}	Driver pulse skew, t _{PHL} – t _{PLH}				4	
t _{PLZ} , t _{PHZ}	Driver disable time			17	40	
t _{PZL} , t _{PZH}	Driver enable time	Receiver enabled		9	18	μs
		Receiver disabled		1	2.4	

Table 10. Supply current and protections: over recommended operating conditions (unless otherwise specified. Please, see "Operating conditions" table)

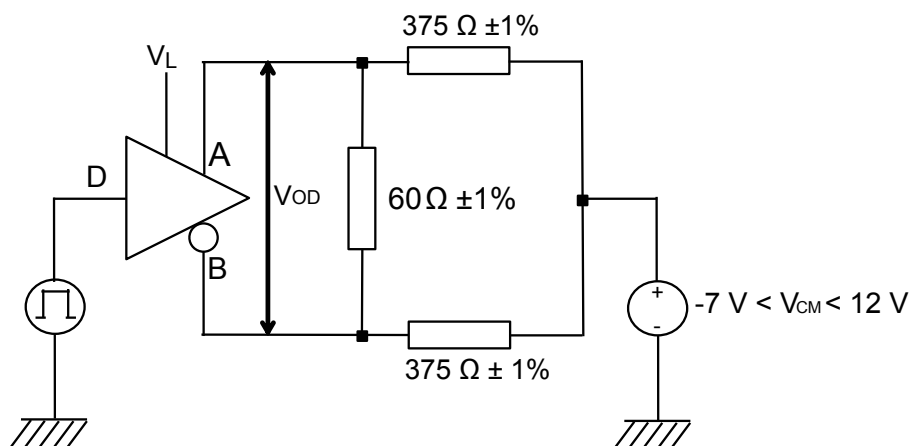
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CC}	Supply current (quiescent)	Driver and receiver enabled DE = V_L , RE = GND, no load, T_{amb}		625		μA
		Driver and receiver enabled DE = V_L , RE = GND, no load, $T < 105\text{ }^{\circ}C$			900 ⁽¹⁾	
		Driver enabled, receiver disabled DE = VCC, =VL, No load, T_{amb}		315		
		Driver enabled, receiver disabled DE = VCC, =VL, No load, $T < 105\text{ }^{\circ}C$			550 ⁽¹⁾	
		Driver disabled, receiver enabled DE = GND, =GND, No Load		515	700	
		Driver and receiver disabled DE = GND, =VL, no load [-40 °C, 105 °C]		0.5	3	
T_{TSD}	Thermal shutdown threshold			165		$^{\circ}C$
T_{TSD_HYS}	Thermal shutdown hysteresis			15		
I_{OS}	Driver short-circuit output current	-7 V < V_{SHORT} < + 12 V	-250		250	mA

1. Guaranteed by simulation.

5 Test circuits and typical characteristics

In the schematics below, C_L includes fixture and instrumentation capacitance.

Figure 6. Driver differential output voltage with common-mode load



Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 ns.

Figure 7. Driver differential and common-mode output with RS-485 load

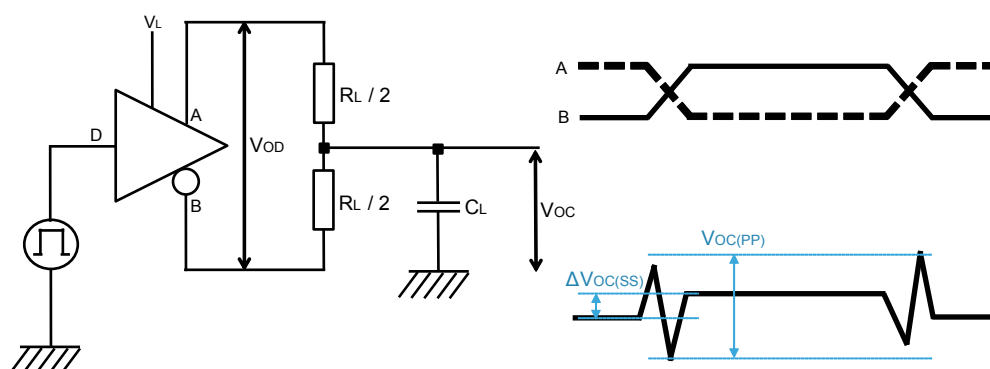


Figure 8. Driver differential output rise and fall times and propagation delays

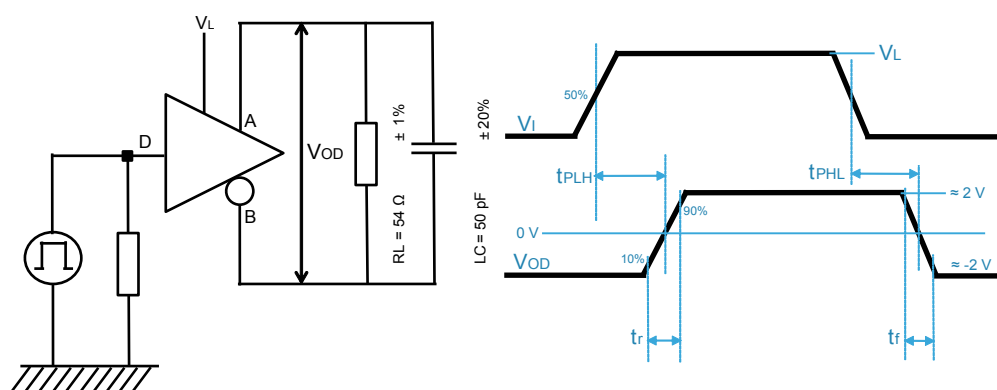


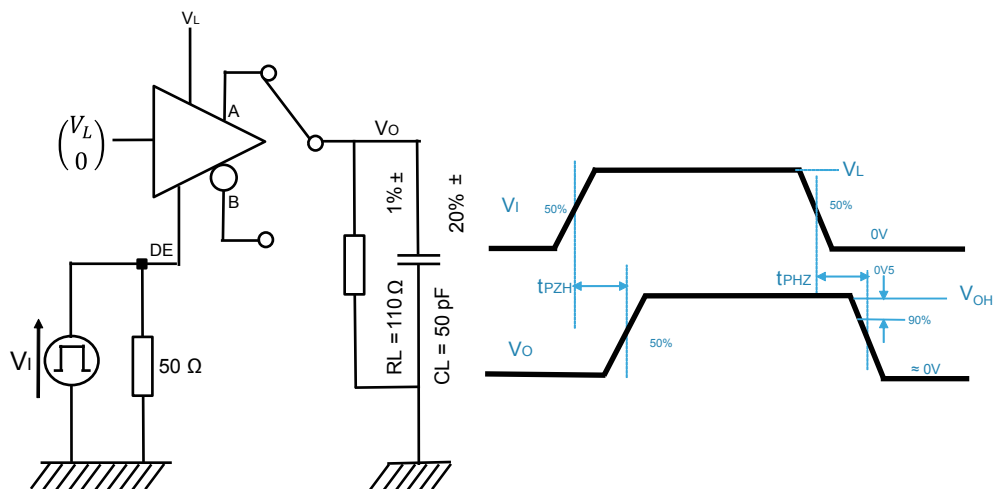
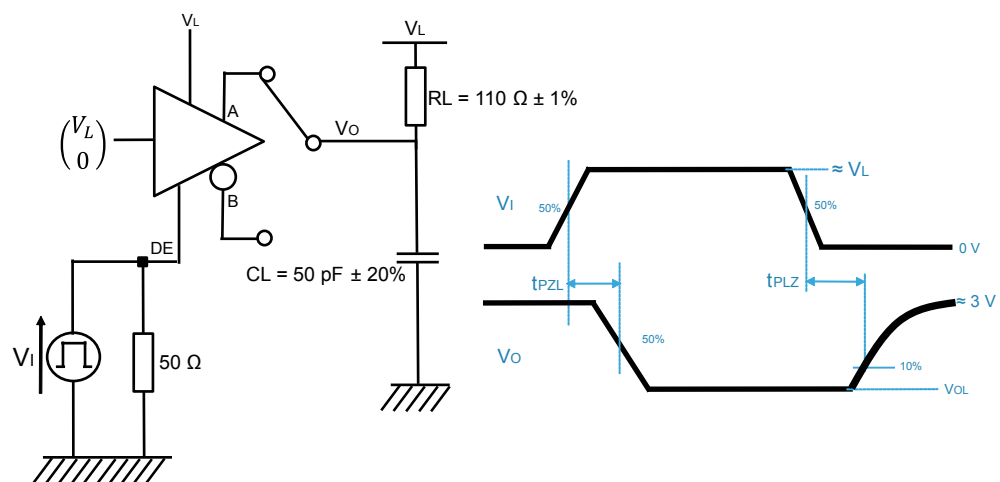
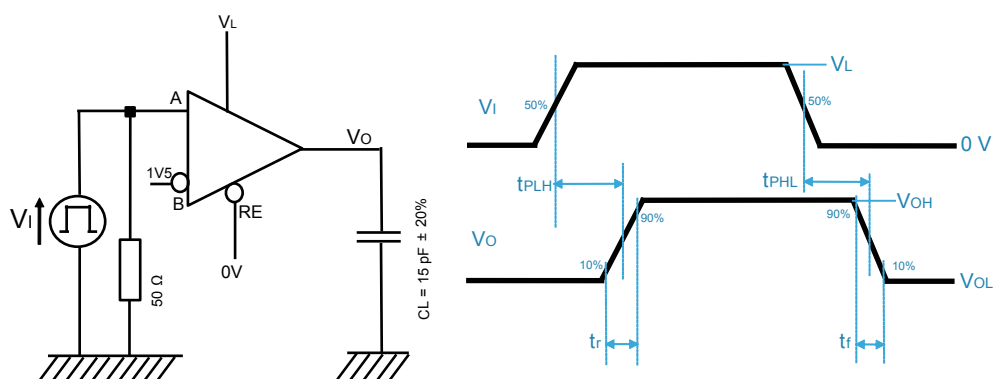
Figure 9. Driver enable and disable times with active high output and pull-down load

Figure 10. Driver enable and disable times with active low output and pull-up load

Figure 11. Receiver output rise and fall times and propagation delay


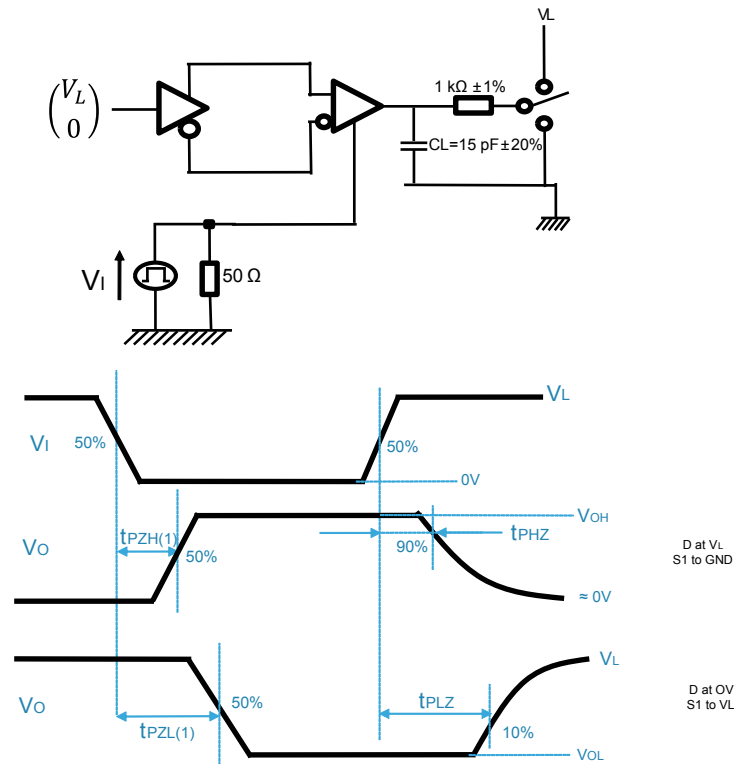
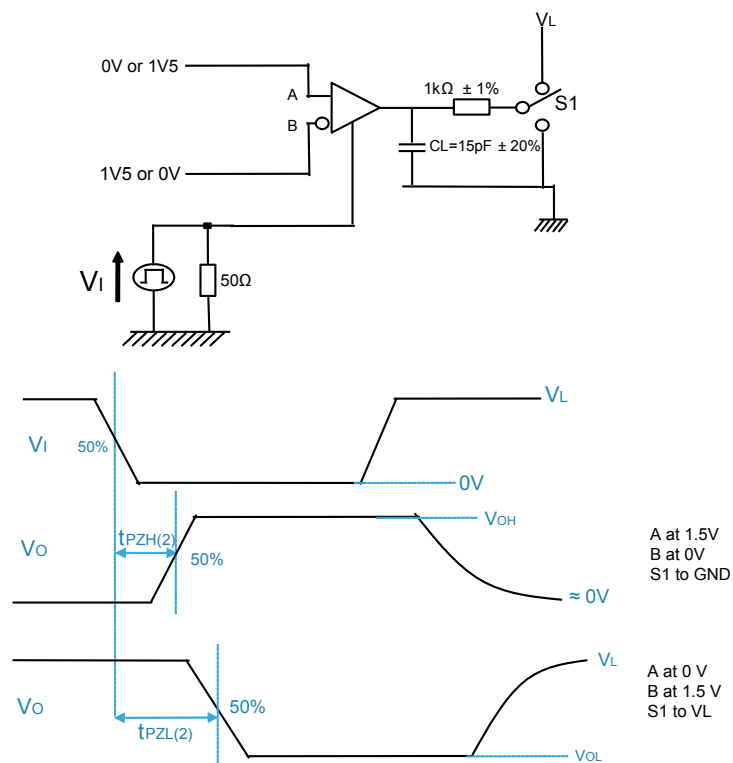
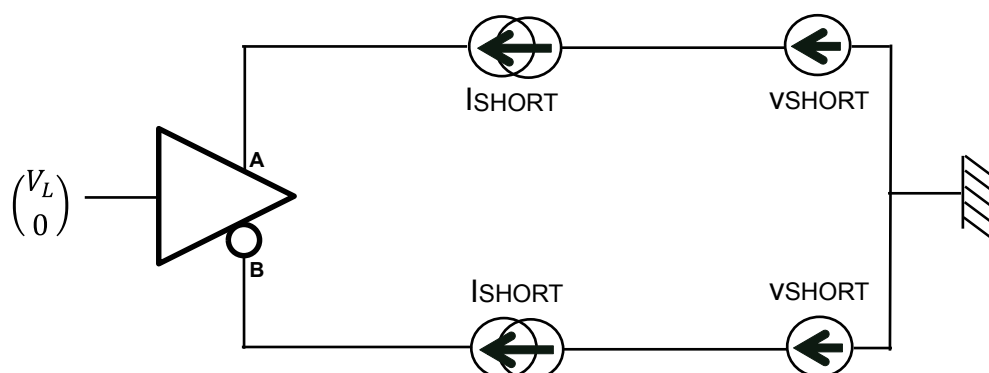
Figure 12. Receiver enable/disable times with driver enabled

Figure 13. Receiver enable/disable times with driver disabled


Figure 14. Short-circuit output current measurement



When one of the driver output is shorted to a voltage source (named VSHORT) between -7 V to +12 V stabilized, the current does not exceed 250 mA and the driver is protected.

6 Typical characteristics

Figure 15. Driver I_{CC} vs V_{CC} supply driver I_{CC} versus temperature 60 Ω load

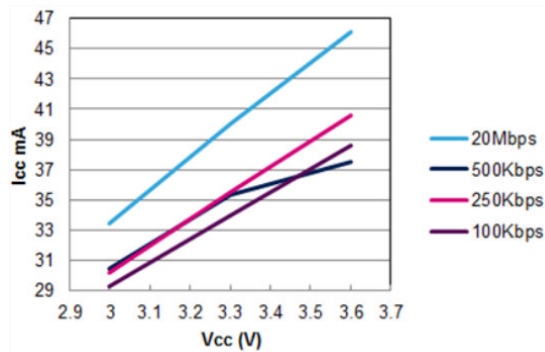


Figure 16. Driver I_{CC} vs temperature 60 Ω load

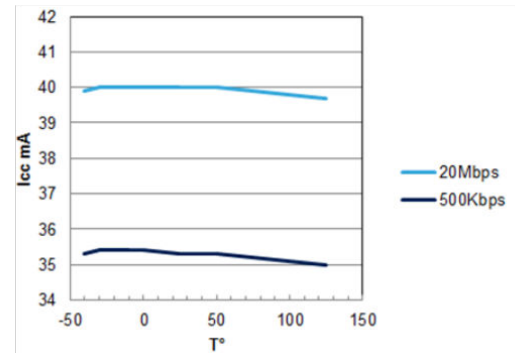


Figure 17. Driver output on 60 Ω load, clock @10 MHz 3V6pp

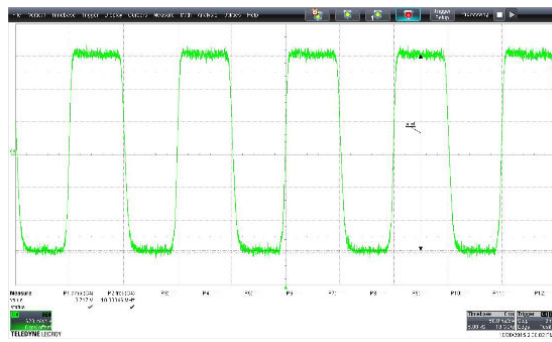


Figure 18. Driver output on 60 Ω load, speed selected @20 MHz 3V6pp

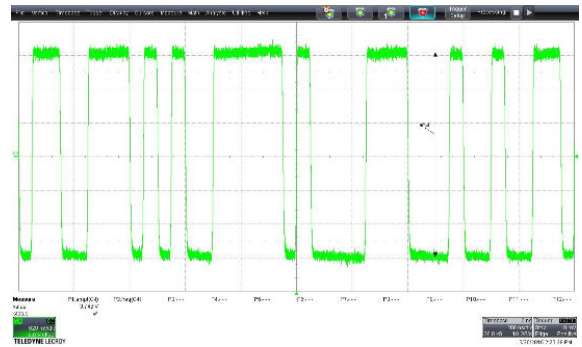
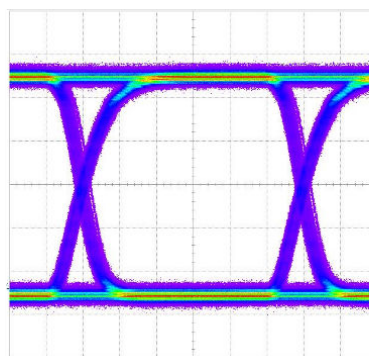


Figure 19. Eye diagram 20 Mbps short line



7 Equivalent input and output schematic diagrams

Figure 20. D and RE inputs

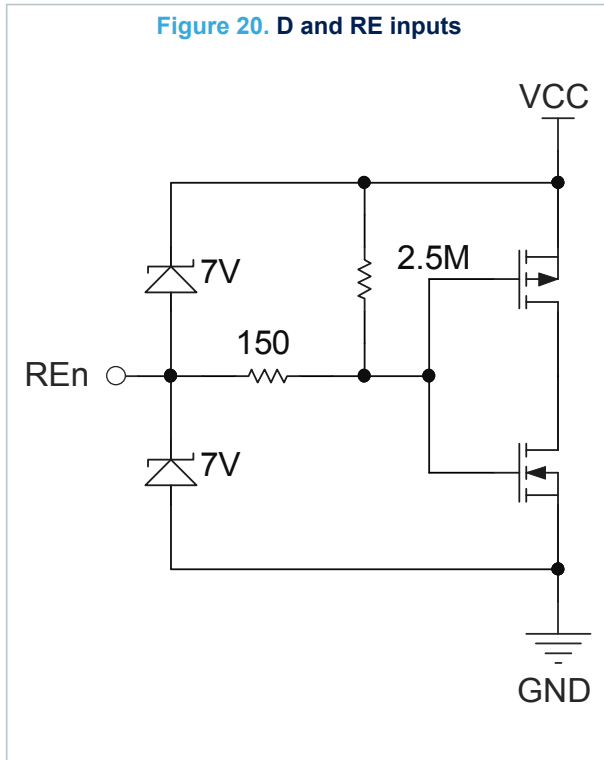


Figure 21. DE and SLR inputs

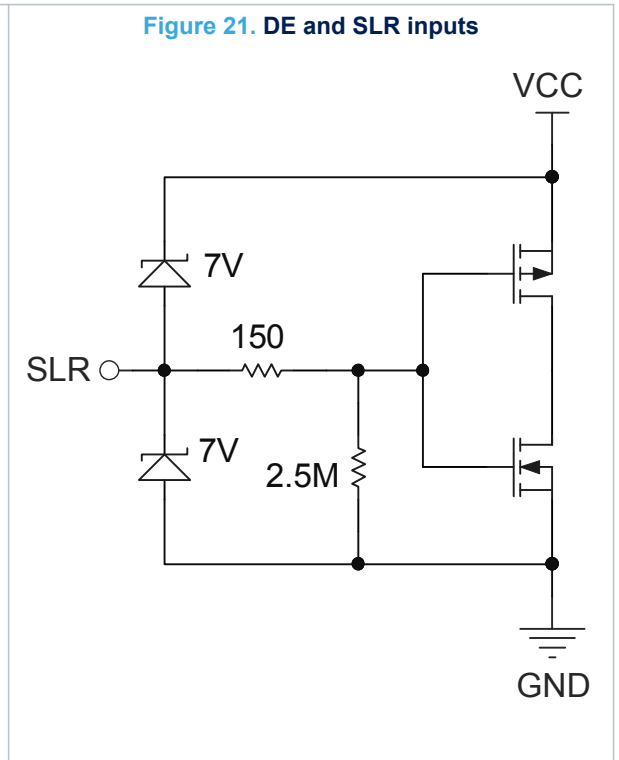


Figure 22. R output

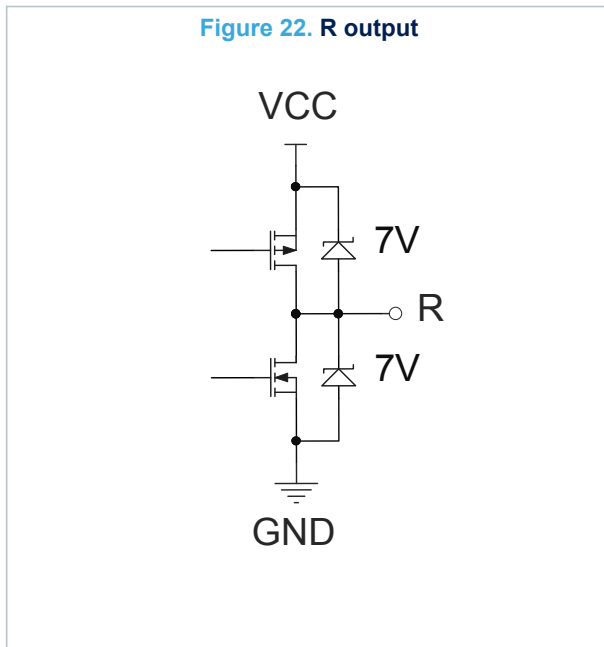


Figure 23. Driver output

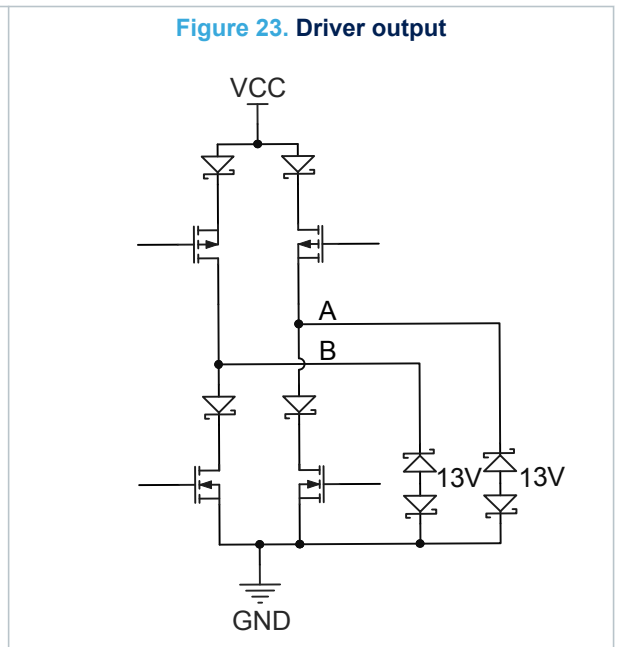
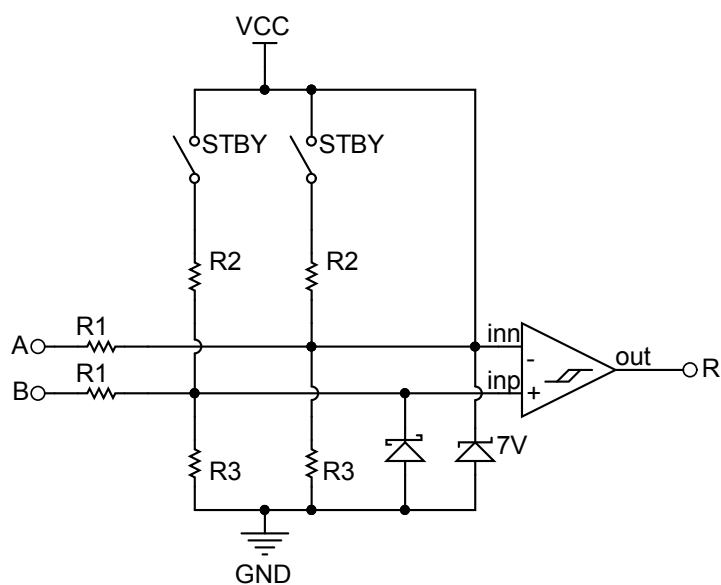


Figure 24. Receiver inputs


8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN10 package information

Figure 25. DFN10 package outline (top and side view)

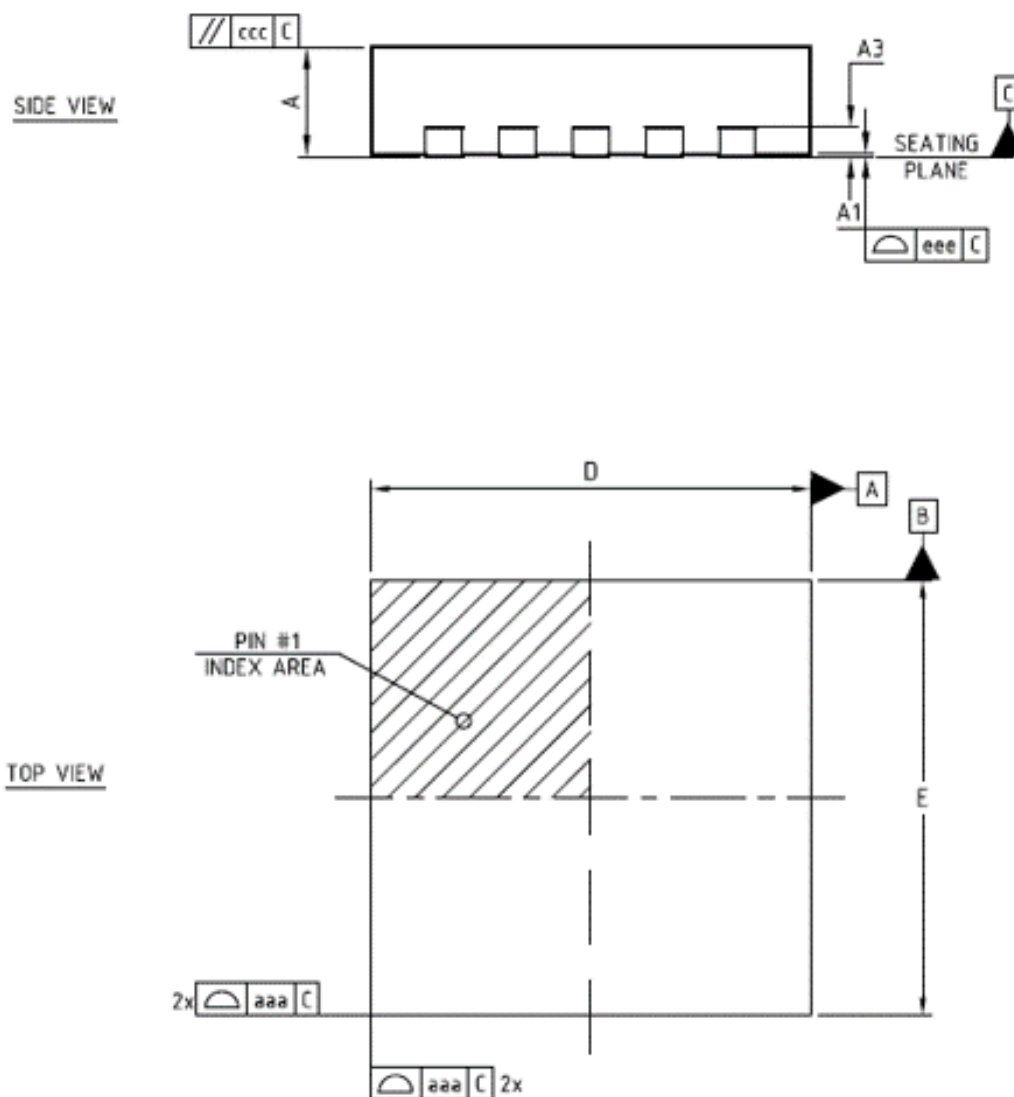
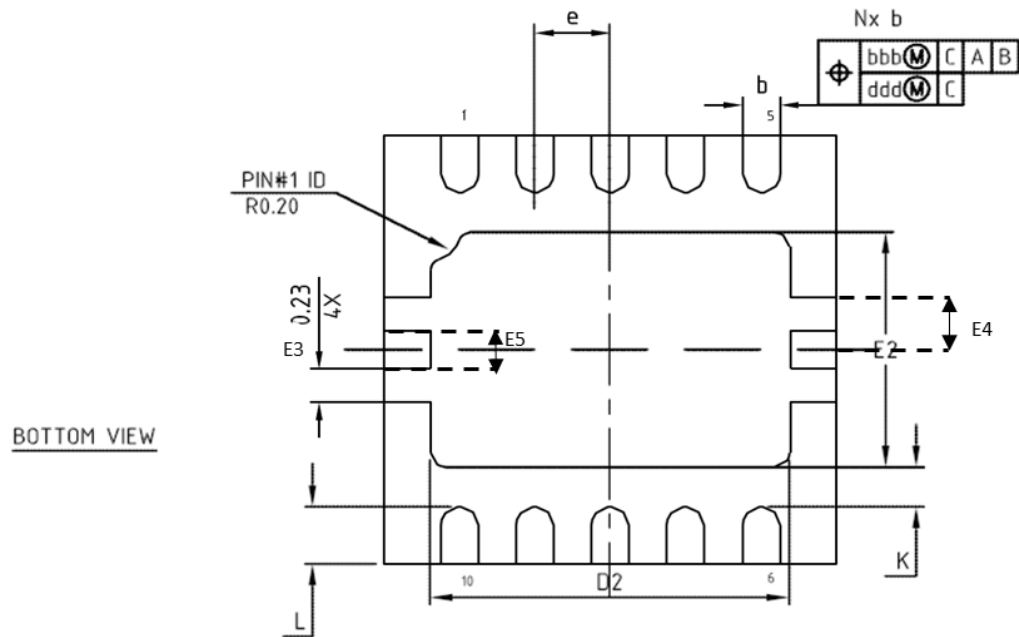
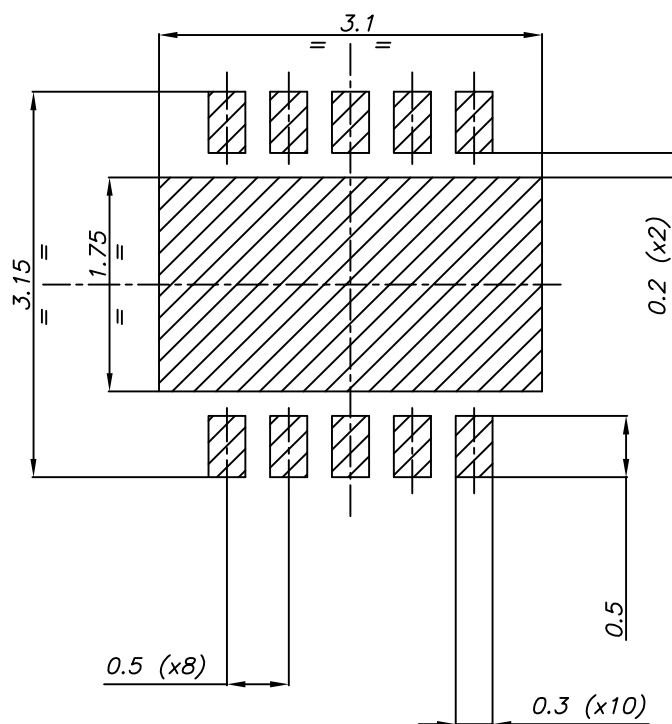


Figure 26. DFN10 package outline (bottom view)

Table 11. DFN10 package mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20		
b	0.20	0.25	0.30
D	2.85	3.00 BSC	3.15
D2	2.284	2.384	2.484
E	2.85	3.00 BSC	3.15
E2	1.546	1.646	1.746
E3	0.130	0.230	0.330
E4	0.265	0.365	0.465
E5	0.170	0.270	0.370
e	0.50 BSC		
K	0.20		
L	0.30	0.40	0.50
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Note: VFDFPN stands for thermally enhanced very thin fine pitch dual flat packages. No lead. Very thin: $0.80\text{ mm} < A \leq 1.00\text{ mm}$ / fine pitch: $e < 1.00\text{ mm}$

Figure 27. DFN10 recommended footprint



9 Ordering information

Order code	Temperature range	Package	Marking
STR485LVQT	-40 °C to +105 °C	DFN10	485L

Revision history

Table 12. Document revision history

Date	Version	Changes
20-Sep-2018	1	Initial release.
16-Oct-2018	2	Updated Table 10. Supply current and protections: over recommended operating conditions (unless otherwise specified. Please, see "Operating conditions" table).
15-Apr-2019	3	Updated Table 9. Driver: over recommended operating conditions (unless otherwise specified. Please, see "Operating conditions" table).
24-Oct-2019	4	Updated Table 1. Pin description. Updated section 7 Equivalent input and output schematic diagrams.
02-Jul-2020	5	Updated Section 8.1 DFN10 package information. Updated Section 9 Ordering information.
21-Nov-2023	6	Updated Section 7 Equivalent input and output schematic diagrams figure 20 and figure 21.
26-Jun-2026	7	Updated Figure 2 and Figure 5 .

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