

MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 67 mΩ, 40 A

NTH4L067N65S3H

Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET FAST series is very suitable for the various power systems for miniaturization and higher efficiency.

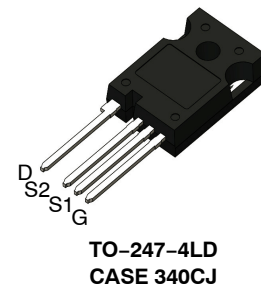
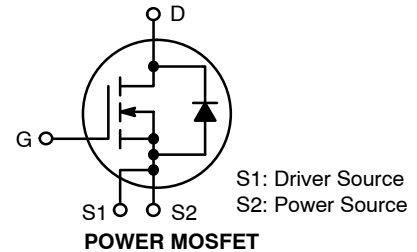
Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 55\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 80\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 691\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

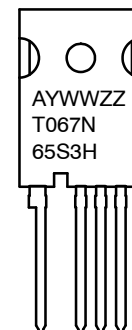
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	67 mΩ @ 10 V	40 A



MARKING DIAGRAM



A	= Assembly Site Code
YWW	= Data Code (Year & Week)
ZZ	= Assembly Lot Code
T067N65S3H	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTH4L067N65S3H

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	± 30	V
		– AC ($f > 1\text{ Hz}$)	± 30	
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$)	40	A
		– Continuous ($T_C = 100^\circ\text{C}$)	25	
I_{DM}	Drain Current	– Pulsed (Note 1)	112	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		422	mJ
I_{AS}	Avalanche Current (Note 2)		6.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.66	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	266	W
		– Derate Above 25°C	2.13	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS} = 6.5\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 20\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.47	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTH4L067N65S3H	T067N65S3H	TO-247 A04	Tube	N/A	N/A	30 Units

NTH4L067N65S3H

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	–	0.63	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	2	μA
		V _{DS} = 520 V, T _C = 125°C	–	1.6	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 3.9 mA	2.4	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 20 A	–	55	67	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 20 A	–	28	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 250 kHz	–	3750	–	pF
C _{oss}	Output Capacitance		–	60	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	691	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	107	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 20 A, V _{GS} = 10 V (Note 4)	–	80	–	nC
Q _{gs}	Gate to Source Gate Charge		–	21	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	20	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.6	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 20 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)	–	28	–	ns
t _r	Turn-On Rise Time		–	7.2	–	ns
t _{d(off)}	Turn-Off Delay Time		–	81	–	ns
t _f	Turn-Off Fall Time		–	2.6	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current		–	–	40	A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	112	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 20 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 20 A, dI _F /dt = 100 A/μs	–	411	–	ns
Q _{rr}	Reverse Recovery Charge		–	7.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

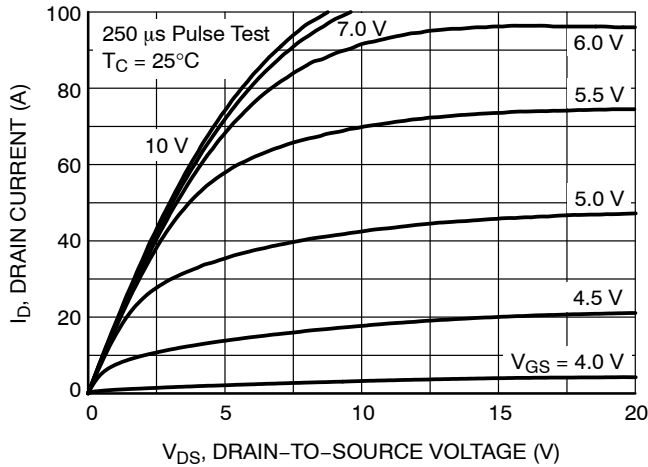


Figure 1. On-Region Characteristics

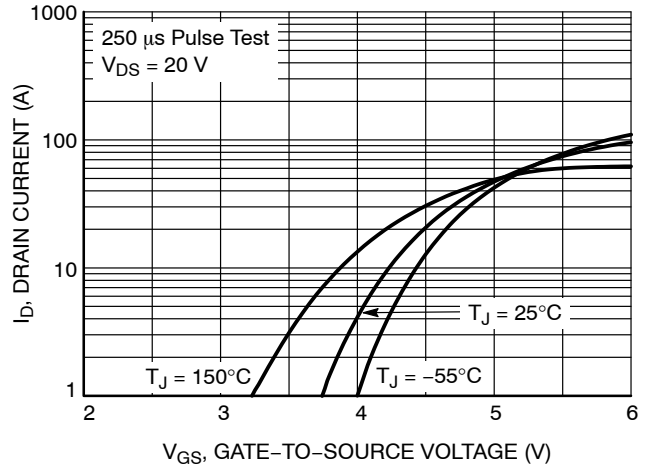


Figure 2. Transfer Characteristics

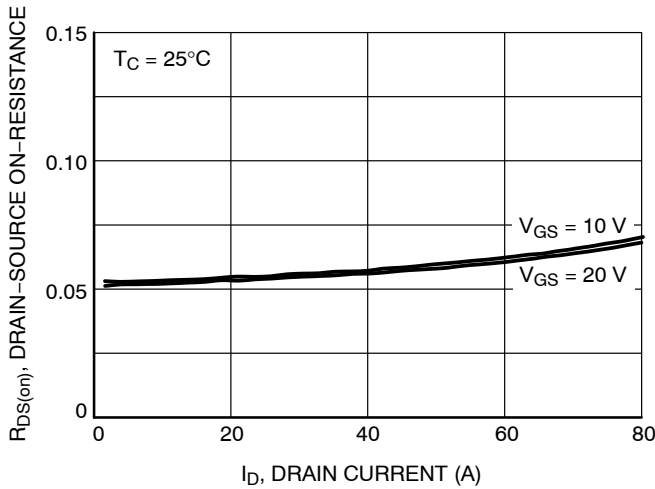


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

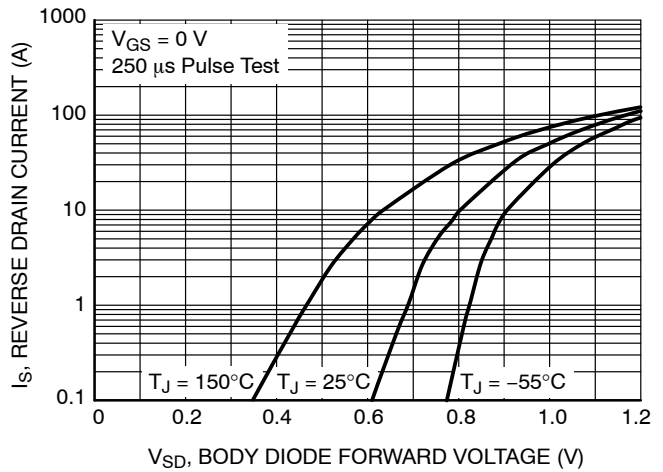


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

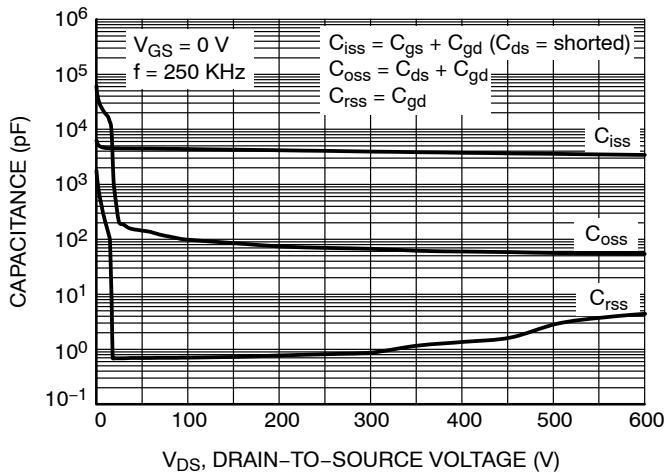


Figure 5. Capacitance Characteristics

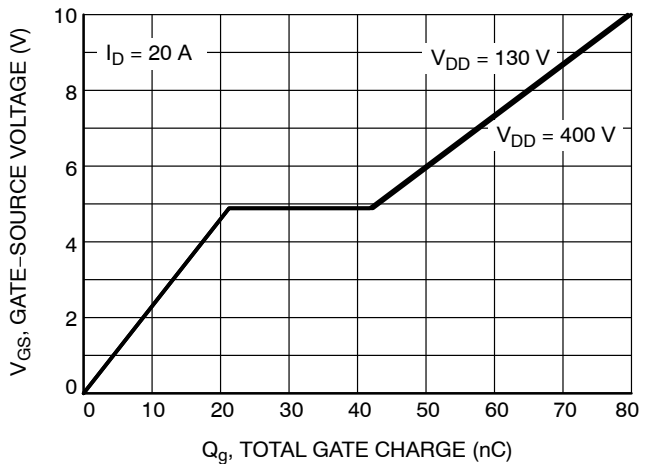


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

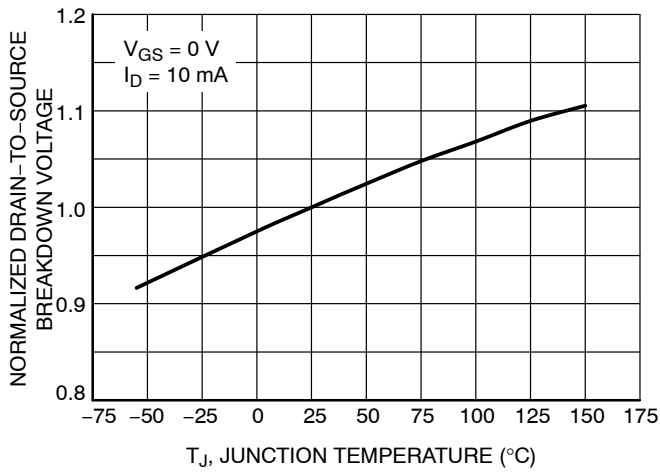


Figure 7. Breakdown Voltage Variation vs. Temperature

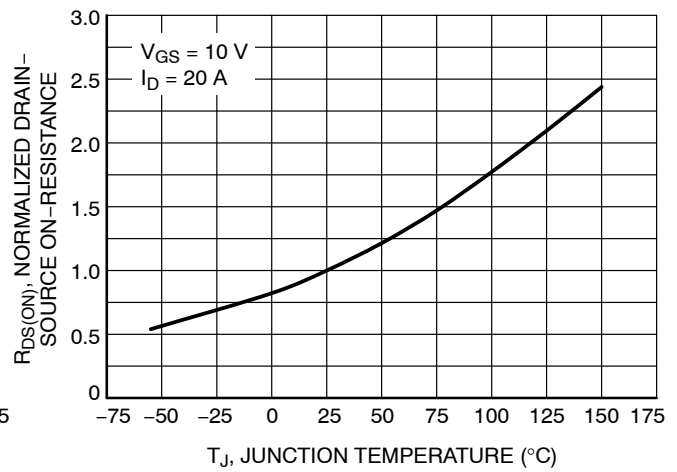


Figure 8. On-Resistance Variation vs. Temperature

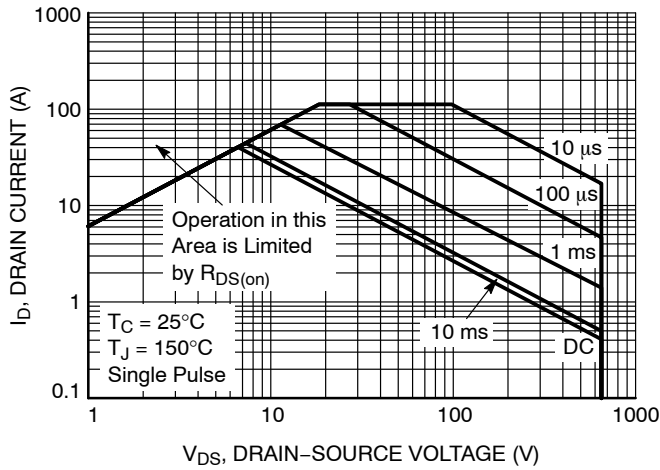


Figure 9. Maximum Safe Operating Area

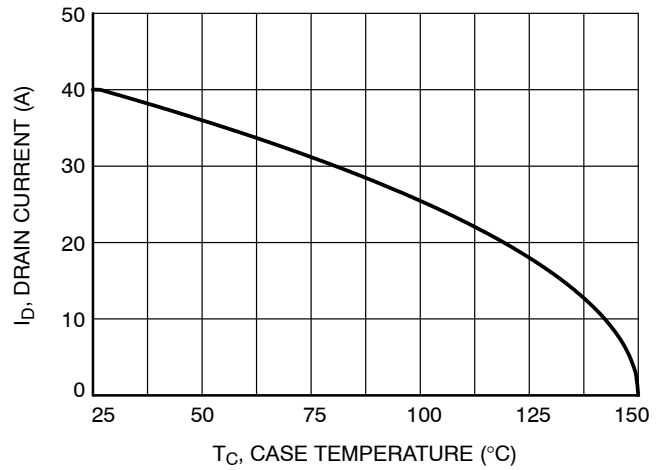


Figure 10. Maximum Drain Current vs. Case Temperature

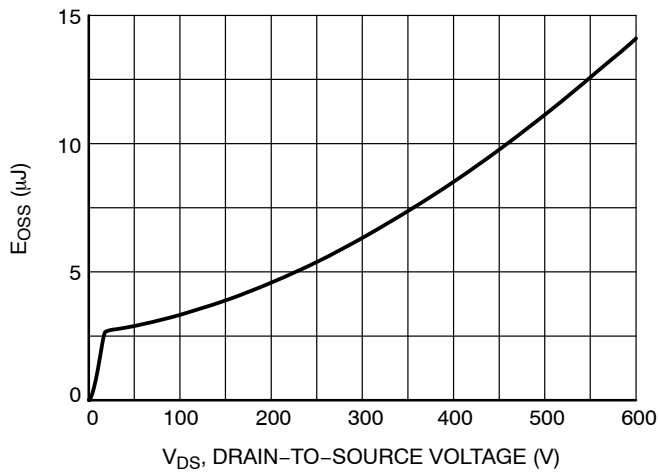


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

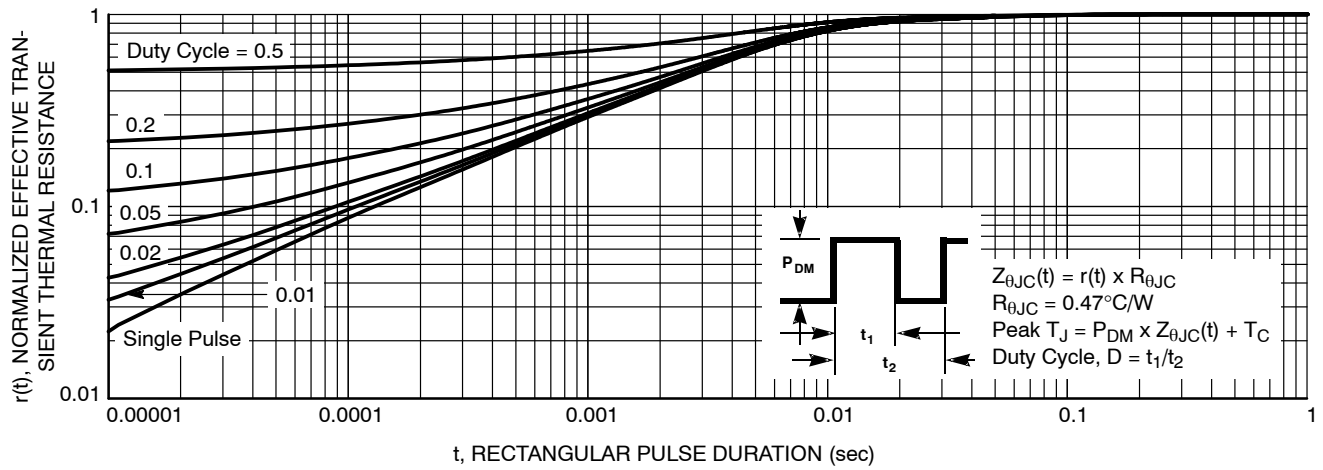


Figure 12. Transient Thermal Impedance

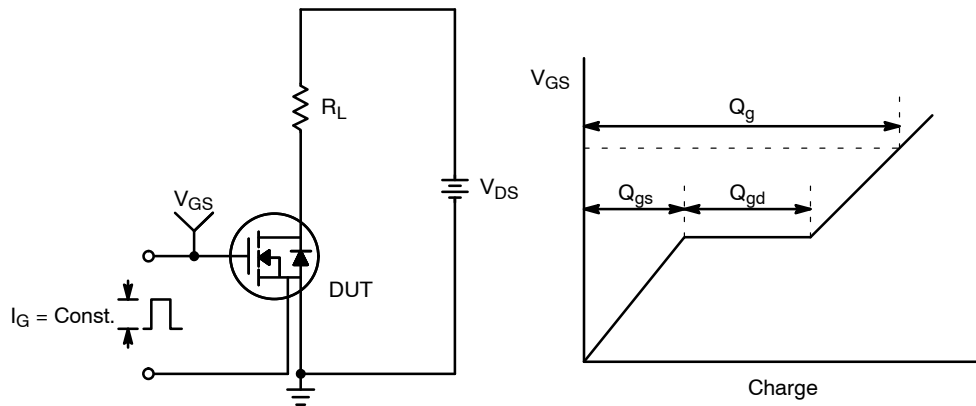


Figure 13. Gate Charge Test Circuit & Waveform

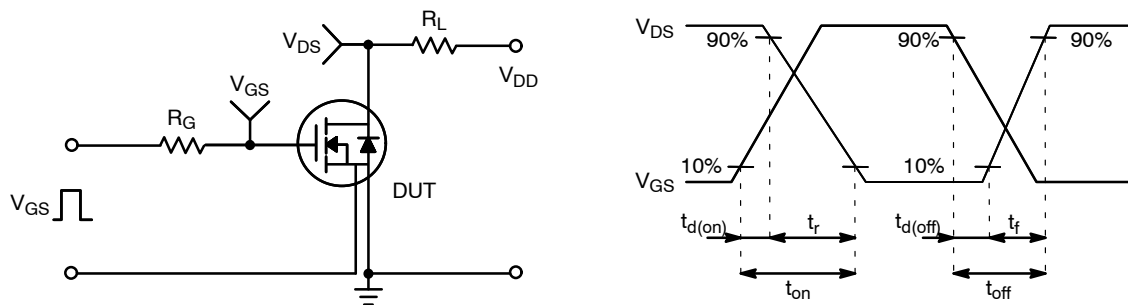


Figure 14. Resistive Switching Test Circuit & Waveforms

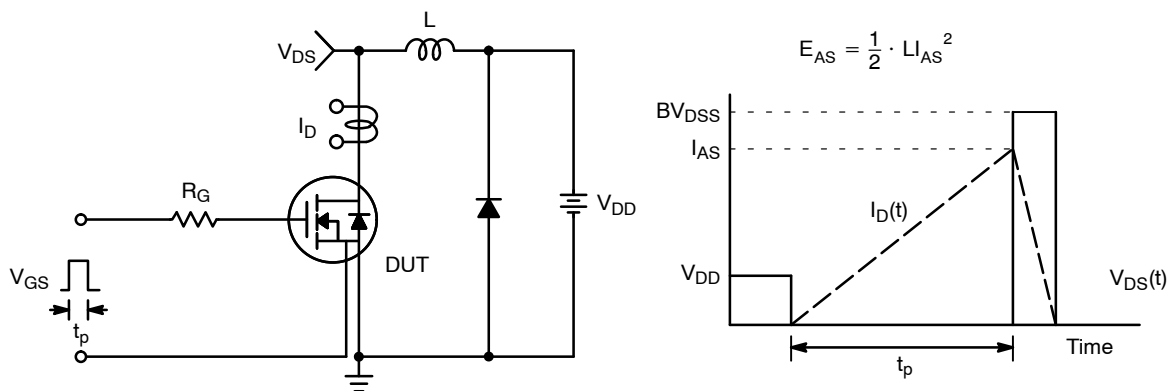


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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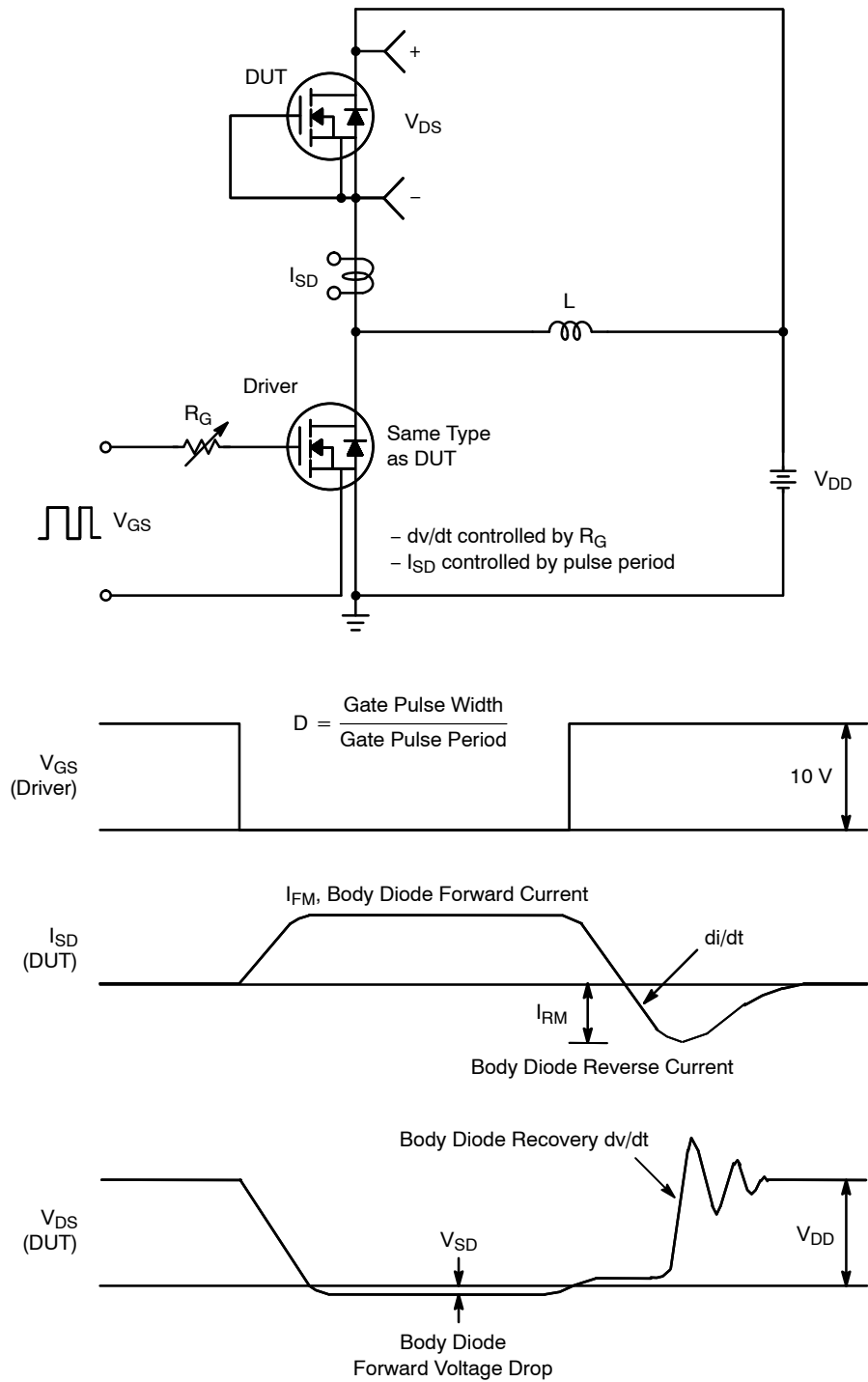
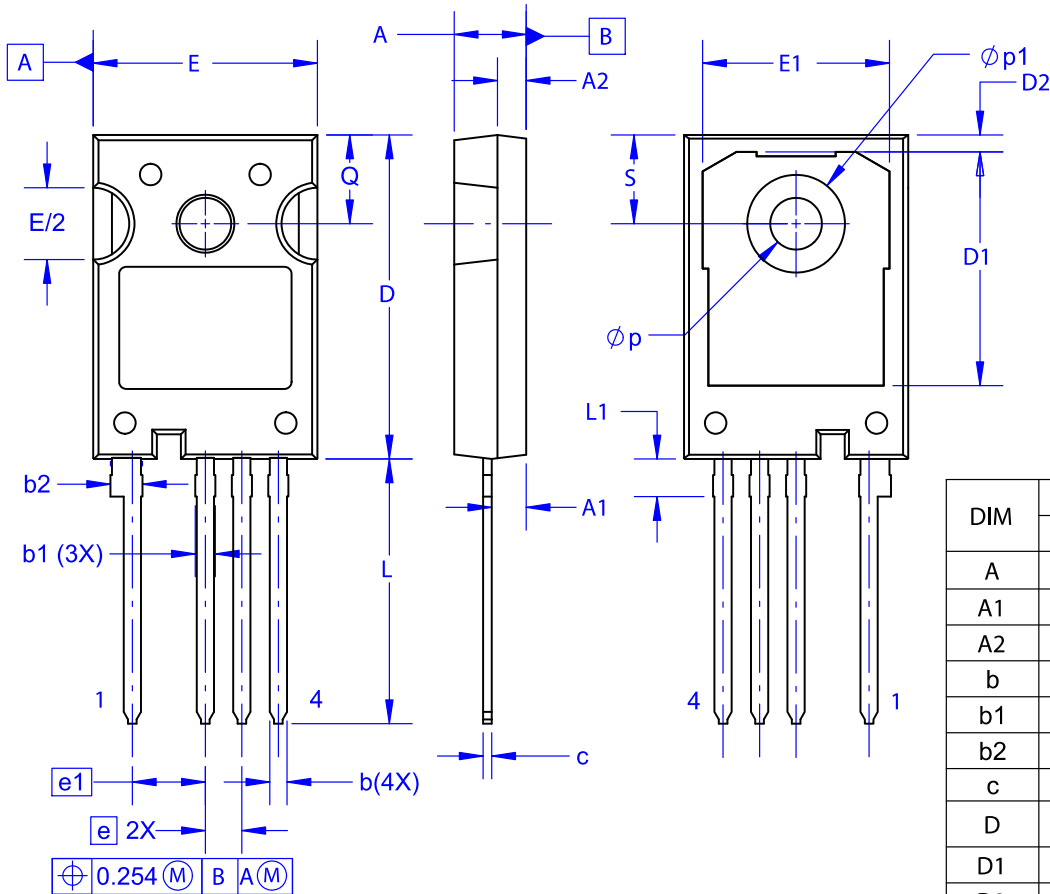


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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PACKAGE DIMENSIONS

TO-247-4LD
CASE 340CJ
ISSUE A



NOTES:

- NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DRAWING CONFORMS TO ASME Y14.5-2009.

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