

OPTIREG™ linear TLE42764

Low-dropout linear voltage regulator



Features

- Very low current consumption
- Adjustable and 5-V fixed output voltage $\pm 2\%$
- Output current up to 400 mA
- Enable input
- Very low dropout voltage
- Output current limitation
- Overtemperature shutdown
- Reverse polarity protection
- Wide temperature range from -40°C up to 150°C
- Green Product (RoHS compliant)

Potential applications

General automotive applications.

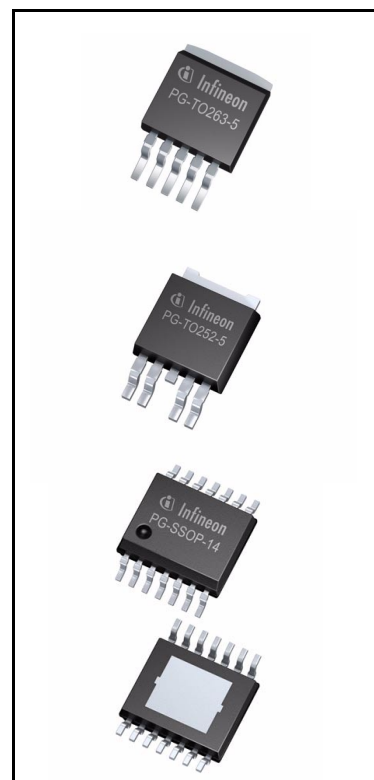
Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE42764 is a monolithic integrated low-dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to an adjustable or 5-V fixed voltage with a precision of $\pm 2\%$. The device is designed for the harsh environment of automotive applications. Therefore, it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE42764 can be also used in all other applications requiring a stabilized voltage between 2.5 V and 20 V.

Due to its very low quiescent current, the TLE42764 is dedicated for use in applications permanently connected to V_{BAT} . In addition, the device can be switched off via the enable input, reducing the current consumption to less than 10 μA .



Type	Package	Marking
TLE42764GV50	PG-TO263-5	42764V5
TLE42764DV50	PG-TO252-5	42764V5
TLE42764GV	PG-TO263-5	42764V

Type	Package	Marking
TLE42764DV	PG-TO252-5	42764V
TLE42764EV50	PG-SSOP-14 exposed pad	42764V5

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Block diagram

1 Block diagram

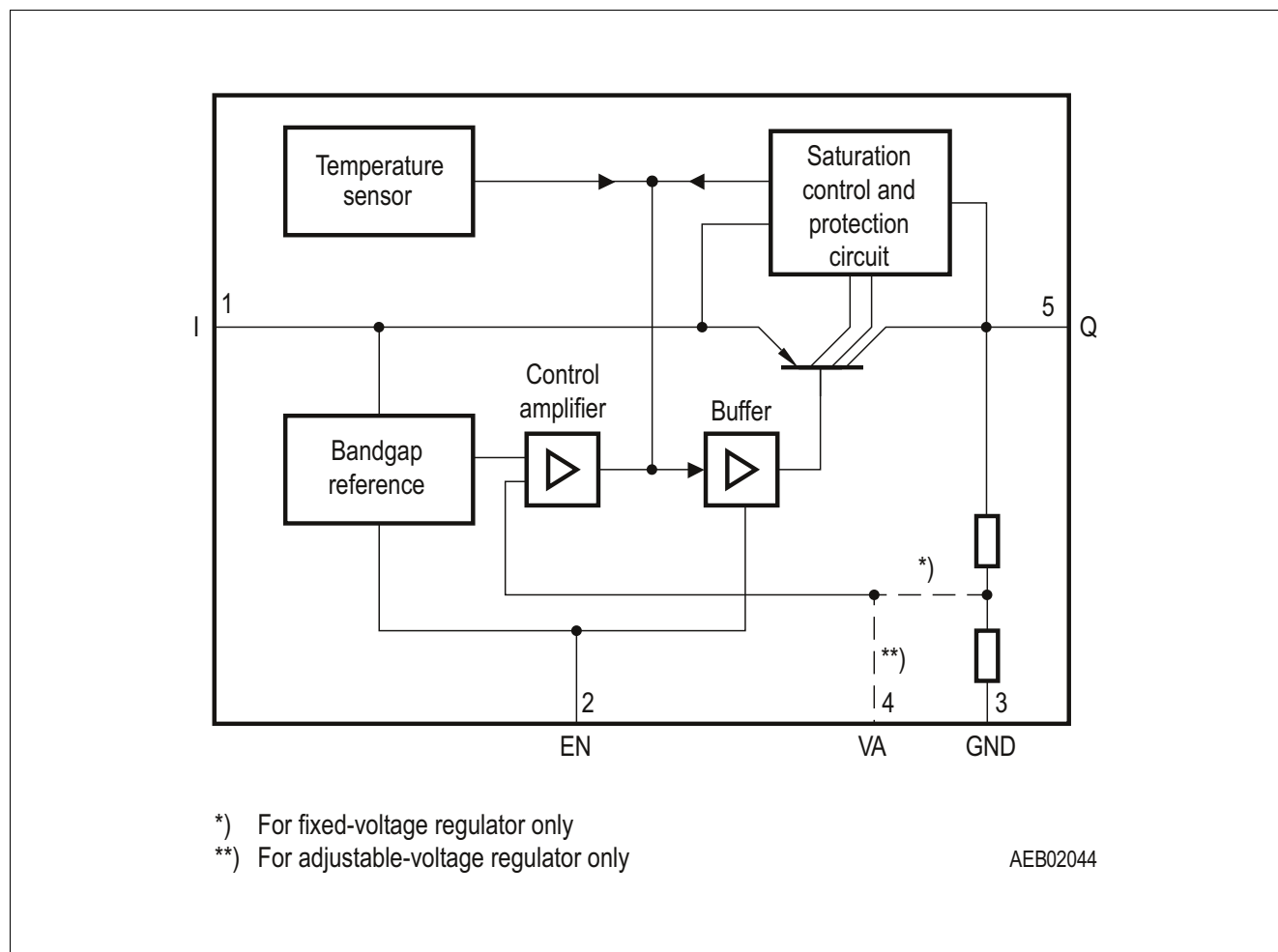


Figure 1 Block diagram

Pin configuration

2 Pin configuration

2.1 Pin assignment PG-TO263-5, PG-TO252-5

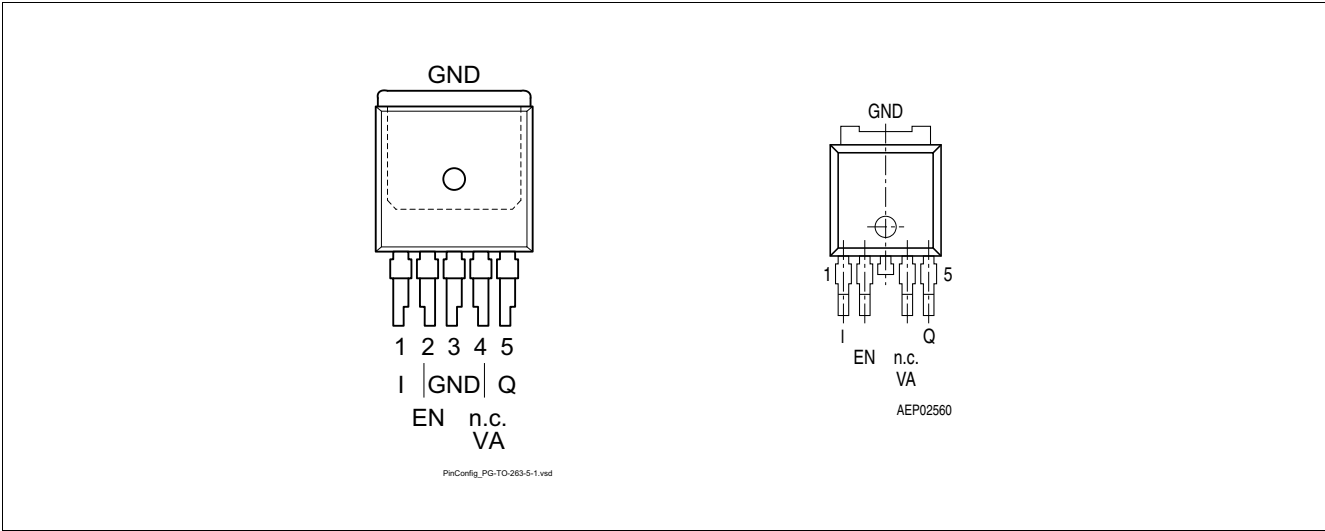


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions PG-TO263-5, PG-TO252-5

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	Input Block to ground directly at the IC with a ceramic capacitor
2	EN	Enable input High-level input signal enables the IC Low-level input signal disables the IC Integrated pull-down resistor
3	GND	Ground Internally connected to heat slug
4	n.c. VA	Not connected for TLE42764GV50, TLE42764DV50 Can be open or connected to GND Voltage-adjust input for TLE42764GV, TLE42764DV Connect external voltage divider to configure the output voltage
5	Q	Output Block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in “Functional range” on Page 8
Heat slug	–	Heat slug Internally connected to GND Connect to GND and heatsink area

Pin configuration

2.3 Pin assignment PG-SSOP-14 exposed pad

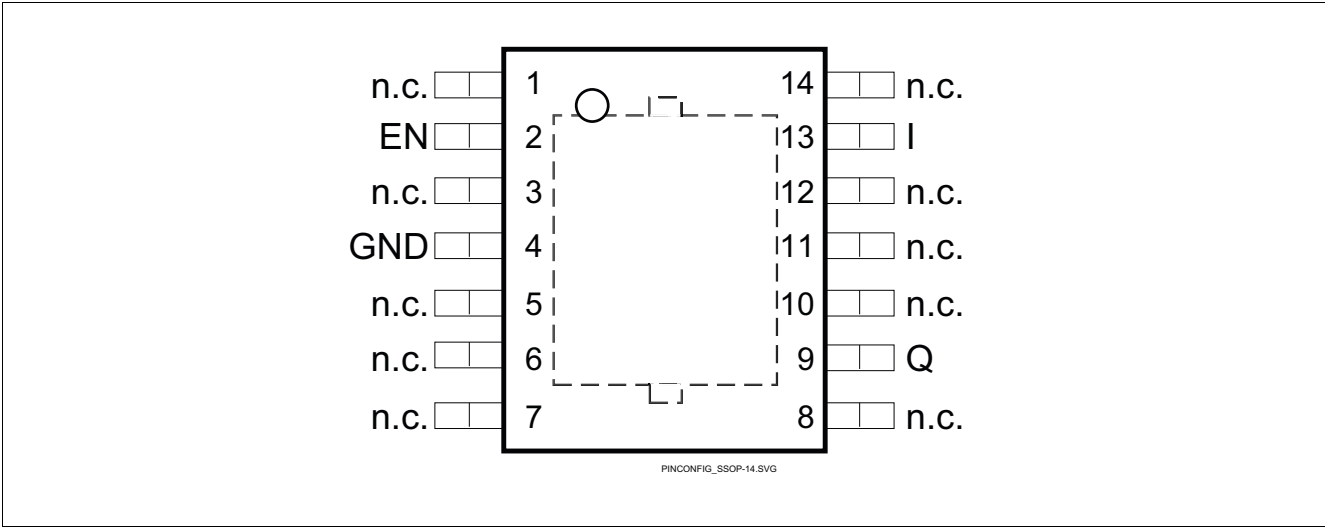


Figure 3 Pin configuration (top view)

2.4 Pin definitions and functions PG-SSOP-14 exposed pad

Table 2 Pin definitions and functions

Pin	Symbol	Function
1, 3, 5-7	n.c.	Not connected Can be open or connected to GND
2	EN	Enable input High-level input signal enables the IC Low-level input signal disables the IC Integrated pull-down resistor
4	GND	Ground
8, 10-12, 14	n.c.	Not connected Can be open or connected to GND
9	Q	Output Block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in “Functional range” on Page 8
13	I	Input Block to ground directly at the IC with a ceramic capacitor
Exposed pad	–	Exposed pad Connect to GND and heatsink area

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings¹⁾

$T_j = -40^{\circ}\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, enable EN							
Voltage	V_I	-42	–	45	V	–	P_4.1.1
Voltage adjust input VA							
Voltage	V_{VA}	-0.3	–	10	V	–	P_4.1.2
Output Q							
Voltage	V_Q	-1	–	40	V	–	P_4.1.3
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD susceptibility							
ESD absorption	$V_{ESD,HBM}$	-3	–	3	kV	²⁾ Human body model (HBM)	P_4.1.6
ESD absorption	$V_{ESD,CDM}$	-1000	–	1000	V	³⁾ Charge device model (CDM) at all pins	P_4.1.7

1) Not subject to production test, specified by design.

2) ESD susceptibility human body model “HBM” according to AEC-Q100-002 - JESD22-A114.

3) ESD susceptibility charged device model “CDM” according to ESDA STM5.3.1.

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

General product characteristics

3.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	5.5	–	40	V	TLE42764GV50, TLE42764DV50, TLE42764EV50	P_4.2.1
Input voltage	V_I	$V_Q + 0.5$	–	40	V	TLE42764GV, TLE42764DV, $V_Q > 4 \text{ V}$	P_4.2.2
Input voltage	V_I	4.5	–	40	V	TLE42764GV, TLE42764DV, $V_Q < 4 \text{ V}$	P_4.2.3
Output capacitor's requirements for stability	C_Q	22	–	–	μF	¹⁾	P_4.2.4
Output capacitor's requirements for stability	$ESR(C_Q)$	–	–	3	Ω	²⁾	P_4.2.5
Junction temperature	T_j	-40	–	150	$^{\circ}\text{C}$	–	P_4.2.6

1) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

2) Relevant ESR value at $f = 10 \text{ kHz}$.

Note: *Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

General product characteristics

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 5 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TLE42764GV, TLE42764GV50 (PG-TO263-5)							
Junction to case	R_{thJC}	–	3.6	–	K/W	¹⁾ Measured to heat slug	P_4.3.1
Junction to ambient	R_{thJA}	–	22	–	K/W	¹⁾²⁾	P_4.3.2
Junction to ambient	R_{thJA}	–	74	–	K/W	¹⁾³⁾ Footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	42	–	K/W	¹⁾³⁾ 300 mm ² heatsink area	P_4.3.4
Junction to ambient	R_{thJA}	–	34	–	K/W	¹⁾³⁾ 600 mm ² heatsink area	P_4.3.5
TLE42764DV, TLE42764DV50 (PG-TO252-5)							
Junction to case	R_{thJC}	–	3.6	–	K/W	¹⁾ Measured to heat slug	P_4.3.6
Junction to ambient	R_{thJA}	–	27	–	K/W	¹⁾²⁾	P_4.3.7
Junction to ambient	R_{thJA}	–	115	–	K/W	¹⁾³⁾ Footprint only	P_4.3.8
Junction to ambient	R_{thJA}	–	52	–	K/W	¹⁾³⁾ 300 mm ² heatsink area	P_4.3.9
Junction to ambient	R_{thJA}	–	40	–	K/W	¹⁾³⁾ 600 mm ² heatsink area	P_4.3.10
TLE42764EV50 (PG-SSOP-14 exposed pad)							
Junction to case	R_{thJC}	–	7	–	K/W	¹⁾	P_4.3.11
Junction to ambient	R_{thJA}	–	41	–	K/W	¹⁾²⁾	P_4.3.12
Junction to ambient	R_{thJA}	–	130	–	K/W	¹⁾³⁾ Footprint only	P_4.3.13
Junction to ambient	R_{thJA}	–	60	–	K/W	¹⁾³⁾ 300 mm ² heatsink area on PCB	P_4.3.14
Junction to ambient	R_{thJA}	–	50	–	K/W	¹⁾³⁾ 600 mm ² heatsink area on PCB	P_4.3.15

- 1) Not subject to production test, specified by design.
- 2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) Specified R_{thJA} value is according to JEDEC JESD51-3 at natural convection on FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μm Cu).

Electrical characteristics

4 Electrical characteristics

4.1 Electrical characteristics voltage regulator

Table 6 Electrical characteristics

$V_I = 13.5 \text{ V}$; $T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Q							
Output voltage	V_Q	4.9	5.0	5.1	V	TLE42764GV50, TLE42764DV50, TLE42764EV50, 5 mA < I_Q < 400 mA, 6 V < V_I < 28 V	P_5.1.1
Output voltage	V_Q	4.9	5.0	5.1	V	TLE42764GV50, TLE42764DV50, TLE42764EV50, 5 mA < I_Q < 200 mA, 6 V < V_I < 40 V	P_5.1.2
Output voltage	ΔV_Q	-2	–	2	%	¹⁾ TLE42764GV, TLE42764DV, R_2 < 50 k Ω , V_Q + 1 V < V_I < 28 V, V_I > 4.5 V, 5 mA $\leq I_Q \leq$ 400 mA	P_5.1.3
	ΔV_Q	-2	–	2	%	¹⁾ TLE42764GV, TLE42764DV, R_2 < 50 k Ω , V_Q + 1 V < V_I < 40 V, V_I > 4.5 V, 5 mA $\leq I_Q \leq$ 200 mA	
Output voltage adjustable range	$V_{Q,range}$	2.5	–	20	V	³⁾ TLE42764GV, TLE42764DV, see Page 15	P_5.1.4
Dropout voltage	V_{dr}	–	250	500	mV	²⁾ TLE42764GV50, TLE42764DV50, TLE42764EV50, I_Q = 250 mA, V_{dr} = V_I – V_Q	P_5.1.5
Dropout voltage	V_{dr}	–	250	500	mV	²⁾ TLE42764GV, TLE42764DV, I_Q = 250 mA, V_I > 4.5 V, V_{dr} = V_I – V_O	P_5.1.6

Electrical characteristics

Table 6 Electrical characteristics (cont'd)

$V_I = 13.5 \text{ V}$; $T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Load regulation	$\Delta V_{Q, lo}$	–	5	35	mV	$I_Q = 5 \text{ mA}$ to 400 mA , $V_I = 6 \text{ V}$ TLE42764GV50, TLE42764DV50, TLE42764EV50, $V_I = 4.5 \text{ V}$ TLE42764GV, TLE42764DV	P_5.1.7
Line regulation	$\Delta V_{Q, li}$	–	15	25	mV	$V_I = 12 \text{ V}$ to 32 V , $I_Q = 5 \text{ mA}$	P_5.1.8
Output current limitation	I_Q	400	600	1100	mA	²⁾	P_5.1.9
Power supply ripple rejection	$PSRR$	–	54	–	dB	³⁾ $f_r = 100 \text{ Hz}$, $V_r = 0.5 \text{ Vpp}$	P_5.1.10
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	³⁾	P_5.1.11

Current consumption

Current consumption, regulator disabled	I_q	–	–	10	μA	$V_{EN} = 0 \text{ V}$, $T_j \leq 100^\circ\text{C}$	P_5.1.12
Quiescent current $I_q = I_I - I_Q$	I_q	–	100	220	μA	$I_Q = 1 \text{ mA}$, $V_{EN} = 5 \text{ V}$	P_5.1.13
Current consumption $I_q = I_I - I_Q$	I_q	–	5	10	mA	$I_Q = 250 \text{ mA}$, $V_{EN} = 5 \text{ V}$	P_5.1.14
Current consumption $I_q = I_I - I_Q$	I_q	–	15	25	mA	$I_Q = 400 \text{ mA}$, $V_{EN} = 5 \text{ V}$	P_5.1.15

1) Influence of resistor divider on precision neglected.

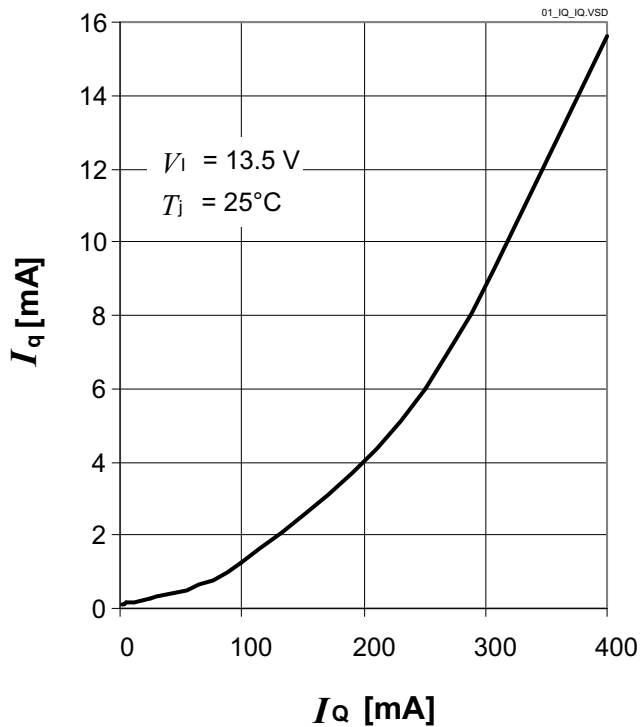
2) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at $V_I = 13.5 \text{ V}$.

3) Not subject to production test, specified by design.

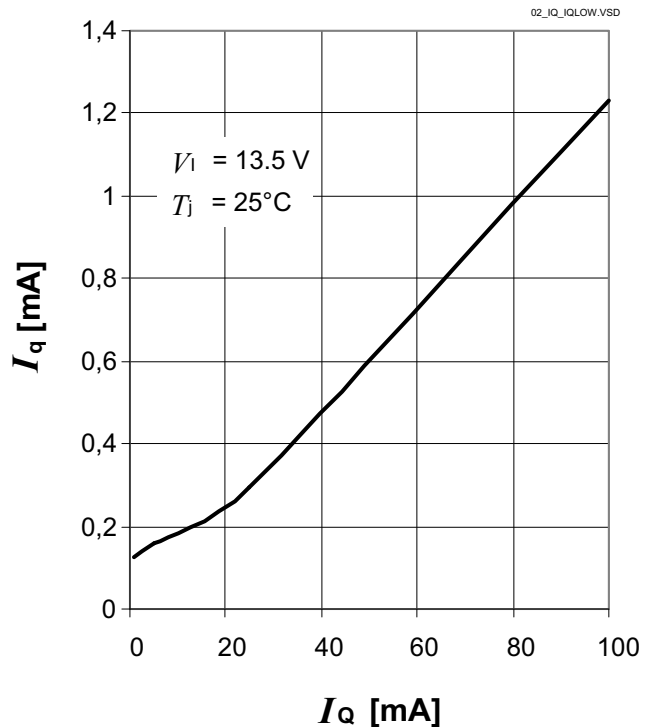
Electrical characteristics

4.2 Typical performance characteristics voltage regulator

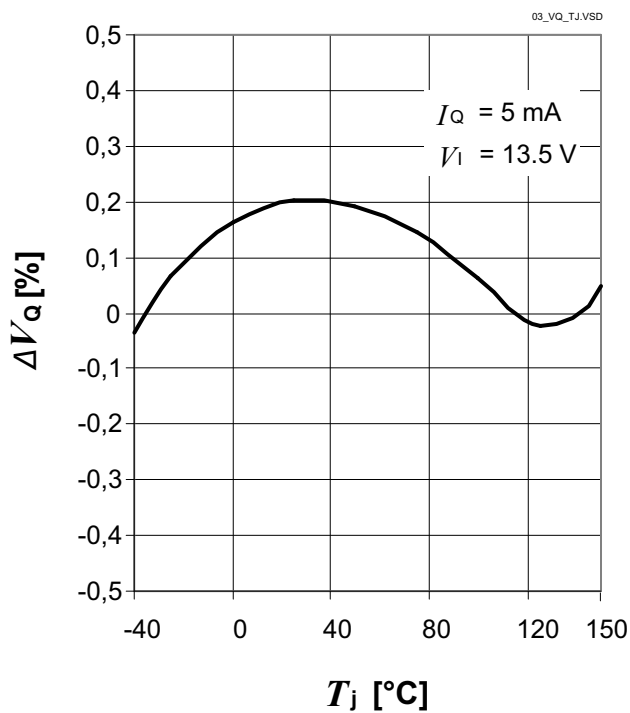
Current consumption I_q versus output current I_Q



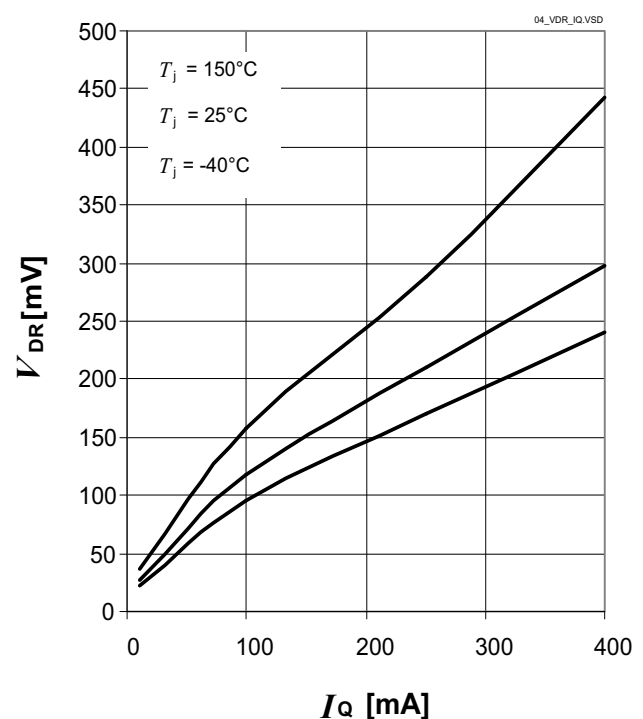
Current consumption I_q versus low output current I_Q



Output voltage V_Q versus junction temperature T_j

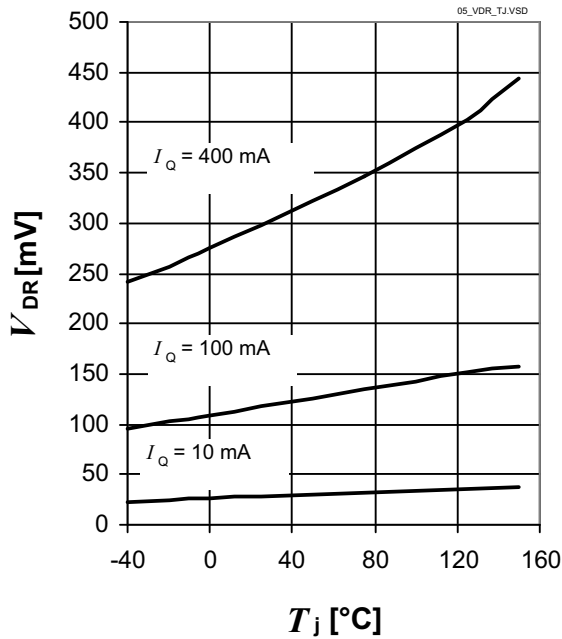


Dropout voltage V_{dr} versus output current I_Q

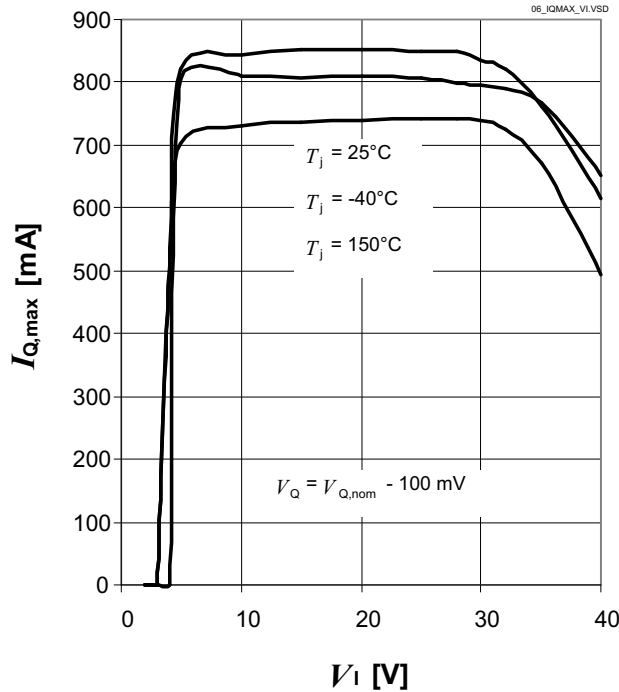


Electrical characteristics

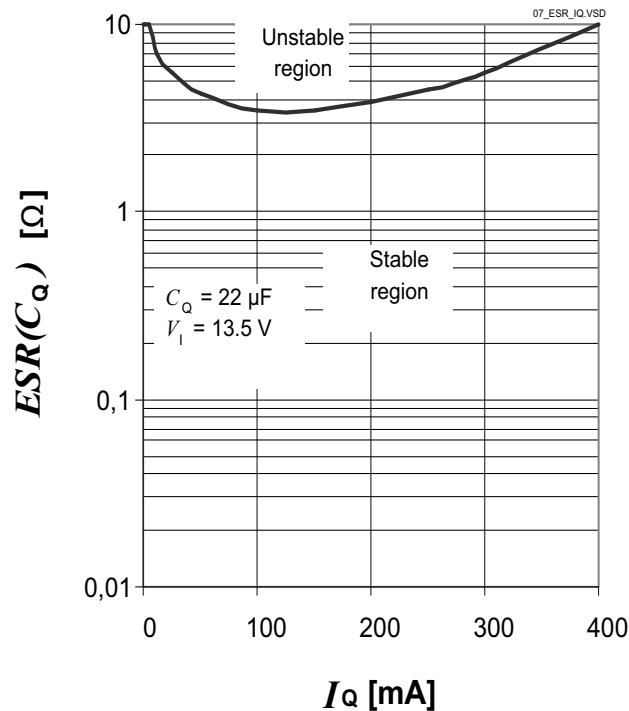
Dropout voltage V_{dr} versus
junction temperature



Maximum output current I_Q versus
input voltage V_I



Region of stability: Output capacitor's ESR $ESR(C_Q)$
versus output current I_Q



Electrical characteristics

4.3 Electrical characteristics enable function

The enable function allows disabling/enabling the regulator via the input pin EN. The regulator is turned on in case the pin EN is connected to a voltage higher than $V_{EN,H}$. This can be, for example, the battery voltage, whereby no additional pull-up resistor is needed. The regulator can be turned off by connecting the pin EN to a voltage less than $V_{EN,L}$, for example, GND.

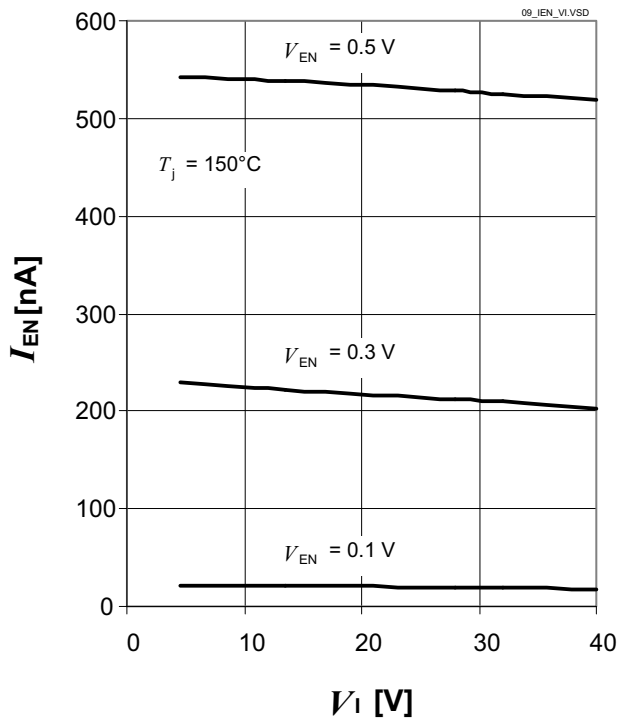
Table 7 Electrical characteristics enable

$V_I = 13.5\text{ V}$; $T_j = -40^\circ\text{C}$ to 150°C ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

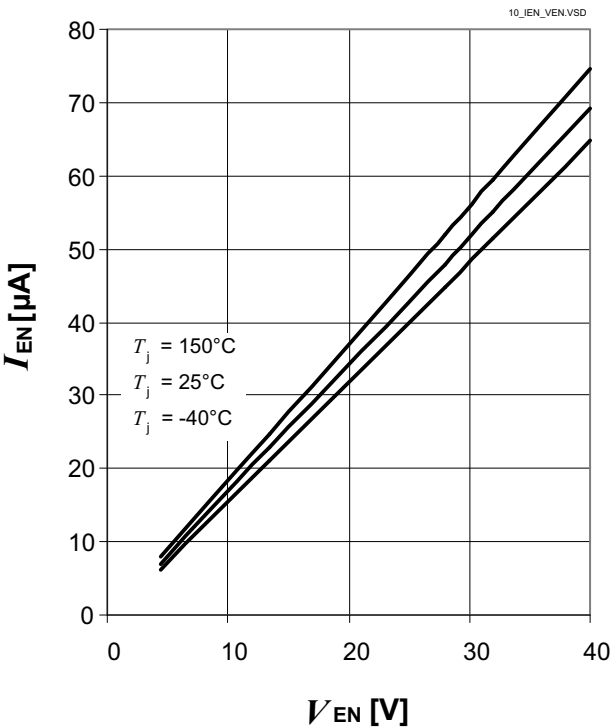
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
High-level input voltage	$V_{EN,H}$	3.5	–	–	V	$V_Q \geq 4.9\text{ V}$	P_5.3.16
Low-level input voltage	$V_{EN,L}$	–	–	0.5	V	$V_Q \leq 0.1\text{ V}$	P_5.3.17
High-level input current	$I_{EN,H}$	5	10	20	μA	$V_{EN} = 5\text{ V}$	P_5.3.18

4.4 Typical performance characteristics enable function

Enabled input current I_{EN} versus input voltage V_I , EN = Off



Enabled input current I_{EN} versus enabled input voltage V_{EN}



Application information

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

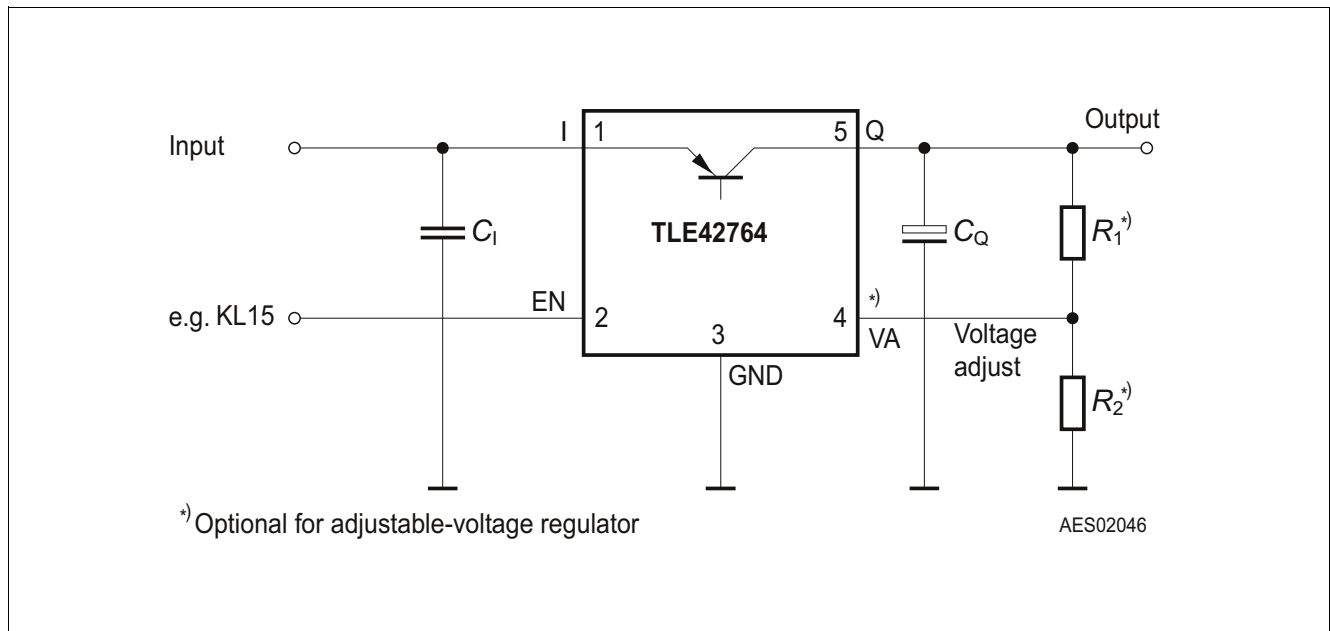


Figure 4 Application diagram

A typical application circuit of the TLE42764 is shown in **Figure 4**. It shows a generic configuration of the voltage regulator, with the recommended minimum number of components one should use. Theoretically, if there is no risk of high-frequency noise at all, even the small input filter capacitor can be omitted. For a normal operation mode of the device, the only required device is the output capacitor, for the TLE42764GV and the TLE42764DV additionally the resistor divider. However, depending on the application's environment, additional components like an input buffer capacitor or a reverse polarity protection diode can be considered as well.

Input filter capacitor

A small ceramic capacitor (for example, 100 nF in **Figure 4**) at the device's input helps filtering high-frequency noise. To reach the best filter effect, this capacitor should be placed as close as possible to the device's input pin. The input filter capacitor does not have an influence on the stability of the device's regulation loop.

Output capacitor C_Q

The output capacitor is the only external component that is required in any case, as it is a part of the device's regulating loop. To maintain stability of this loop, the TLE42764 requires an output capacitor respecting the values given in **"Functional range" on Page 8**.

Adjusting the output voltage of variable output regulators TLE42764GV, TLE42764DV

The output voltage of the TLE42764GV and the TLE42764DV can be adjusted between 2.5 V and 20 V by an external resistor divider, connected to the voltage adjust pin VA.

The pin VA is connected to the error amplifier comparing the voltage at this pin with the internal reference voltage of typically 2.5 V.

Application information

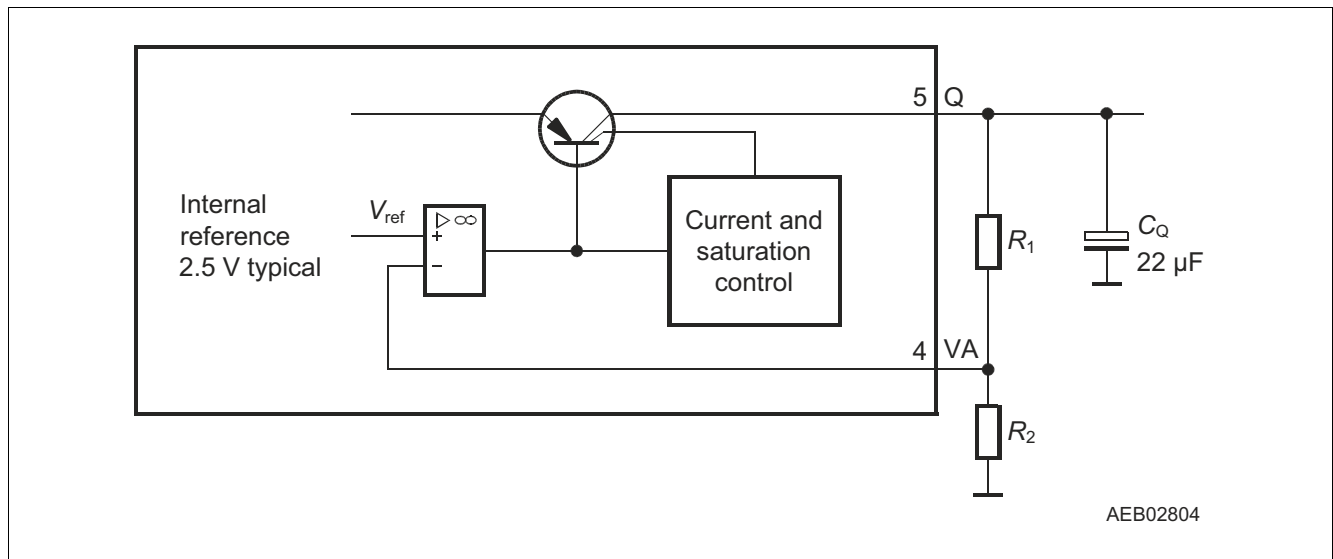


Figure 5 External components at output for variable voltage regulator

The output voltage can be easily calculated, neglecting the current flowing into the VA pin:

$$V_Q = \frac{R_1 + R_2}{R_2} \times V_{ref} \quad (5.1)$$

where

$$R_2 < 50 \text{ k}\Omega \quad (5.2)$$

to neglect the current flowing into the VA pin, with:

- V_{ref} : internal reference voltage, typically 2.5 V
- R_1 : resistor between regulator output Q and voltage adjust pin VA
- R_2 : resistor between voltage adjust pin VA and GND

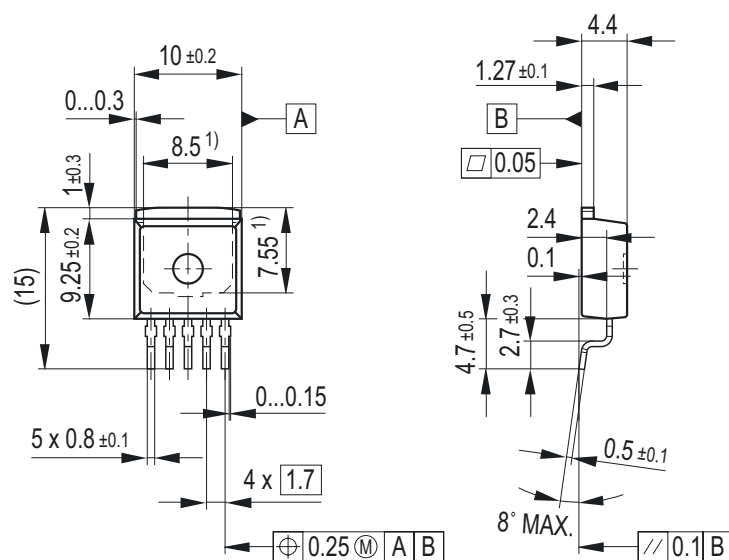
For a 2.5-V output voltage, the output pin Q has to be directly connected to the adjust pin VA.

Take into consideration that the accuracy of the resistors R_1 and R_2 adds an additional error to the output voltage tolerance.

5.1 Further application information

For further information you may contact <https://www.infineon.com>.

6 Package information



1) Typical

Metal surface min. X = 7.25, Y = 6.9

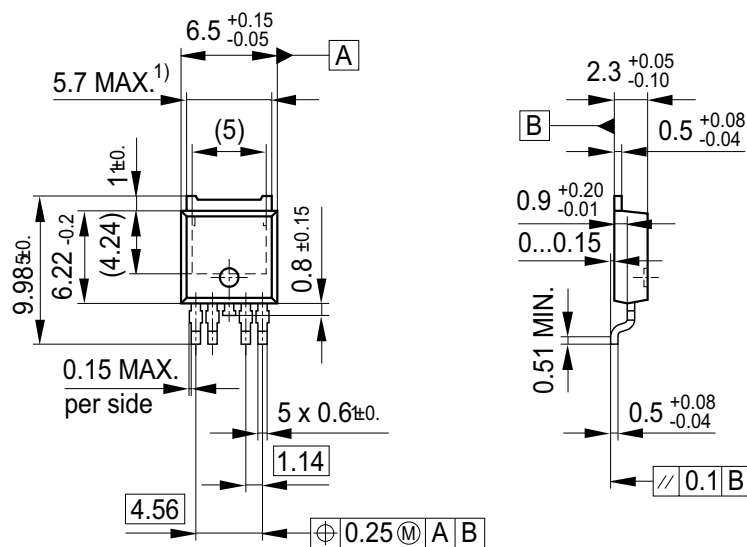
All metal surfaces tin plated, except area of cut.

GPT09113

Figure 6 PG-T0263-5¹⁾

1) Dimensions in mm

Package information



1) Includes mold flashes on each side.
 All metal surfaces tin plated, except area of cut.

Figure 7 PG-T0252-5¹⁾

1) Dimensions in mm

Package information

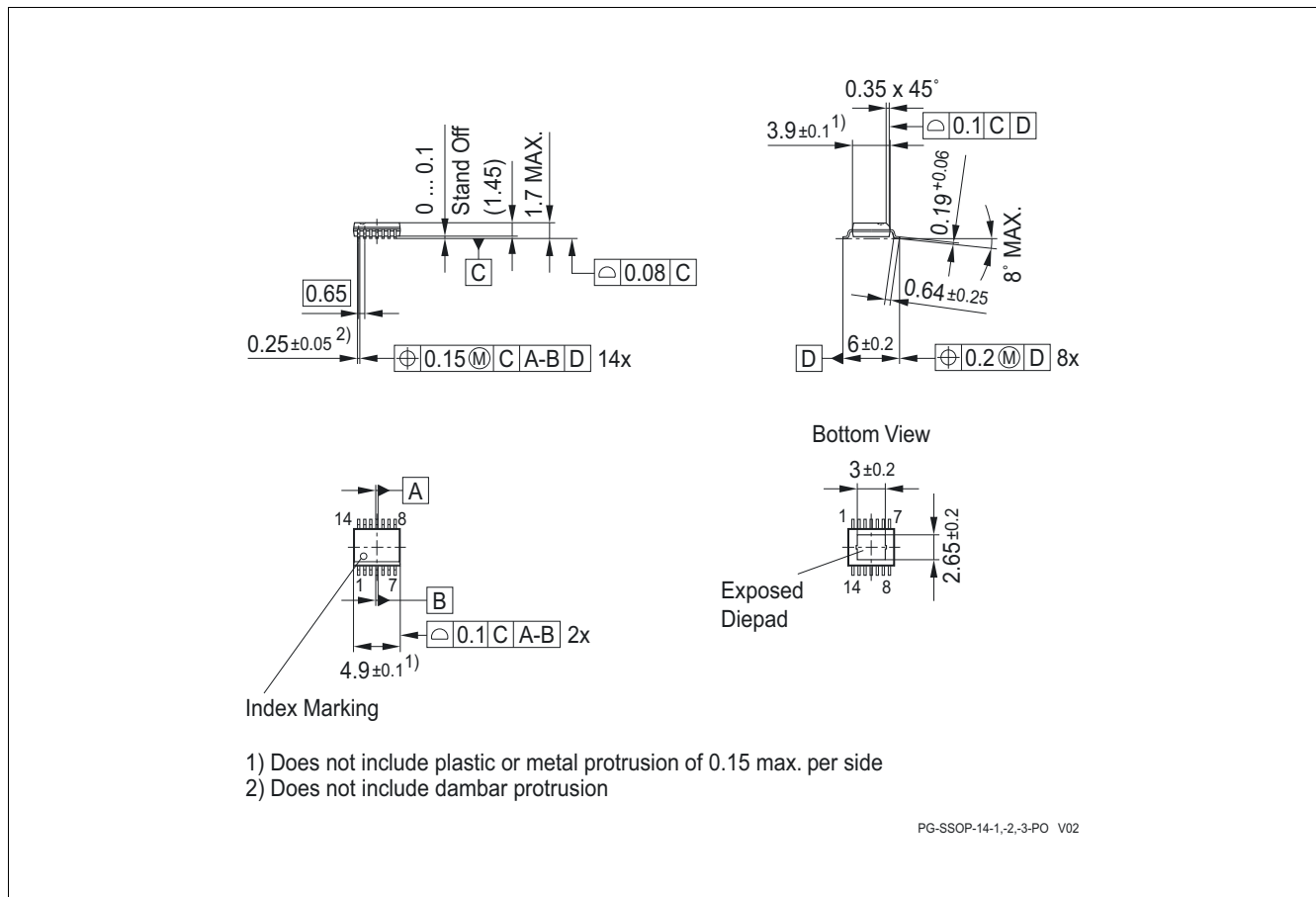


Figure 8 PG-SSOP-14 exposed pad¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

Revision history

7 Revision history

Revision	Date	Changes
1.31	2023-06-05	Editorial changes
1.3	2013-07-30	Split of the accuracy specification for the adjustable variants TLE42764GV and TLE42764DV (5.1.3) into two different conditions. For high input voltages up to 40 V and output current up to 200 mA the accuracy is specified with $\pm 2\%$. For input voltages up to 28 V, the output current is allowed to go up to 400 mA to achieve an accuracy of $\pm 2\%$ according to the specification.
1.2	2011-02-15	Updated version final datasheet: 5-V version TLE42764EV50 in PG-SSOP-14 exposed pad package and all related description added
1.1	2009-10-09	Updated version final datasheet: 5-V versions in PG-TO252-5 and PG-TO263-5 package and all related descriptions added
		In "Features" on page 2 in text "and 5 V Fixed" added
		In "Description" on page 2 "or 5 V fixed" added
		In table on bottom of page "Overview" on page 2 2 product versions including package and marking added
		In "Functional Range" on page 7 item 4.2.1 added
		In "Electrical Characteristics Voltage Regulator" on page 9 item 5.1.1, item 5.1.2 and item 5.1.5 added; in conditions of item 5.1.7 " $V_I = 6\text{ V}$ TLE42764GV50, TLE42764DV50;" added
1.0	2008-01-14	Initial version final datasheet

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