

# MC74HC08A

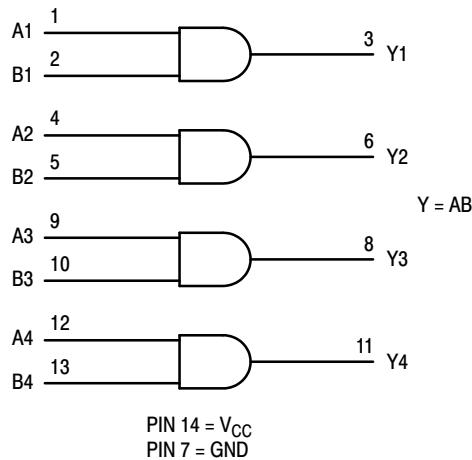
## Quad 2-Input AND Gate High-Performance Silicon-Gate CMOS

The MC74HC08A is identical in pinout to the LS08. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

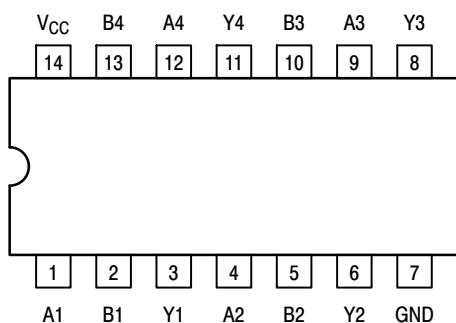
### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

### LOGIC DIAGRAM



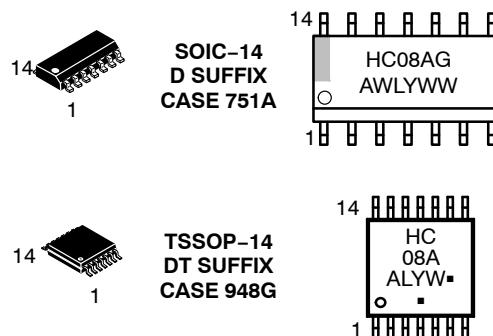
### Pinout: 14-Lead Packages (Top View)



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### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | L      |
| H      | L | L      |
| H      | H | H      |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HC08A

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | – 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | – 0.5 to $V_{CC}$ + 0.5 | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | – 0.5 to $V_{CC}$ + 0.5 | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>SOIC Package†<br>TSSOP Package†       | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature  | – 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C  
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter   | Min   | Max                   | Unit     |
|-------------------|---|---|-----------------------|----------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                   | 2.0   | 6.0                   | V        |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage<br>(Referenced to GND) | 0   | $V_{CC}$              | V        |
| $T_A$             | Operating Temperature, All Package Types                | – 55  | + 125                 | °C       |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)                  | 0<br>$V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 1000<br>0<br>500<br>0 | ns<br>ns |

## ORDERING INFORMATION

| Device           | Package               | Shipping <sup>†</sup> |
|------------------|-----------------------|-----------------------|
| MC74HC08ADG      | SOIC-14<br>(Pb-Free)  | 55 Units / Rail       |
| MC74HC08ADR2G    | SOIC-14<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC74HC08ADTR2G   | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel    |
| NLV74HC08ADG*    | SOIC-14<br>(Pb-Free)  | 55 Units / Rail       |
| NLV74HC08ADR2G*  | SOIC-14<br>(Pb-Free)  | 2500 / Tape & Reel    |
| NLV74HC08ADTR2G* | TSSOP-14<br>(Pb-Free) | 2500 / Tape & Reel    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

# MC74HC08A

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Condition  | V <sub>CC</sub><br>V     | Guaranteed Limit             |                              |                              | Unit |
|-----------------|--|--|--------------------------|------------------------------|------------------------------|------------------------------|------|
|                 |  |  |                          | -55 to 25°C                  | ≤85°C                        | ≤125°C                       |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1V or V <sub>CC</sub> – 0.1V<br> I <sub>out</sub>   ≤ 20µA  | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1V or V <sub>CC</sub> – 0.1V<br> I <sub>out</sub>   ≤ 20µA  | 2.0<br>3.0<br>4.5<br>6.0 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20µA   | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | V    |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0<br>4.5<br>6.0        | 2.48<br>3.98<br>5.48         | 2.34<br>3.84<br>5.34         | 2.20<br>3.70<br>5.20         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20µA   | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | V    |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0<br>4.5<br>6.0        | 0.26<br>0.26<br>0.26         | 0.33<br>0.33<br>0.33         | 0.40<br>0.40<br>0.40         |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                      | ±0.1                         | ±1.0                         | ±1.0                         | µA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0µA   | 6.0                      | 1.0                          | 10                           | 40                           | µA   |

## AC CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V   | Guaranteed Limit     |                      |                       | Unit |
|--|--|--|----------------------|----------------------|-----------------------|------|
|  |  |  | -55 to 25°C          | ≤85°C                | ≤125°C                |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A or B to Output Y<br>(Figures 1 and 2) | 2.0<br>3.0<br>4.5<br>6.0                                       | 75<br>30<br>15<br>13 | 95<br>40<br>19<br>16 | 110<br>55<br>22<br>19 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)          | 2.0<br>3.0<br>4.5<br>6.0                                       | 75<br>27<br>15<br>13 | 95<br>32<br>19<br>16 | 110<br>36<br>22<br>19 | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance  |  | 10                   | 10                   | 10                    | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Buffer)*                              | Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V |                      |                      |                       | pF   |
|  |  | 20   |                      |                      |                       |      |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC08A

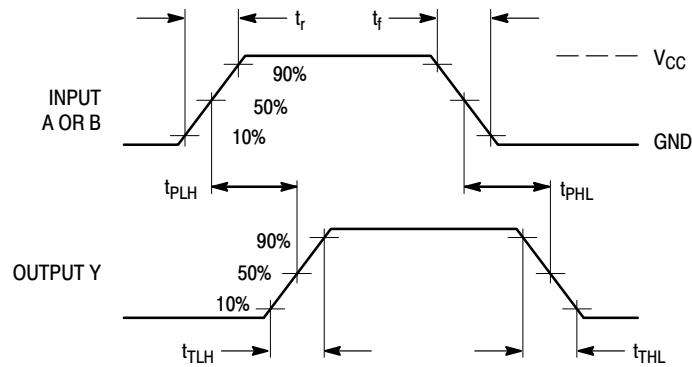
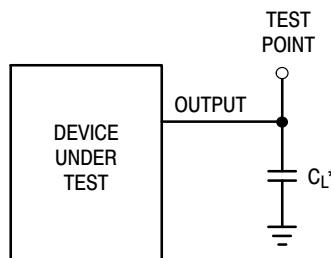


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

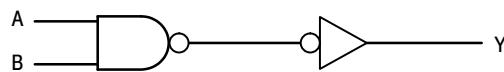


Figure 3. Expanded Logic Diagram  
(1/4 of the Device)

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

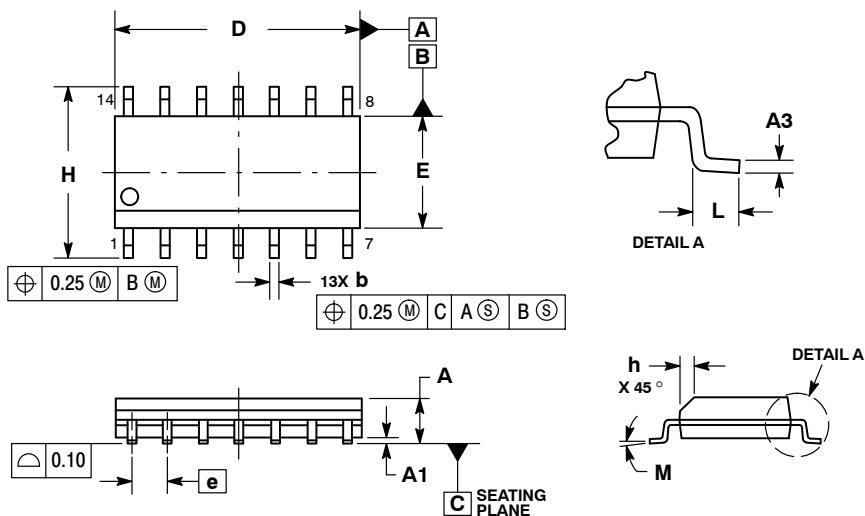
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SCALE 1:1

SOIC-14 NB  
CASE 751A-03  
ISSUE L

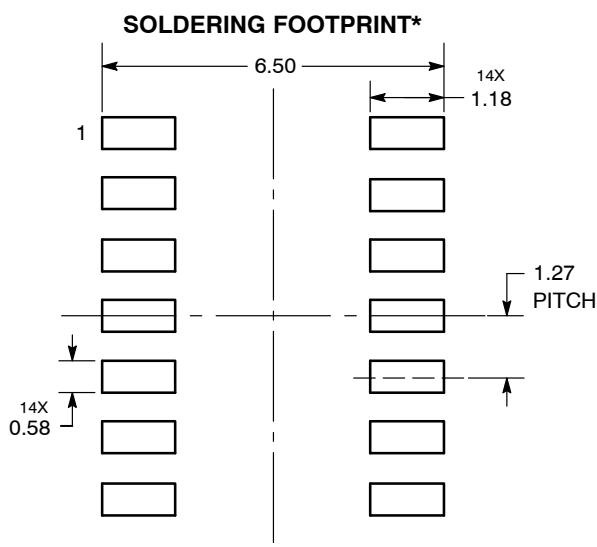
DATE 03 FEB 2016



NOTES:

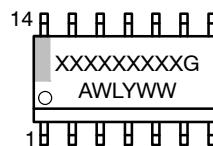
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0 °         | 7 °  | 0 °       | 7 °   |



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "■", may or may not be present.

STYLES ON PAGE 2

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**SOIC-14**  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

**STYLE 1:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. NO CONNECTION  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 2:**  
CANCELLED

**STYLE 3:**  
PIN 1. NO CONNECTION  
2. ANODE  
3. ANODE  
4. NO CONNECTION  
5. ANODE  
6. NO CONNECTION  
7. ANODE  
8. ANODE  
9. ANODE  
10. NO CONNECTION  
11. ANODE  
12. ANODE  
13. NO CONNECTION  
14. COMMON CATHODE

**STYLE 4:**  
PIN 1. NO CONNECTION  
2. CATHODE  
3. CATHODE  
4. NO CONNECTION  
5. CATHODE  
6. NO CONNECTION  
7. CATHODE  
8. CATHODE  
9. CATHODE  
10. NO CONNECTION  
11. CATHODE  
12. CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 5:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. NO CONNECTION  
7. COMMON ANODE  
8. COMMON CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. ANODE/CATHODE  
12. ANODE/CATHODE  
13. NO CONNECTION  
14. COMMON ANODE

**STYLE 6:**  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE  
7. CATHODE  
8. ANODE  
9. ANODE  
10. ANODE  
11. ANODE  
12. ANODE  
13. ANODE  
14. ANODE

**STYLE 7:**  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. ANODE/CATHODE  
8. ANODE/CATHODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. COMMON CATHODE  
12. COMMON ANODE  
13. ANODE/CATHODE  
14. ANODE/CATHODE

**STYLE 8:**  
PIN 1. COMMON CATHODE  
2. ANODE/CATHODE  
3. ANODE/CATHODE  
4. NO CONNECTION  
5. ANODE/CATHODE  
6. ANODE/CATHODE  
7. COMMON ANODE  
8. COMMON ANODE  
9. ANODE/CATHODE  
10. ANODE/CATHODE  
11. NO CONNECTION  
12. ANODE/CATHODE  
13. ANODE/CATHODE  
14. COMMON CATHODE

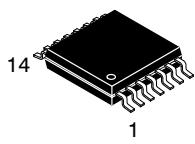
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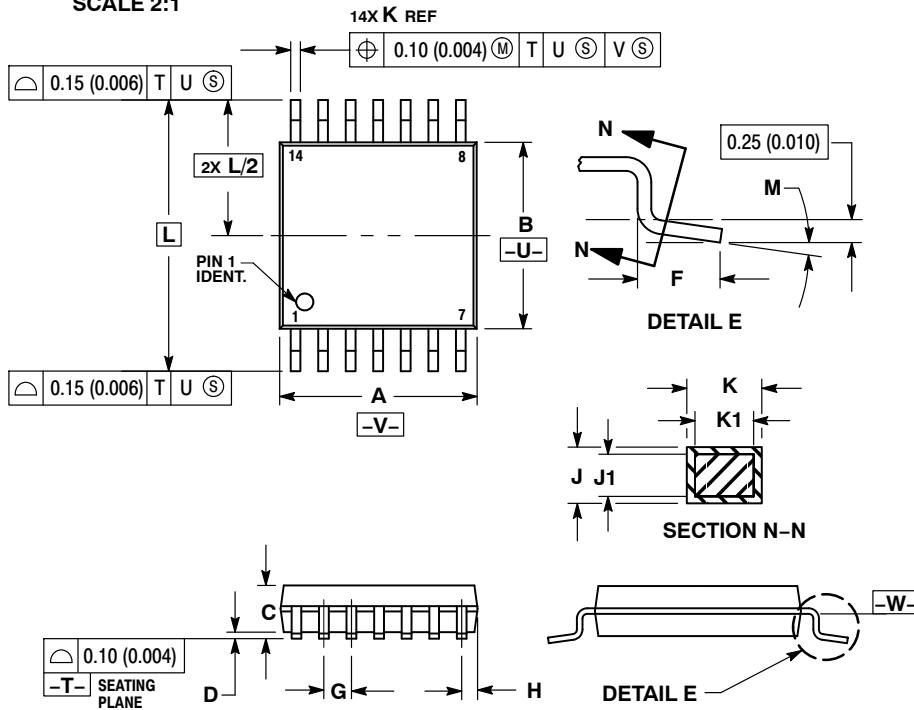
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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1  
SCALE 2:1



TSSOP-14 WB  
CASE 948G  
ISSUE C

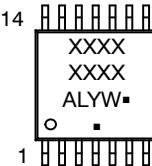
DATE 17 FEB 2016

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES |       |
|-----|-------------|------|--------|-------|
|     | MIN         | MAX  | MIN    | MAX   |
| A   | 4.90        | 5.10 | 0.193  | 0.200 |
| B   | 4.30        | 4.50 | 0.169  | 0.177 |
| C   | ---         | 1.20 | ---    | 0.047 |
| D   | 0.05        | 0.15 | 0.002  | 0.006 |
| F   | 0.50        | 0.75 | 0.020  | 0.030 |
| G   | 0.65        | BSC  | 0.026  | BSC   |
| H   | 0.50        | 0.60 | 0.020  | 0.024 |
| J   | 0.09        | 0.20 | 0.004  | 0.008 |
| J1  | 0.09        | 0.16 | 0.004  | 0.006 |
| K   | 0.19        | 0.30 | 0.007  | 0.012 |
| K1  | 0.19        | 0.25 | 0.007  | 0.010 |
| L   | 6.40        | BSC  | 0.252  | BSC   |
| M   | 0°          | 8°   | 0°     | 8°    |

GENERIC  
MARKING DIAGRAM\*

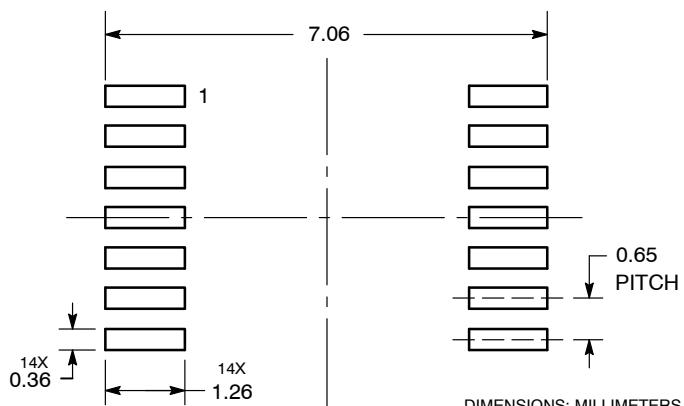


A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "■", may or may not be present.

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