

# MOSFET - Power, Single N-Channel, SUPERFET® V, FRFET®, TDFN4 600 V, 61 mΩ, 41 A NTMT061N60S5F

## Description

The SUPERFET V MOSFET FRFET series, optimized reverse recovery performance of body diode, can remove additional component and improve system reliability for soft switching applications such as PSFB and LLC. The Power88 package which is an ultra-slim SMD package offers excellent switching performance by providing kelvin source configuration and lower parasitic source inductance.

## Features

- 650 V @  $T_J = 150^\circ\text{C}$  / Typ.  $R_{DS(on)} = 48.8 \text{ m}\Omega$
- 100% Avalanche Tested / MSL1 Qualified
- Kelvin Source Configuration and Low Parasitic Source Inductance
- Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

## Applications

- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Lighting / Charger/ Adapter / Industrial Power Supplies

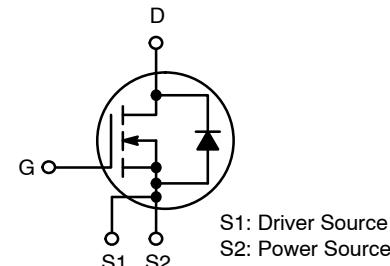
## ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ , Unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	600	V
Gate-to-Source Voltage	$V_{GSS}$	$\pm 30$	V
		$\pm 30$	
Continuous Drain Current	$I_D$	41	A
		25	
Power Dissipation	$P_D$	255	W
Pulsed Drain Current (Note 1)	$I_{DM}$	146	A
Pulsed Source Current (Body Diode) (Note 1)	$I_{SM}$	146	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C
Source Current (Body Diode)	$I_S$	41	A
Single Pulse Avalanche Energy	$E_{AS}$	376	mJ
Avalanche Current	$I_{AS}$	6.7	A
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	2.55	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		70	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	$T_L$	260	°C

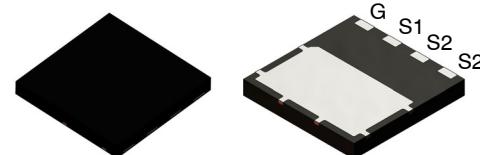
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{SD} \leq 20.5 \text{ A}$ ,  $dI/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 400 \text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

$V_{DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
600 V	61 mΩ @ 10 V	41 A

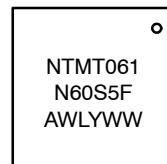


POWER MOSFET



TDFN4 8x8 2P  
CASE 520AB

## MARKING DIAGRAM



NTMT061N60S5F = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

## ORDERING INFORMATION

Device	Package	Shipping
NTMT061N60S5F	TDFN4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMT061N60S5F

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	$R_{\theta JC}$	0.49	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max.	$R_{\theta JA}$	45	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	$I_D = 10 \text{ mA}$ , Referenced to $25^{\circ}\text{C}$	–	630	–	$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 600 \text{ V}, T_J = 25^{\circ}\text{C}$	–	–	10	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}} = \pm 30 \text{ V}, V_{\text{DS}} = 0 \text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 20.5 \text{ A}, T_J = 25^{\circ}\text{C}$	–	48.8	61	$\text{m}\Omega$
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 4.6 \text{ mA}, T_J = 25^{\circ}\text{C}$	3.2	–	4.8	V
Forward Trans-conductance	$g_{\text{FS}}$	$V_{\text{DS}} = 20 \text{ V}, I_D = 20.5 \text{ A}$	–	39	–	S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 400 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 250 \text{ kHz}$	–	4175	–	pF
Output Capacitance	$C_{\text{oss}}$		–	63	–	
Time Related Output Capacitance	$C_{\text{OSS}(\text{tr.})}$	$I_D = \text{Constant}, V_{\text{DS}} = 0 \text{ V to } 400 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	–	963	–	
Energy Related Output Capacitance	$C_{\text{OSS}(\text{er.})}$	$V_{\text{DS}} = 0 \text{ V to } 400 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	–	103	–	
Total Gate Charge	$Q_{\text{G}(\text{tot})}$	$V_{\text{DD}} = 400 \text{ V}, I_D = 20.5 \text{ A}, V_{\text{GS}} = 10 \text{ V}$	–	76	–	nC
Gate-to-Source Charge	$Q_{\text{GS}}$		–	23	–	
Gate-to-Drain Charge	$Q_{\text{GD}}$		–	23	–	
Gate Resistance	$R_{\text{G}}$		$f = 1 \text{ MHz}$	6	–	$\Omega$

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 0/10 \text{ V}, V_{\text{DD}} = 400 \text{ V}, I_D = 20.5 \text{ A}, R_{\text{G}} = 4.7 \Omega$	–	42	–	ns
Rise Time	$t_r$		–	15	–	
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		–	108	–	
Fall Time	$t_f$		–	2.8	–	

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{\text{SD}}$	$V_{\text{GS}} = 0 \text{ V}, I_{\text{SD}} = 20.5 \text{ A}, T_J = 25^{\circ}\text{C}$	–	–	1.2	V
Reverse Recovery Time	$t_{\text{RR}}$	$V_{\text{GS}} = 0 \text{ V}, I_{\text{SD}} = 20.5 \text{ A},$ $dl/dt = 100 \text{ A}/\mu\text{s}, V_{\text{DD}} = 400 \text{ V}$	–	124	–	ns
Reverse Recovery Charge	$Q_{\text{RR}}$		–	717	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS

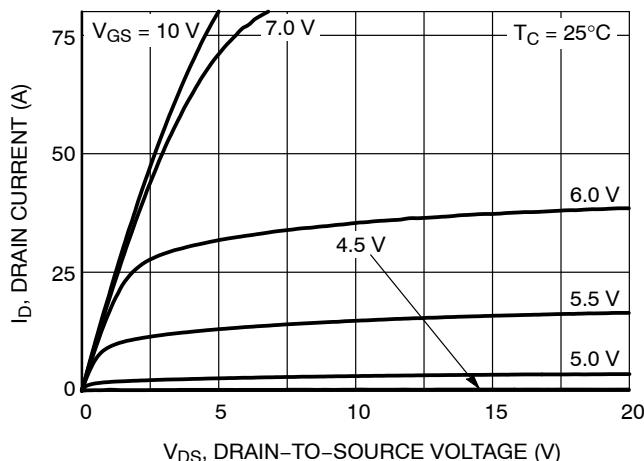


Figure 1. On-Region Characteristics

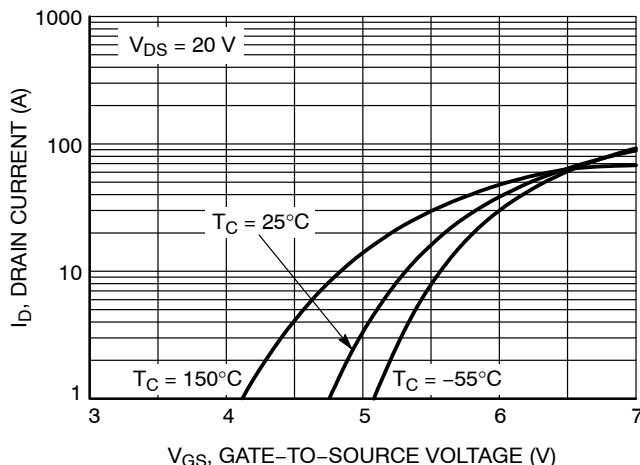


Figure 2. Transfer Characteristics

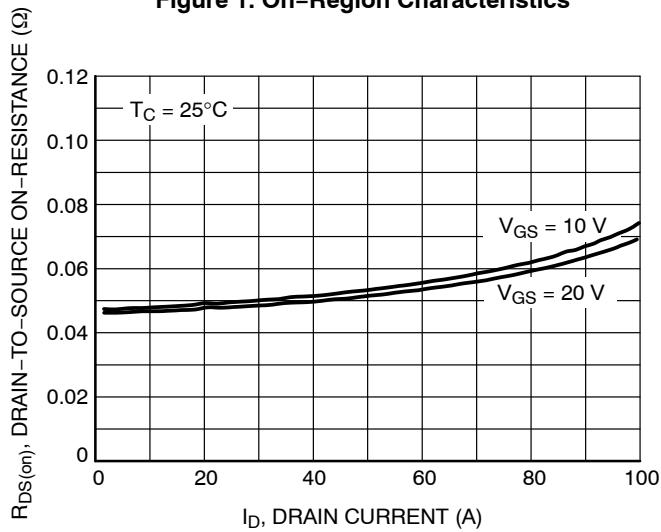


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

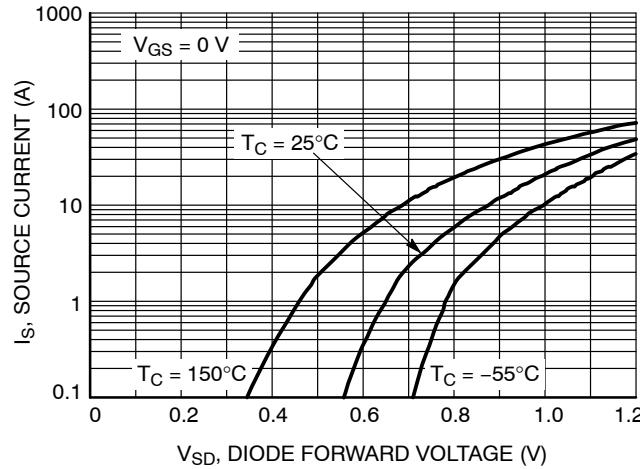


Figure 4. Diode Forward Voltage vs. Source Current

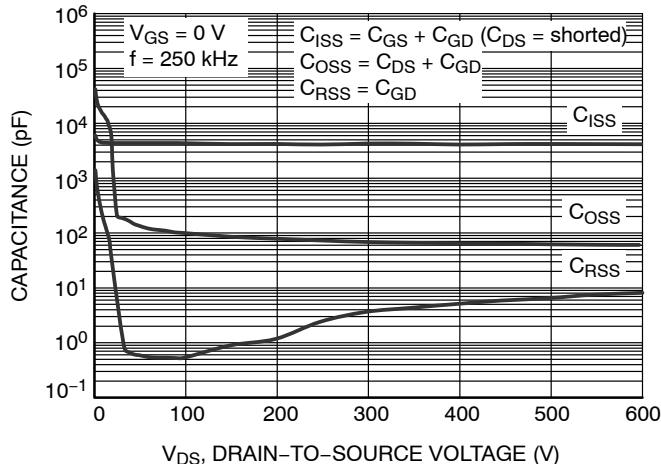


Figure 5. Capacitance Characteristics

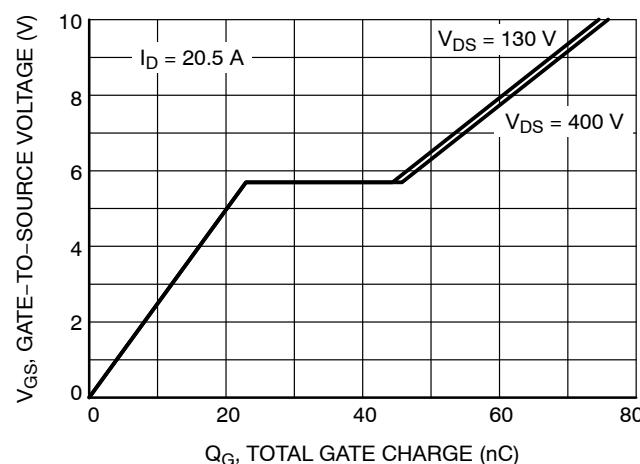
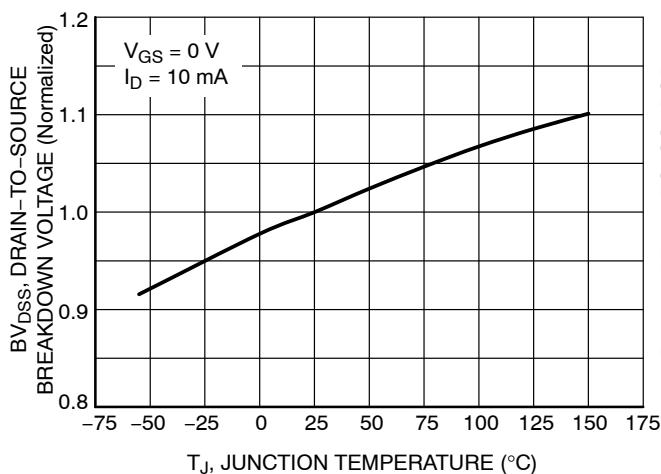
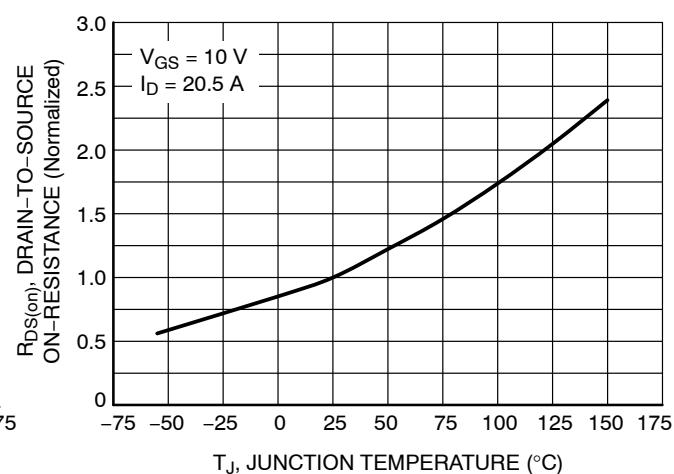


Figure 6. Gate Charge Characteristics

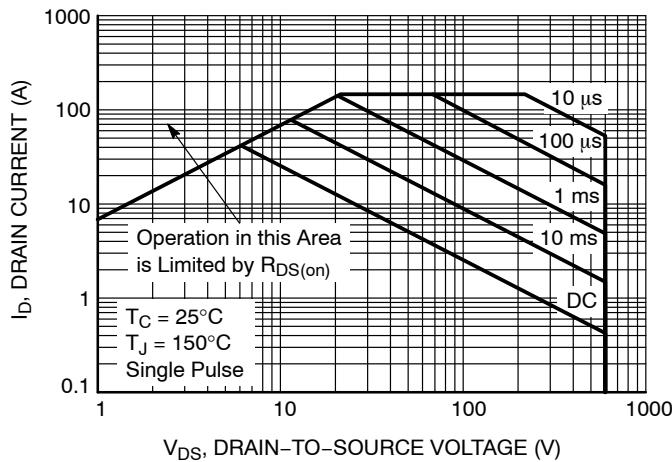
## TYPICAL CHARACTERISTICS



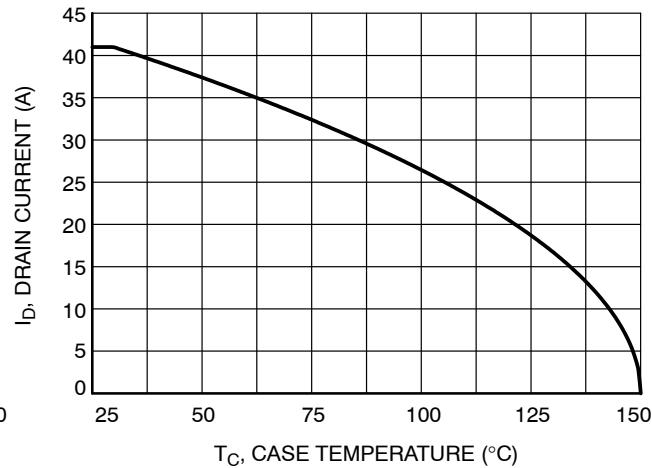
**Figure 7. Breakdown Voltage Variation vs. Temperature**



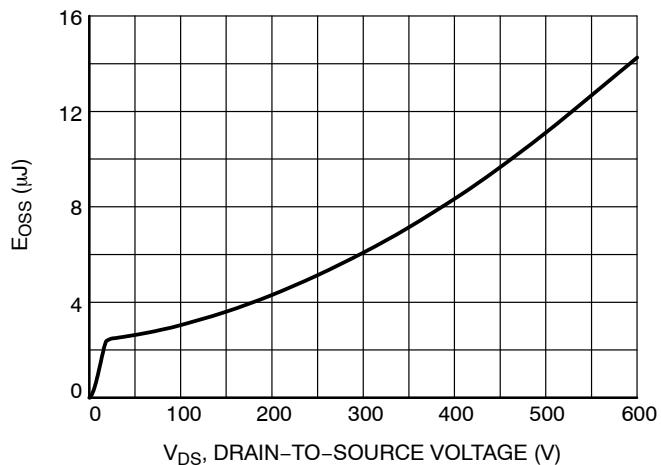
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. E<sub>oss</sub> vs. Drain-to-Source Voltage**

# NTMT061N60S5F

## TYPICAL CHARACTERISTICS

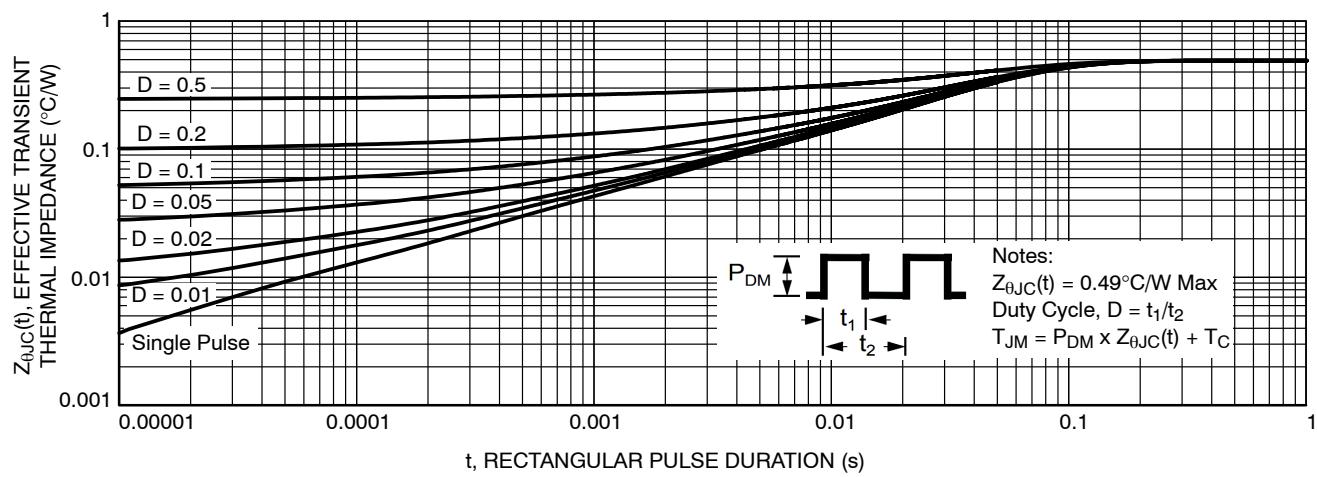


Figure 12. Transient Thermal Impedance

## NTMT061N60S5F

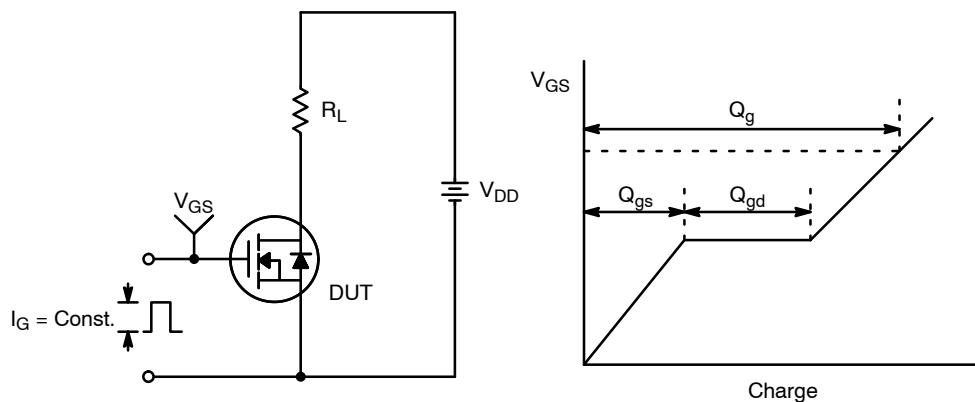


Figure 13. Gate Charge Test Circuit & Waveform

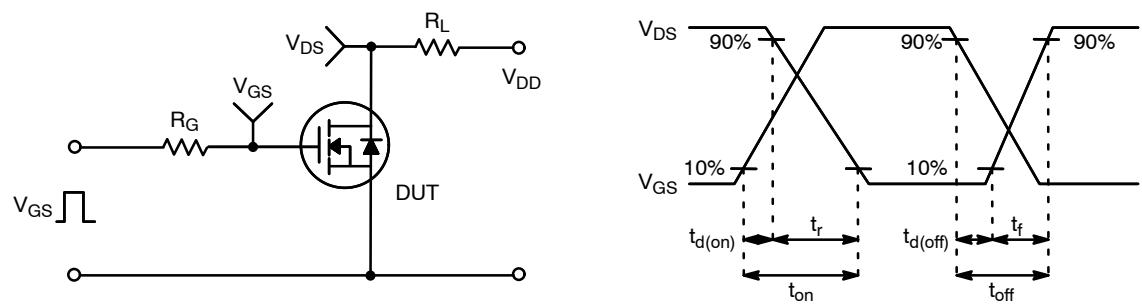


Figure 14. Resistive Switching Test Circuit & Waveforms

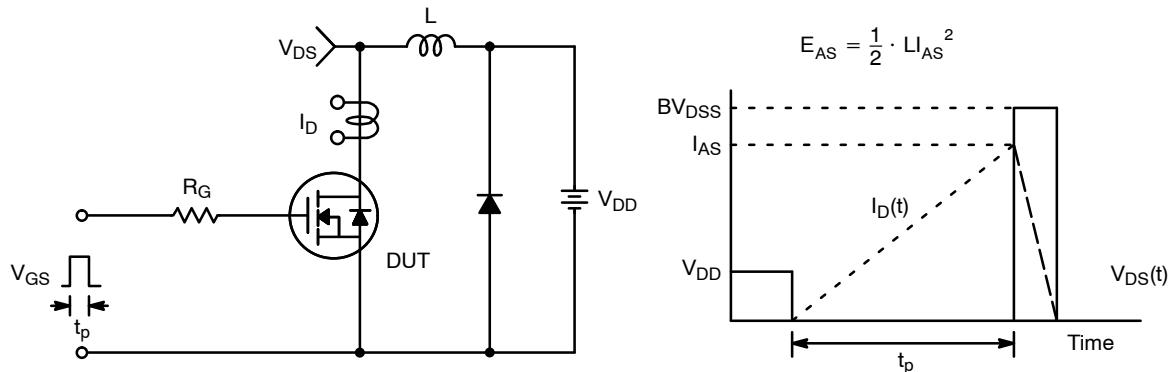


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

## NTMT061N60S5F

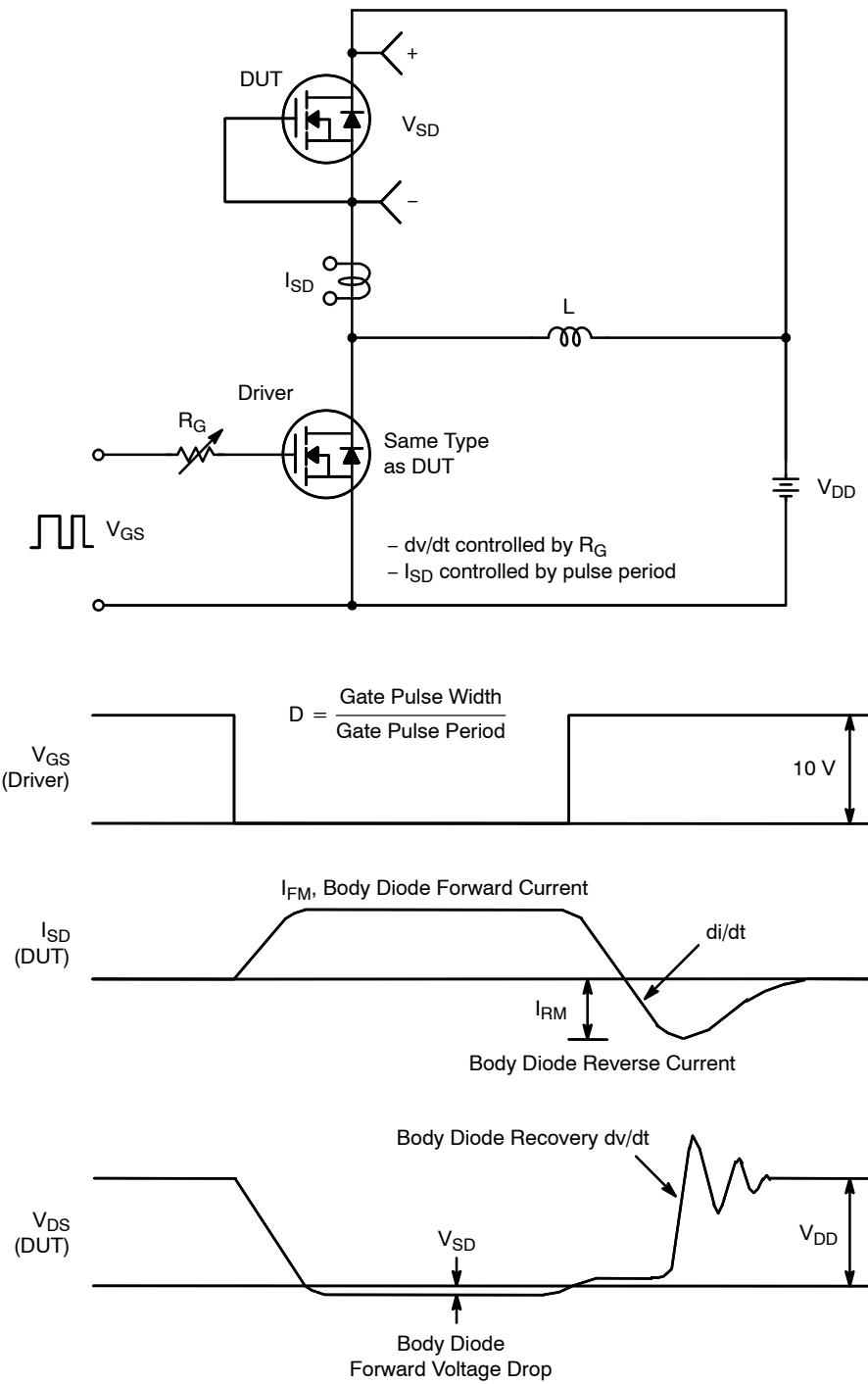
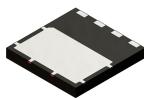


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

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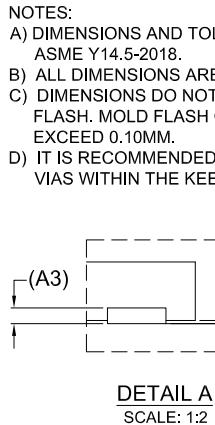
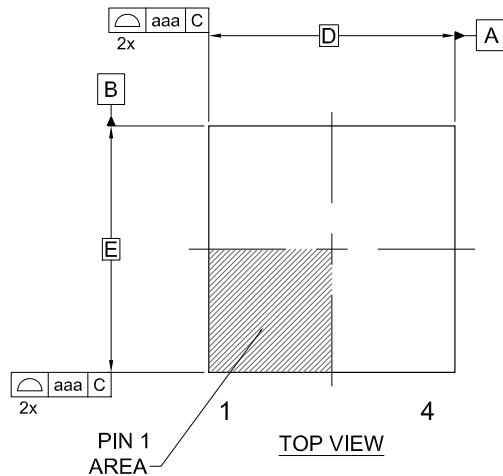
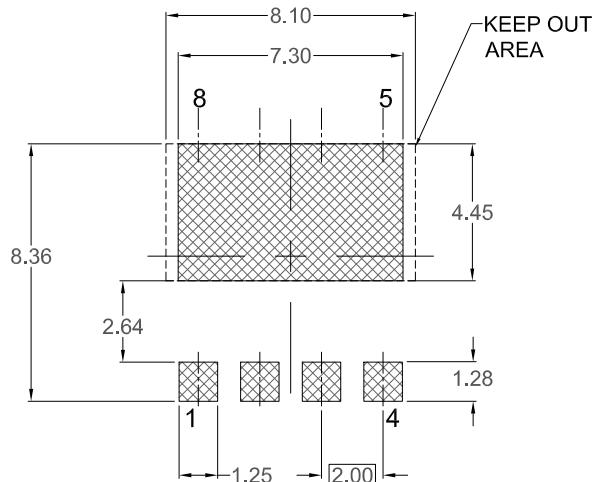
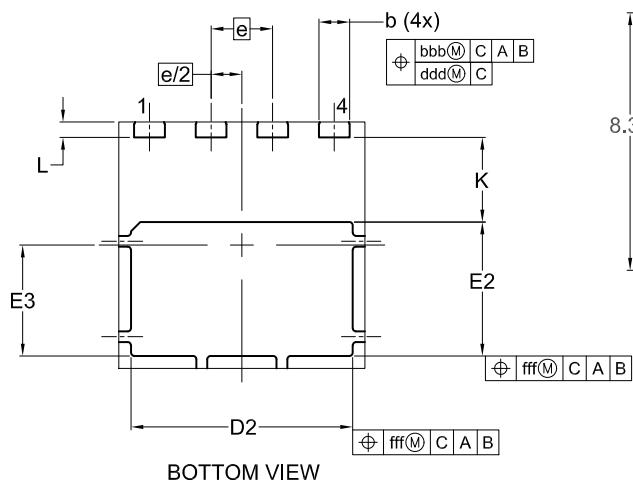
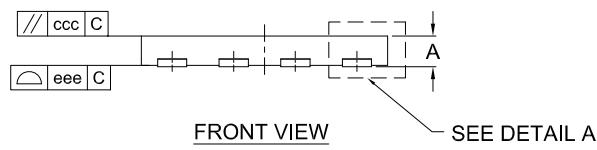


## TDFN4 8.00x8.00x1.00, 2.00P

CASE 520AB

ISSUE A

DATE 07 JUN 2024

DETAIL A  
SCALE: 1:2

## RECOMMENDED LAND PATTERN

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PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ONSEMI SOLDERING  
AND MOUNTING TECHNIQUES REFERENCE  
MANUAL, SODERRM/D.

GENERIC  
MARKING DIAGRAM\*

XXXX = Specific Device Code

A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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