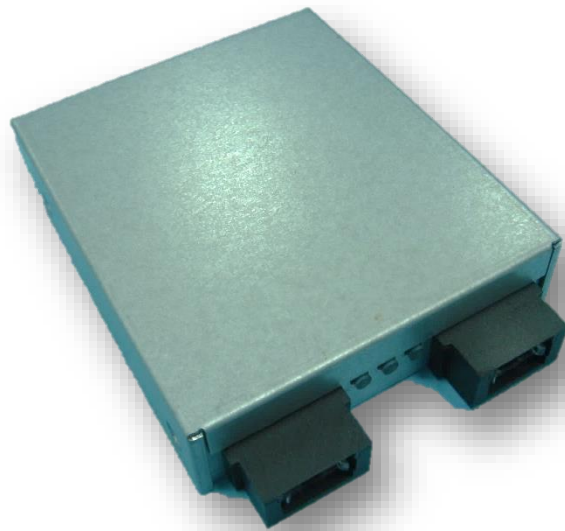


Specification

Dual QSFP+40GBase-SR4 Optical Bypass Module



O B M – D 3 Q H 2 – B 0 1
(With Tx Disable)

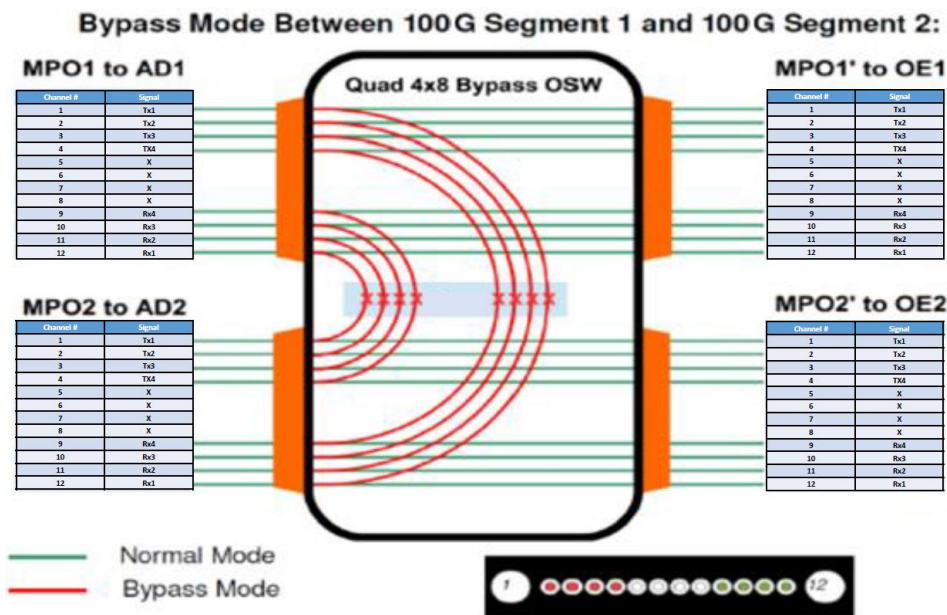
■ Product Overview

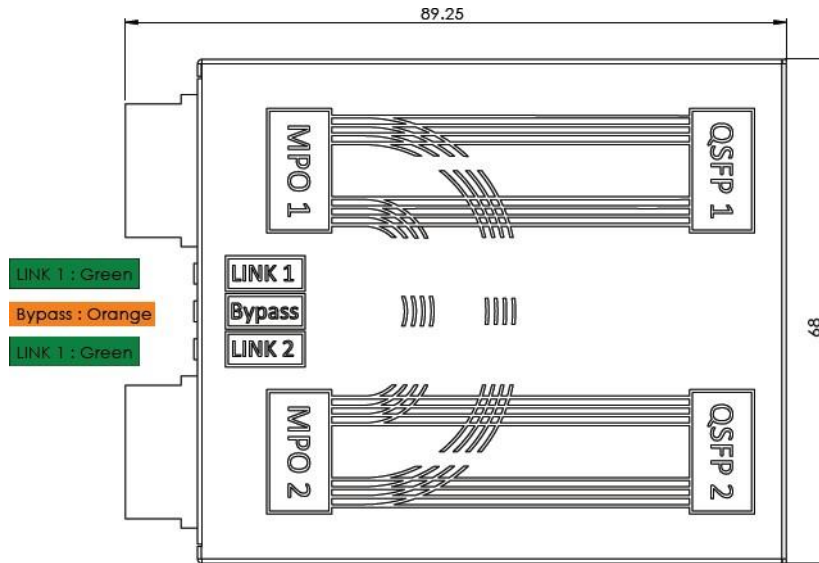
FormericaOE dual QSFP+,40G Base-SR4 (2*40G) Optical Bypass Module (OBM) is a compact box that contains two QSFP+,40G Base-SR4 optical transceivers and optical switches control circuit board. It can be integrated with I/O ports controllers in a Network Interface Card (NIC). The FormericaOE dual QSFP+,40G Base-SR4 OBM is targeted to inline network system that maintains network connectivity when power failure occurs or system fails, particularly for Data Centers that employ extensive QSFP+,40G Base-SR4 for optical inter connects between servers and switches. FormericaOE Dual QSFP+,40G Base-SR4 OBM supports normal and bypass modes, and can be controlled to perform the block mode. In normal mode, the ports are independent interfaces. In bypass mode, all packets received from one port are transmitted to the adjacent port. In block mode, the module blocks the route. FormericaOE Dual QSFP+,40G Base-SR4 OBM can bypass or block its I/O ports on a host system failure, power off, or upon software request. It can be integrated with any brand of CPU controller. It is suitable for connecting with in-line equipment for power failure or system maintenance. When the in-line unit is not on or is in bypass mode, the relays within the OBM are set to bridge the optical signals directly through the optical switch, completely bypassing the in-line equipment. If the in-line equipment is operating normally, then it supplies power to the switch through a high speed connector PIN. Compact and competitive cost, this module provides excellent performance on your network.

Features

- Reliable Passive Fiber Bypass (Latching)
- Low Return Loss
- Available in 50/125µm Multi Mode Fiber
- PCB Mountable Type
- Fast Ethernet Standard Compliant
- Digital Diagnostic SFF-8472 Rev.10.2 Compliant
- SONET/SDH Standard Compliant
- Two MPO-MT Adapter
- Compliant with CE& FCC Standard
- Compact Format and RoHS Compliant

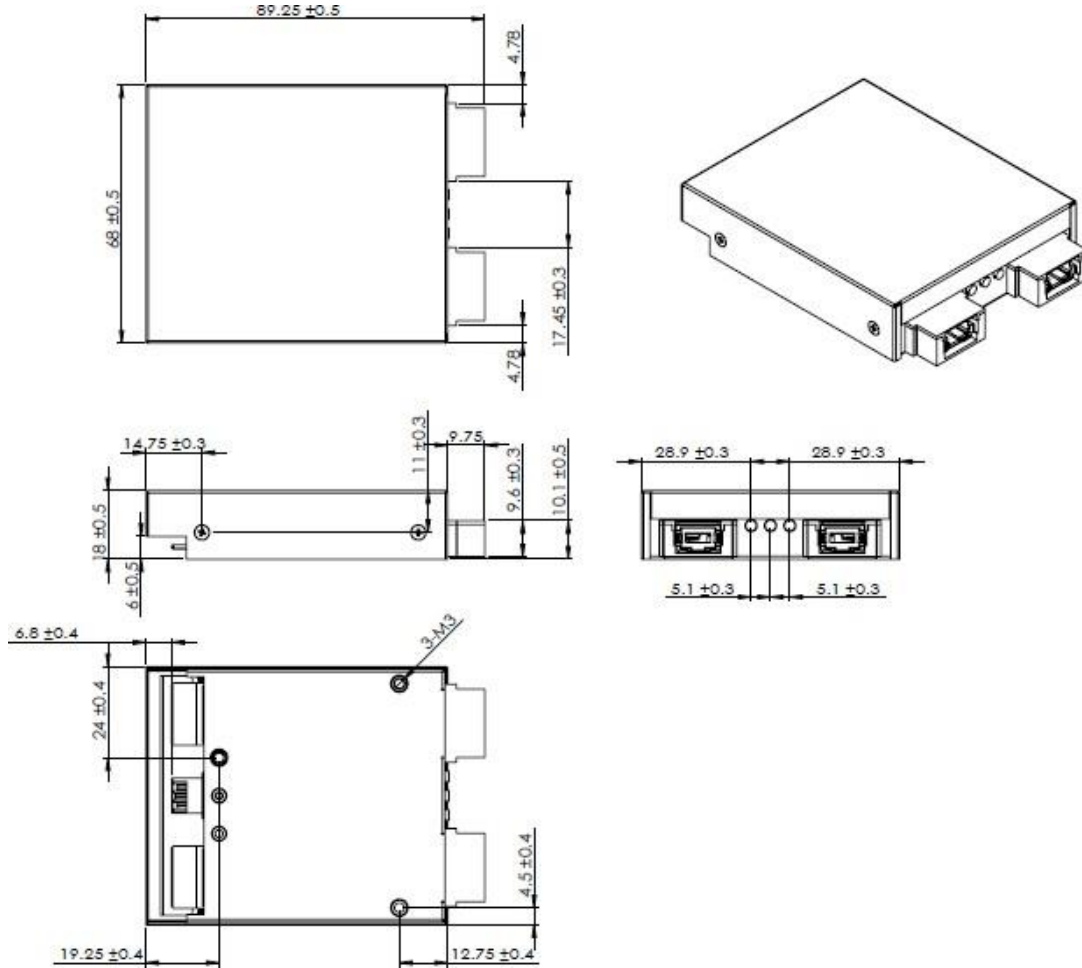
Block Diagram and Optical Paths





- Link1 and Link2 indications:
Green: Link
- Bypass indications:
Orange: Data Rate 40G

■ Module Outline Drawing (mm)



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Ts	-40		85	°C
Supply Voltage	Vcc	0		5	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Top	0		70	°C	1
+5.0V Supply Voltage	Vcc5	4.75		5.25	V	
+3.3V Supply Voltage	Vcc3	3.10		3.50	V	
Relative Humidity (non condensation)		5		85	%	
Data Rate		2.5		10.3125	Gbps	

Note1: Please see order information

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
+5.0V Supply Current	I _{CC5}			100	mA	
+3.3V Supply Current	I _{CC3}			1200	mA	
Transmitter (Each QSFP)						
Transmitter Differential Input Voltage	V _{DT}	175		1600	mV	1
Transmitter Disable Input-High	V _{DISH}	2		V _{CC} +0.3	V	
Transmitter Disable Input-Low	V _{DISL}	-0.3		0.8	V	
Transmitter Fault Pull up Resistor	R _{TX FAULT}	4.7		10	KΩ	2
Transmitter Fault Output-High	V _{TXFH}	2.4		V _{CC}	V	2
Transmitter Fault Output-Low	V _{TXFL}	0		0.5	V	2
Receiver (Each QSFP)						
Receiver Differential Output Voltage	V _{DR}	200		900	mV	3
Receiver LOS Load	RRXLOS	4.7		10	KΩ	2
LOS Output Voltage-High	V _{LOSH}	2.4		V _{CC}	V	2
LOS Output Voltage-Low	V _{LOSL}	0		0.5	V	2
Optical Switch						
Latching Voltage-High	V _{LATH}	4.75	5	5.25	V	
Latching Voltage-Low	V _{LATL}	0		0.8	V	
Latching Resistance	R _{LAT}		125		Ω	

Notes:

1. Internally AC coupled and terminated to 100Ω differential load.
2. Pull up to V_{CC} on Host Board.
3. Internally AC coupled, but requires a 100Ω differential termination at or internal to Serializer/Deserializer.

Optical Characteristics

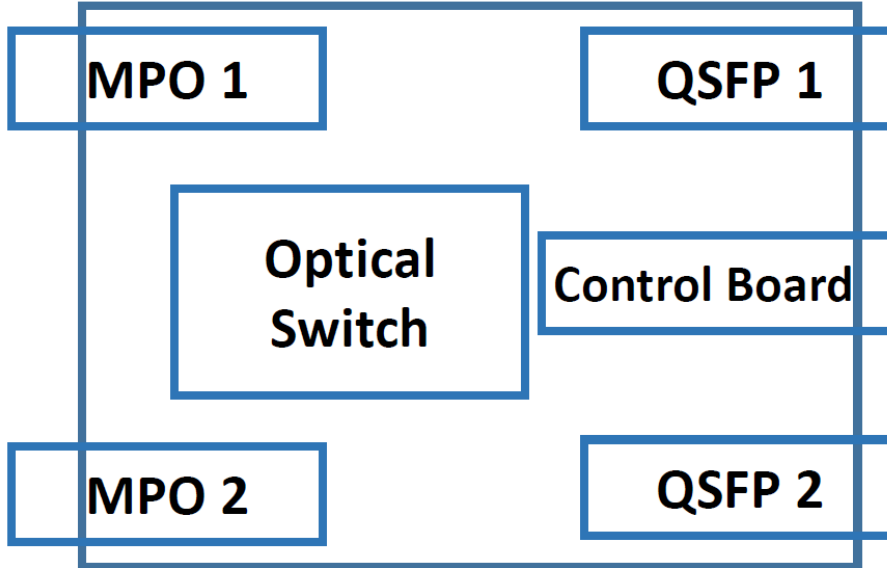
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Output Optical Power (Avg.)	P _O	-7.6		2.4	dBm	1
Optical Extinction Ratio	ER	3			dB	
Center Wavelength	λ	840	850	860	nm	
Spectral Width (RMS)	σλ			0.65	nm	
Receiver						
Stress Receiver Sensitivity (Avg.)	P _{IN}			-5.4	dBm	1,2
Input Optical Wavelength	λ	840		860	DBm	
LOS-Deasserted	P _A			-7.5	dBm	
LOS-Asserted	P _D	-30			dBm	
LOS-Hysteresis	P _A - P _D	0.5			dB	
Optical Switch						
Wavelength Range	λ	670		980	nm	
Insertion Loss	OIL		0.35	3.2	dB	
Return Loss	ORL	30			dB	
Switch Time				8	ms	
Lifetime			≥ 10 ⁷		times	
Latching Resistance	R _{LAT}		125		Ω	

Notes:

1. Normal Mode (Bypass off).
2. The sensitivity provided at a BER of 1×10⁻¹² or better with an input signal consisting of 10.3125Gb/s, 2³¹-1 PRBS

■ Block Diagram For 2x40G OBM

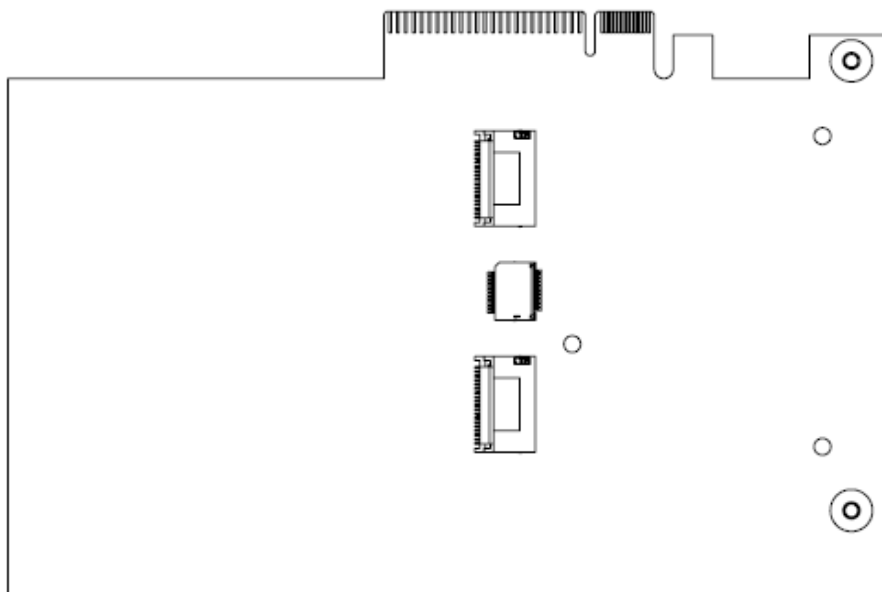
Top View



■ Host Board Connector

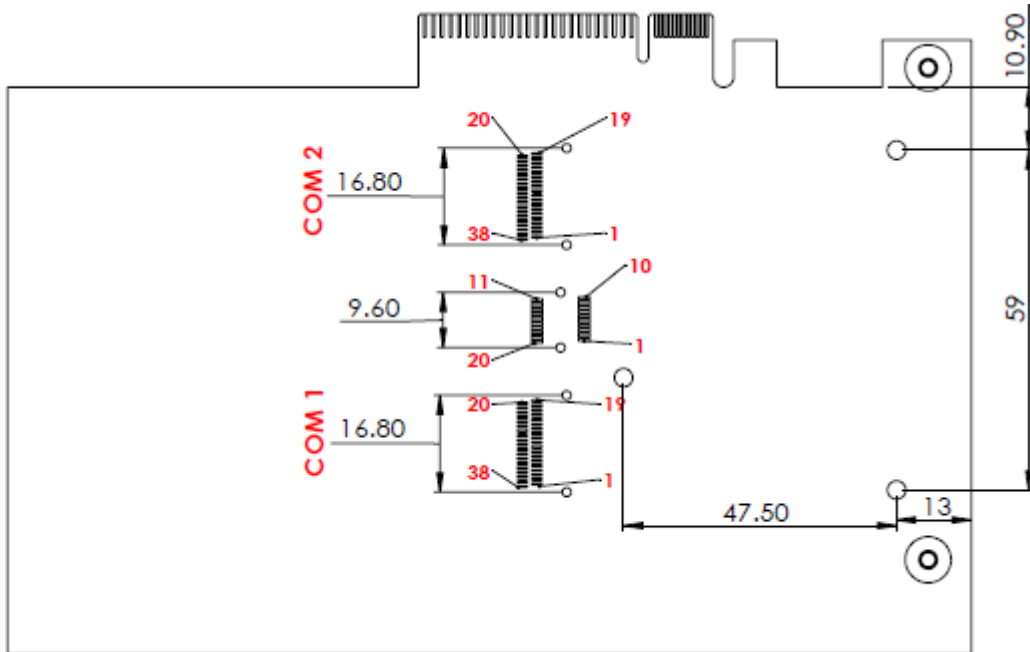
Top View

QSFP Connector x 2
SFP Connector x 1



COM 1 & COM 2 Module Pad Assignments

Top View



38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMODE
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	Rx4p
24	Rx4n
23	GND
22	Rx2p
21	Rx2n
20	GND

Top Side
Viewed From Top

Module Card Edge

1	GND
2	TX2n
3	TX2p
4	GND
5	TX4n
6	TX4p
7	GND
8	ModSelL
9	ResetL
10	VccRx
11	SCL
12	SDA
13	GND
14	Rx3p
15	Rx3n
16	GND
17	Rx1p
18	Rx1n
19	GND

Bottom Side
Viewed From Bottom

COM 1 & COM 2 Pin Definition

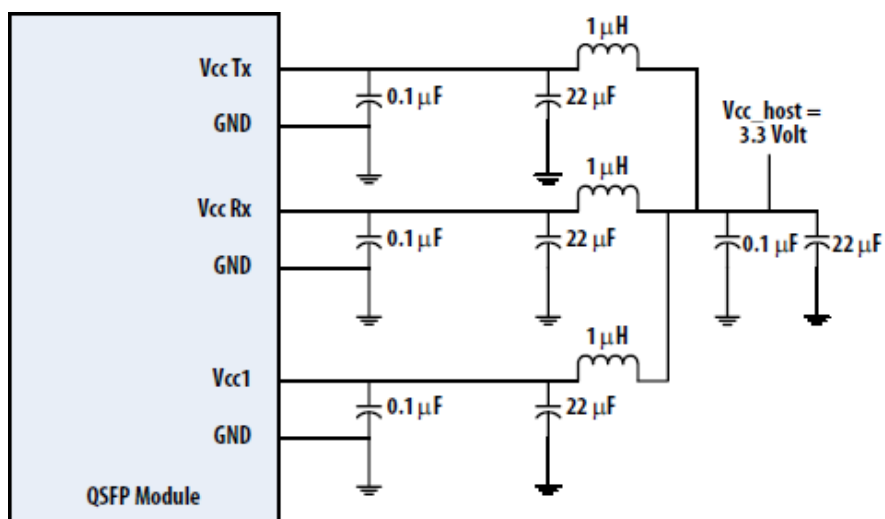
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTTL-I	ModSelL	Module Select	3	
9	LVTTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	2
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTTL-O	ModPrsL	Module Present	3	
28	LVTTTL-O	IntL	Interrupt	3	

29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note:

- GND** is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
- Vcc Rx, Vcc1 and Vcc Tx** are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Figure. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

Recommended Host Board Power Supply Circuit



Control Board Pin Definition

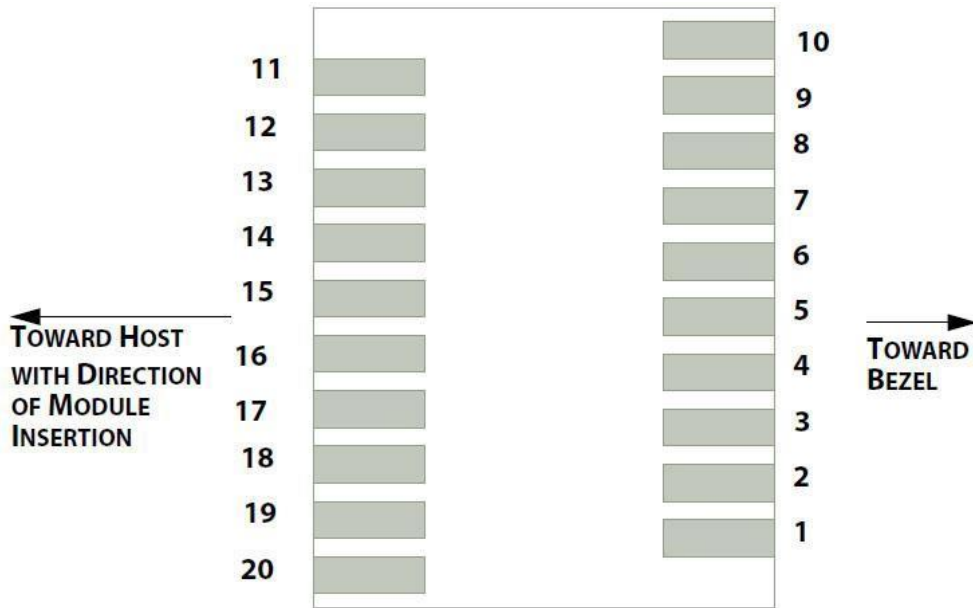


Figure: Module Interface to Host

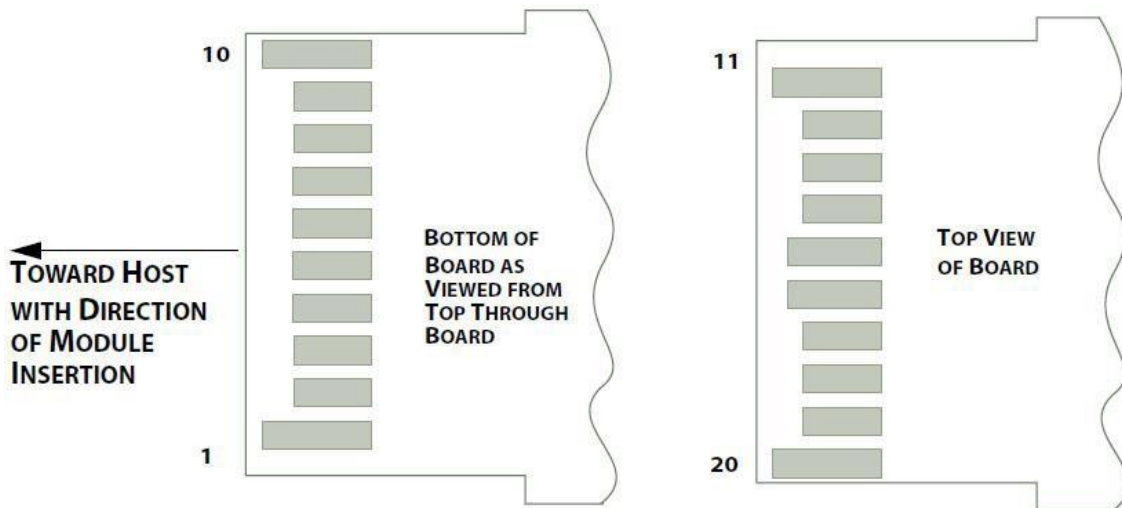
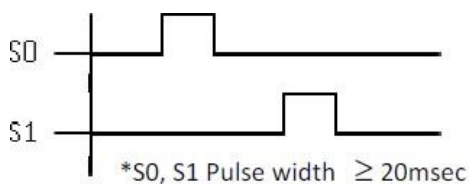


Figure: Module Contact Assignment

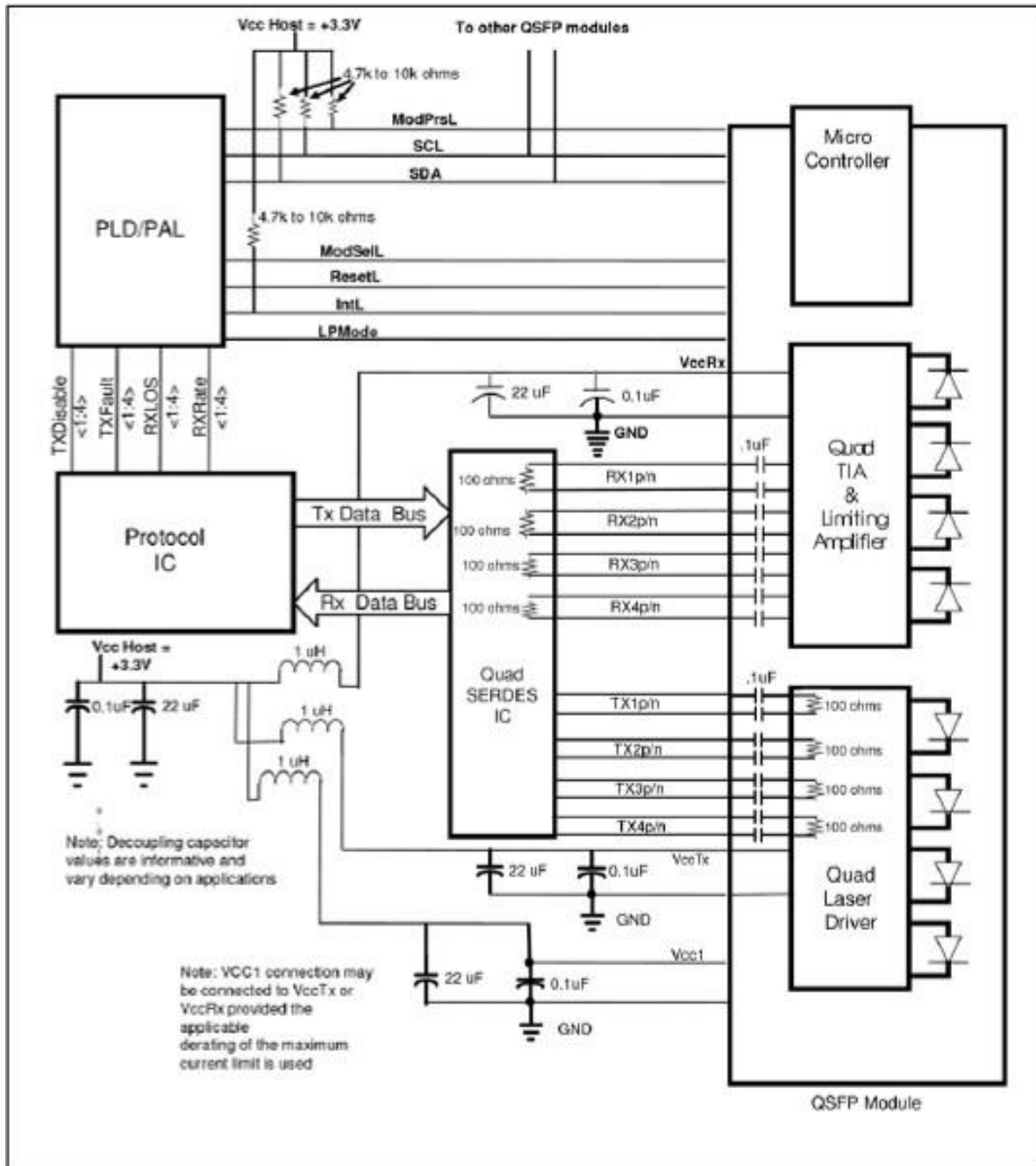
Control Board Pin Descriptions

Pin	Name	Pin Type	Description
1	GND	GND	Ground
2	MON1	Output/LVTTL	Status of Optical Switch 1
3	MON2	Output/LVTTL	Status of Optical Switch 2
4	MON3	Output/LVTTL	Status of Optical Switch 3
5	MON4	Output/LVTTL	Status of Optical Switch 4
6	MOD_ABS	Output/LVTTL	Module absent indicator. It is connected to the module ground. (0: Module present, 1: Module absent)
7	VCC	PWR	5.0V power supply
8	S0	Input/LVTTL	Change the Optical Switch status
9	S1	Input/LVTTL	Change the Optical Switch status
10	GND	GND	Ground
11	GND	GND	Ground
12	LINK 2 LED_CTL	Input/LVTTL	Green Color; LED Control - LED1: 3.3V = right on, 0V = right off. (Note 1.) ; Indicate the normal mode of 1st QSFP+
13	Bypass LED_CTL	Input/LVTTL	Orange Color; LED Control - LED2: 3.3V = mid on, 0V = mid off. (Note 1.) ; Indicate the bypass mode
14	LINK 1 LED_CTL	Input/LVTTL	Green Color; LED Control - LED3: 3.3V = left on, 0V = left off. (Note 1.) ; Indicate the normal mode of 2 nd QSFP+
15	VCC	PWR	3.3V power supply
16	VCC	PWR	3.3V power supply
17	LED4_CTL	Input/LVTTL	Control ON/OFF of LED4. (0:Turn ON, 1: Turn OFF)
18	LED5_CTL	Input/LVTTL	Control ON/OFF of LED5. (0:Turn ON, 1: Turn OFF)
19	NC	NC	No Connection
20	GND	GND	Ground

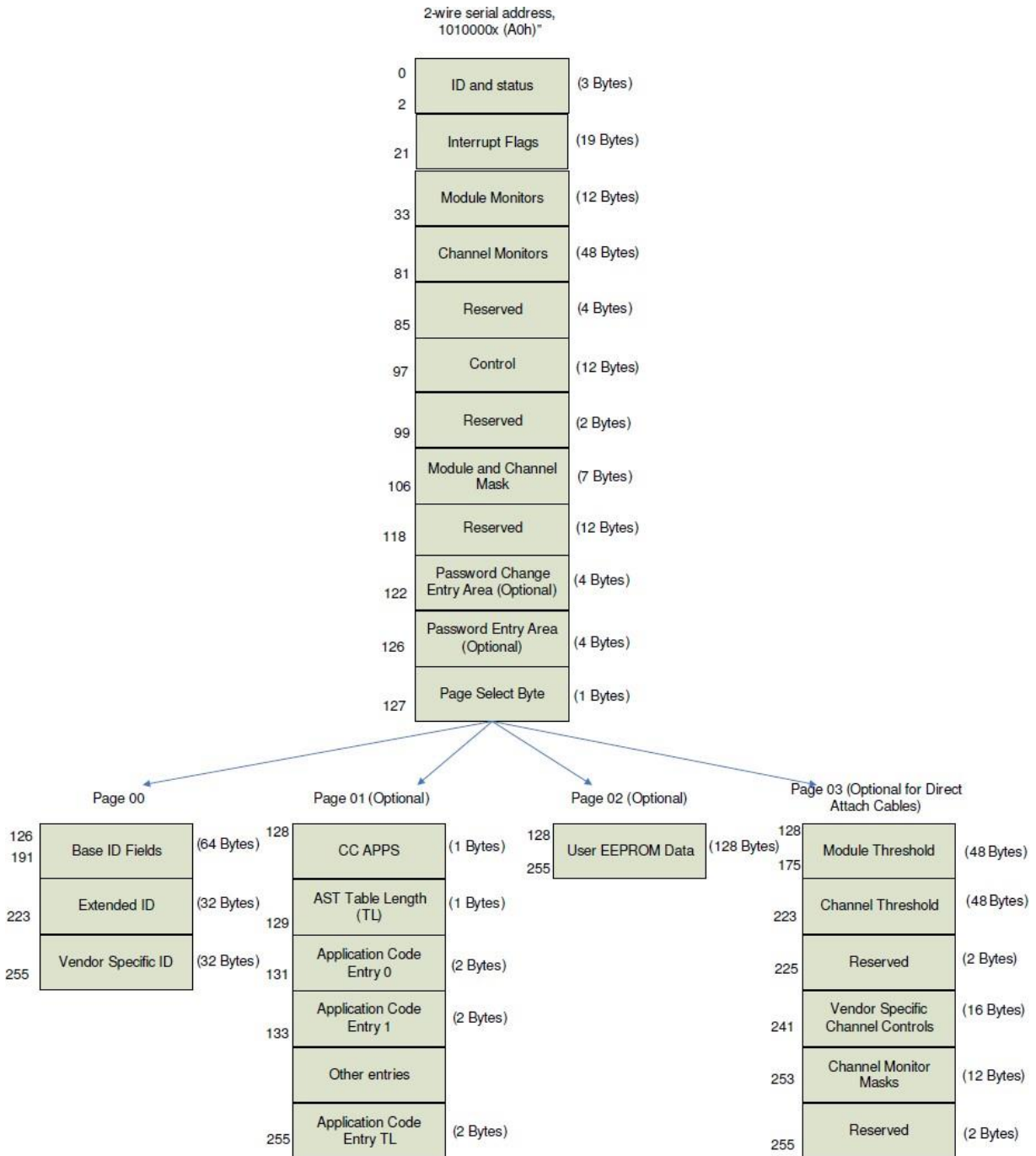


S0 = High, S1 = Low. To change the OSW state to ON state.
S0 = Low, S1 = High. To change the OSW state to OFF state.

Recommended Interface Circuit



Memory Map



■ ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

■ LASER Safety

This is a Class 1 Laser Product according to IEC/EN60825-1:2014 (Third Edition). This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 56, dated MAY 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Attention: L'utilisation de commandes ou de réglages ou l'exécution de procédures autres que celles spécifiées dans le document peut entraîner une exposition à des radiations dangereuses.

■ **Contact Information**

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inquiry@formericaoe.com www.formericaoe.com	

Revision History

Date	Version	Description of Changes
11/24/2017	1.1	Optical Switch of Insertion Loss < 3.2
03/04/2019	1.2	1. Footer style change. 2. Contact information has been added on the last page.
08/07/2019	1.3	Add product LED image on Page.4
07/30/2020	1.4	Modify mechanical tolerance
01/17/2024	2.0	Modify Pin 7, 12, 13 & 14 description of control board on page 14