

3 DIMM Buffer

General Description

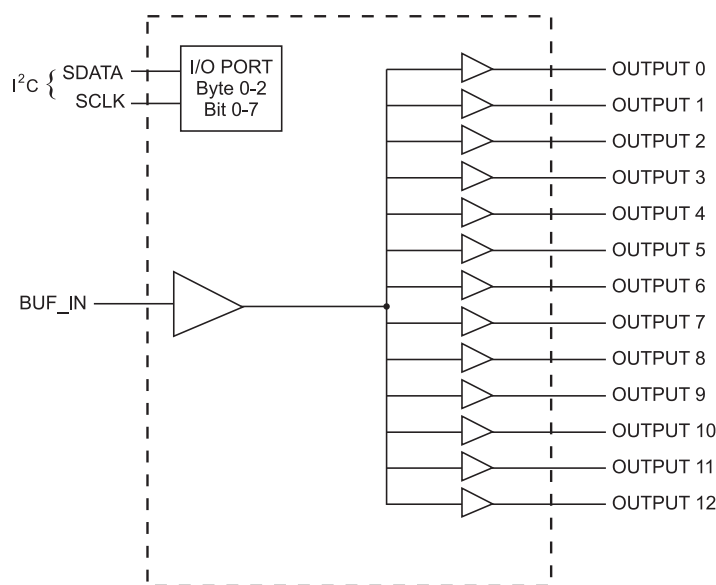
The ICS9179-12 is a buffer intended for reduced pin count 2 - chip Intel BX chipset designs

An I²C interface is included, enabling individual outputs to be turned on or off. With 13 outputs, up to 3 DIMMs are supported.

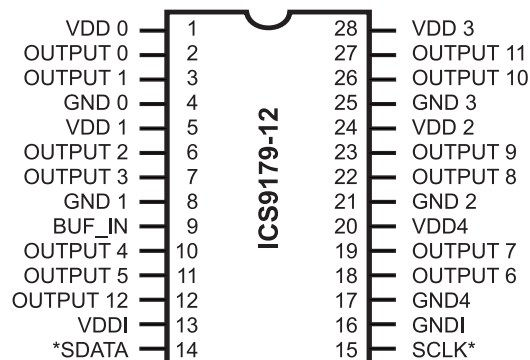
Features

- Thirteen high speed, low noise buffers, supports up to three SDRAM DIMMs.
- Buffer outputs skew matched to within 250 ps.
- I²C Serial Configuration interface to allow individual OUTPUTs to be stopped low.
- Multiple VDD, VSS pins for noise reduction
- 3.3V±5% supply voltage
- 28-pin SOIC and SSOP package
- Propagation delay between 1 to 5.5ns
- Operation to 133MHz at 3.3V±5%

Block Diagram



Pin Configuration



28-Pin SOIC and SSOP

* Internal pull-up resistor of 100K Ohms to 3.3V on indicated inputs

Power Groups

VDD (0:4), GND (0:4) = Power supply for OUTPUT buffer

VDDI, GNDI = Power supply for I²C circuitry

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 3, 6, 7, 10, 11, 12, 18, 19, 22, 23, 26, 27	OUTPUT (0:12)	OUT	Clock outputs ¹
9	BUF_IN	IN	Input for buffers
14	SDATA	I/O	Data pin for I ² C circuitry ³
15	SCLK	I/O	Clock pin for I ² C circuitry ³
1, 5, 20, 24, 28	VDD (0:4)	PWR	3.3V Power supply for OUTPUT buffers
4, 8, 17, 21, 25	GND (0:4)	PWR	Ground for OUTPUT buffers
13	VDDI	PWR	3.3V Power supply for I ² C circuitry and internal logic
16	GNDI	PWR	Ground for I ² C circuitry and internal logic

Notes:

1. At power up all thirteen OUTPUTs are enabled and active.
2. OE has a 100K Ohm internal pull-up resistor to keep all outputs active.
3. The SDATA and SCLK inputs both have internal pull-up resistors with values above 100K Ohms.

Technical Pin Function Descriptions

VDD

This is the power supply to the internal core logic of the device as well as the clock output buffers for OUTPUT (0:12).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

GND

This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

OUTPUT (0:12)

These Output Clocks are used to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the OUTPUTs output is controlled by the supply voltage that is applied to VDD of the device, operates at 3.3 volts.

I²C

The SDATA and SCLOCK Inputs are used to program the device. The clock generator is a slave-receiver device in the I²C protocol. It will allow read-back of the registers. See configuration map for register functions. The I²C specification in Philips I²C Peripherals Data Handbook (1996) should be followed.

BUF_IN

Input for Fanout buffers (OUTPUT 0:12).

VDDI

This is the power supply to I²C circuitry.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 _(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 6**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 _(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification.
Read-Back will support Intel PIIX4 "Block-Read" protocol.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

0264E—12/09/08

Serial Configuration Command Bitmaps

Byte 0: OUTPUT Clock Register (Default=0)

BIT	PIN#	PWD	DESCRIPTION
Bit7	11	1	OUTPUT5
Bit6	10	1	OUTPUT4
Bit5	-	1	Reserved
Bit4	-	1	Reserved
Bit3	7	1	OUTPUT3
Bit2	6	1	OUTPUT2
Bit1	3	1	OUTPUT1
Bit0	2	1	OUTPUT0

Byte 1: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	27	1	OUTPUT11 (Act/Inact)
Bit 6	26	1	OUTPUT10 (Act/Inact)
Bit 5	23	1	OUTPUT9 (Act/Inact)
Bit 4	22	1	OUTPUT8 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	19	1	OUTPUT7 (Act/Inact)
Bit 0	18	1	OUTPUT6 (Act/Inact)

Byte 2: OUTPUT Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	12	1	OUTPUT12 (Act/Inact)
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Functionality

OE#	OUTPUT (0:13)
0	Hi-Z
1	1 X BUF_IN

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

ICS9279-12 Power Consumption

The values below are estimates of target specifications.

Condition	Max 3.3V supply consumption Max discrete cap loads VDD = 3.465V All static inputs = VDD or GND
No Clock Mode (BUF_IN - VDD1 or GND) I ² C Circuitry Active	3mA
Active 66MHz (BUF_IN = 66.66MHz)	230mA
Active 100MHz (BUF_IN = 100.00MHz)	360mA
Active 133MHz (BUF_IN = 133.33MHz)	500mA

0264E—12/09/08

Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND -0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input & Supply

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V $\pm 5\%$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	uA
Input Low Current	I_{IL}	$V_{IN} = 0$ V; Inputs with no pull-up resistors	-5			uA
	I_{IL}	$V_{IN} = 0$ V; Inputs with 100K pull-up resistors	-60			uA
Operating Supply Current	I_{DD1}	$C_L = 0$ pF; F_{IN} @ 66MHz			120	mA
	I_{DD2}	$C_L = 0$ pF; F_{IN} @ 100MHz			180	mA
	I_{DD3}	$C_L = 0$ pF; F_{IN} @ 133MHz			250	mA
	I_{DD4}	$C_L = 30$ pF; $R_S = 33\Omega$; F_{IN} @ 66MHz			230	mA
	I_{DD5}	$C_L = 30$ pF; $R_S = 33\Omega$; F_{IN} @ 100MHz			360	mA
	I_{DD6}	$C_L = 30$ pF; $R_S = 33\Omega$; F_{IN} @ 133MHz			500	mA
Input frequency	F_i^1	$V_{DD} = 3.3$ V; All Outputs Loaded	10		133	MHz
Input Capacitance	C_{IN}^1	Logic Inputs			5	pF

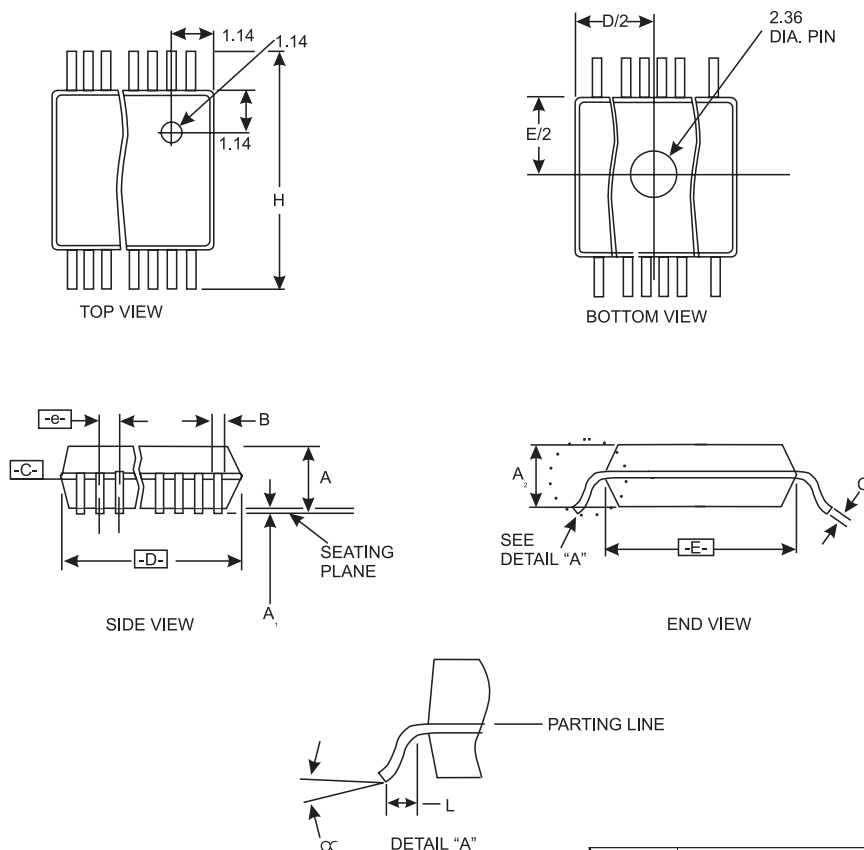
¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Outputs

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$; $C_L = 20 - 30 \text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP}	$V_O = V_{DD}^*(0.5)$	10		24	Ω
Output Impedance	R_{DSN}	$V_O = V_{DD}^*(0.5)$	10		24	Ω
Output High Voltage	V_{OH}	$I_{OH} = -30 \text{ mA}$	2.6			V
Output Low Voltage	V_{OL}	$I_{OL} = 23 \text{ mA}$			0.4	V
Output High Current	I_{OH}	$V_{OH} = 2.0 \text{ V}$			-54	mA
Output Low Current	I_{OL}	$V_{OL} = 0.8 \text{ V}$	40			mA
Rise Time ¹	T_r	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$			1.33	ns
Fall Time ¹	T_f	$V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$			1.33	ns
Duty Cycle ¹	D_t	$V_T = 1.5 \text{ V}$	45		55	%
Skew ¹	T_{sk}	$V_T = 1.5 \text{ V}$			250	ps
Propagation ¹	T_{PROP1}	$V_T = 1.5 \text{ V}$	1		5.5	ns
	T_{PROP2}	$V_T = 50\% \text{ BIN to } 10\% \text{ OUT}$	1		5	ns
	T_{PROPEN}	$V_T = 1.5 \text{ V}$	1		8	ns
	$T_{PROPDIS}$	$V_T = 1.5 \text{ V}$	1		8	ns

¹Guaranteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.068	0.073	0.078	14	0.239	0.244	0.249
A1	0.002	0.005	0.008	16	0.239	0.244	0.249
A2	0.066	0.068	0.070	20	0.278	0.284	0.289
b	0.010	0.012	0.015	24	0.318	0.323	0.328
c	0.004	0.006	0.008	28	0.397	0.402	0.407
D	See Variations			30	0.397	0.402	0.407
E	0.205	0.209	0.212	28 Pin SSOP Package			
e		0.0256 BSC					
H	0.301	0.307	0.311				
L	0.025	0.030	0.037				
N	See Variations						
α	0°	4°	8°				

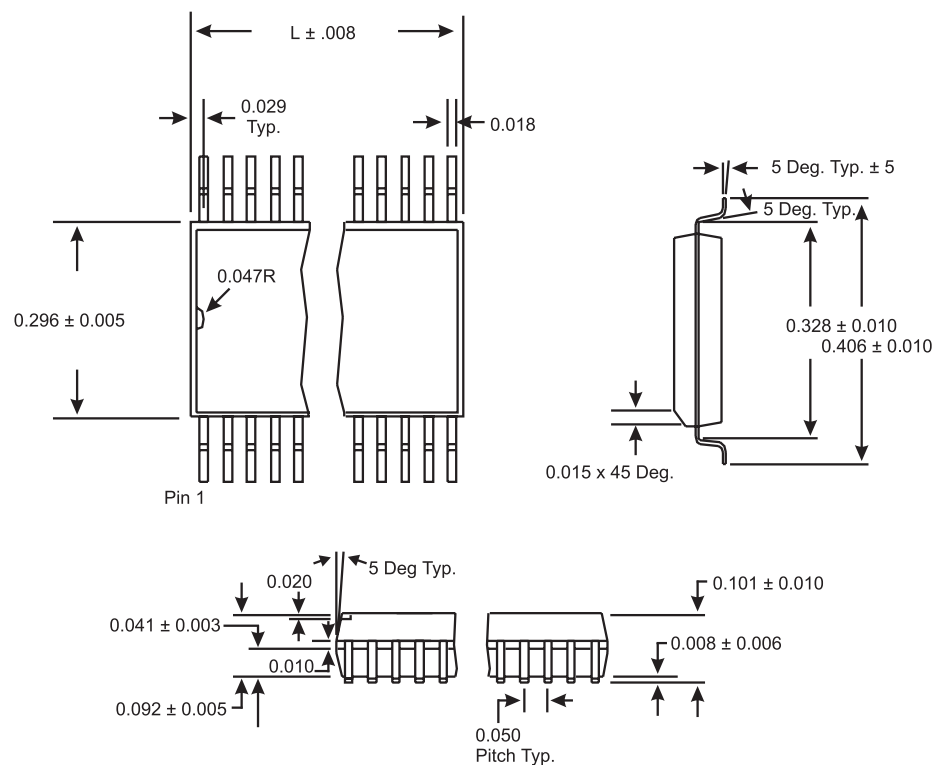
Ordering Information

9179yF-12LFT

Example:

XXXX y F - PPPLFT

- Designation for tape and reel packaging
- Annealed Lead Free (optional, RoHs compliant part)
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Package Type
- F=SSOP
- Revision Designator (will not correlate with datasheet revision)
- Device Type (consists of 3 or 4 digit numbers)



LEAD COUNT	28L
DIMENSIONL	0.704

SOIC Package

Ordering Information

9179yM-12LFT

Example:

XXXX y M - PPPLFT

- Designation for tape and reel packaging
- Annealed Lead Free (optional, RoHs compliant part)
- Pattern Number (2 or 3 digit number for parts with ROM code patterns)
- Package Type
 - M=SOIC
- Revision Designator (will not correlate with datasheet revision)
- Device Type (consists of 3 or 4 digit numbers)

Revision History

Rev.	Issue Date	Description	Page #
E	12/9/2008	Removed ICS prefix from ordering information	8-9

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.