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March 2015

FDD8453LZ

N-Channel PowerTrench® MOSFET

40V, 50A, 6.7mΩ

Features

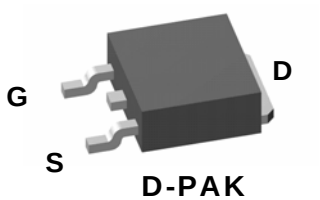
- Max $r_{DS(on)}$ = 6.7mΩ at V_{GS} = 10V, I_D = 15A
- Max $r_{DS(on)}$ = 8.7mΩ at V_{GS} = 4.5V, I_D = 13A
- HBM ESD protection level >7kV typical (Note 4)
- RoHS Compliant

General Description

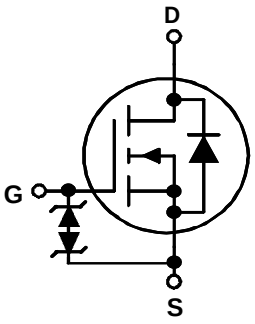
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and switching loss. G-S zener has been added to enhance ESD voltage level.

Applications

- Inverter
- Synchronous Rectifier



D-PAK
(TO-252)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		50	A
	-Continuous (Silicon limited)	T_C = 25°C		75	
	-Continuous	T_A = 25°C	(Note 1a)	16.4	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	253	mJ
P_D	Power Dissipation	T_C = 25°C		65	W
	Power Dissipation	T_A = 25°C	(Note 1a)	3.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8453LZ	FDD8453LZ	D-PAK (TO-252)	13"	16mm	2500 units

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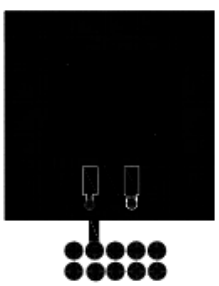
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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		36		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-6.0		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 15A		5.8	6.7	mΩ
		V_{GS} = 4.5V, I_D = 13A		6.8	8.7	
		V_{GS} = 10V, I_D = 15A, T_J = 125°C		9.1	10.6	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 15A		77		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		2640	3515	pF
C_{oss}	Output Capacitance			320	425	pF
C_{rss}	Reverse Transfer Capacitance			190	285	pF
R_g	Gate Resistance	f = 1MHz		2.3		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 15A, V_{GS} = 10V, R_{GEN} = 6Ω		11	19	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			37	58	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V; V_{DD} = 20V, I_D = 15A		46	64	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 5V; V_{DD} = 20V, I_D = 15A		24	33	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20V, I_D = 15A		7		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 20V, I_D = 15A		8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.0A (Note 2)		0.7	1.2	V
		V_{GS} = 0V, I_S = 15A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 15A, di/dt = 100A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			20	32	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 96°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: Starting T_J = 25°C, L = 3mH, I_{AS} = 13A, V_{DD} = 40V, V_{GS} = 10V.

4: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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Typical Characteristics T_J = 25°C unless otherwise noted

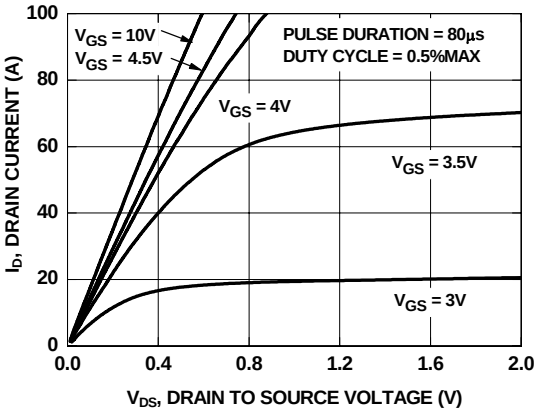


Figure 1. On-Region Characteristics

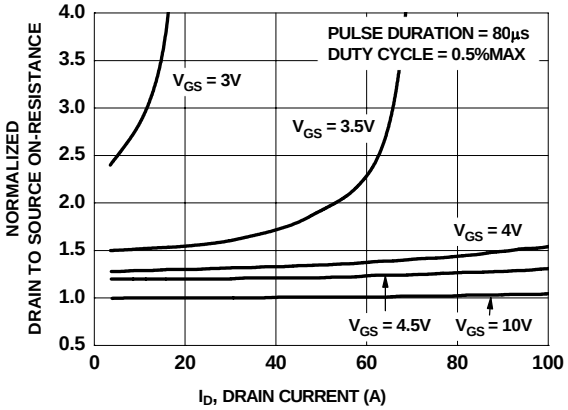


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

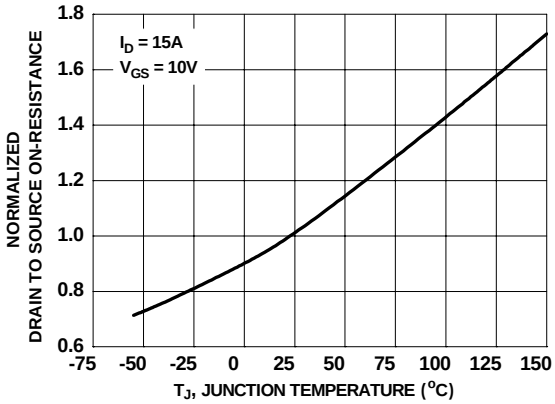


Figure 3. Normalized On-Resistance vs Junction Temperature

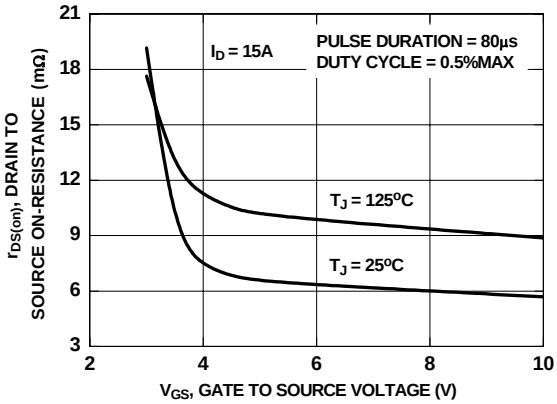


Figure 4. On-Resistance vs Gate to Source Voltage

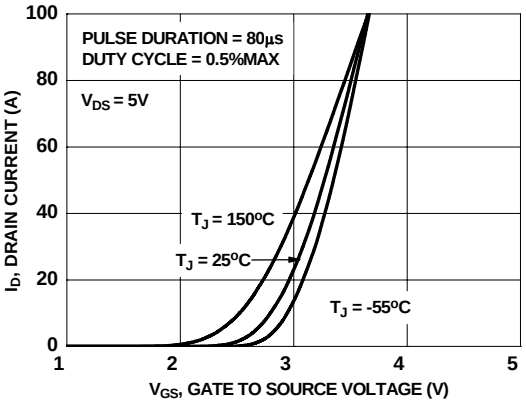


Figure 5. Transfer Characteristics

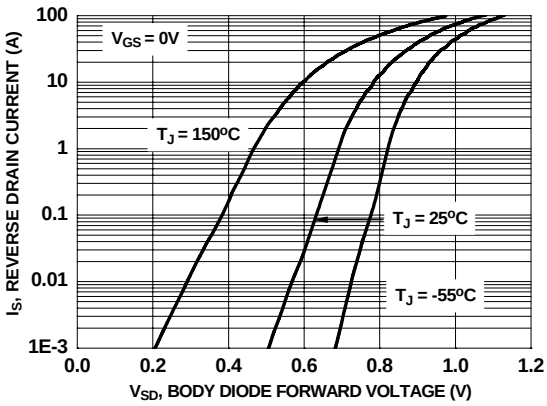


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics T_J = 25°C unless otherwise noted

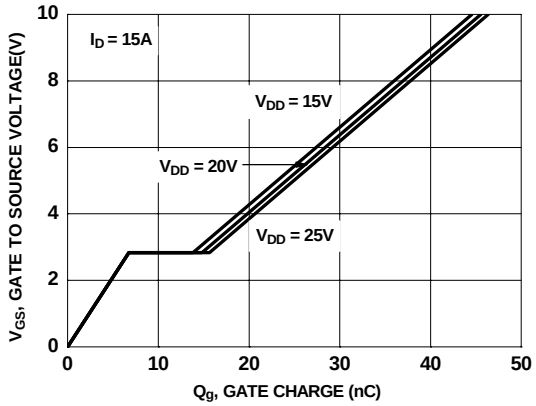


Figure 7. Gate Charge Characteristics

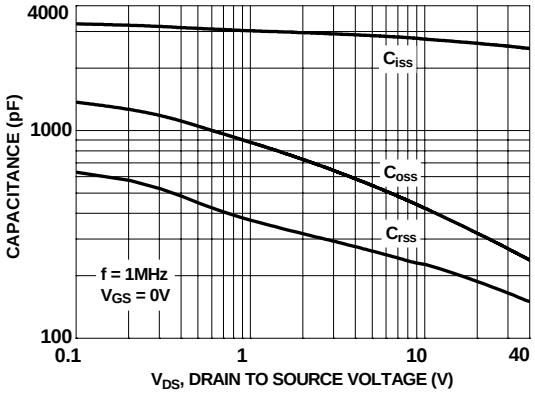


Figure 8. Capacitance vs Drain to Source Voltage

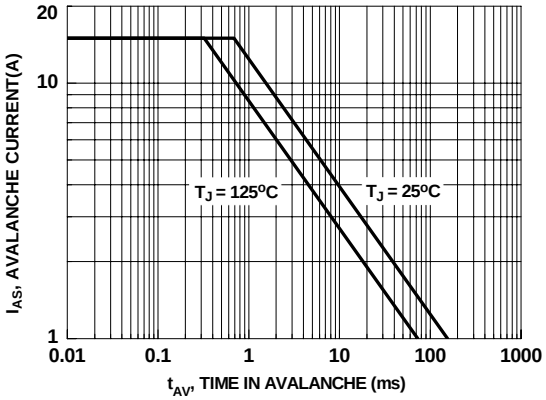


Figure 9. Unclamped Inductive Switching Capability

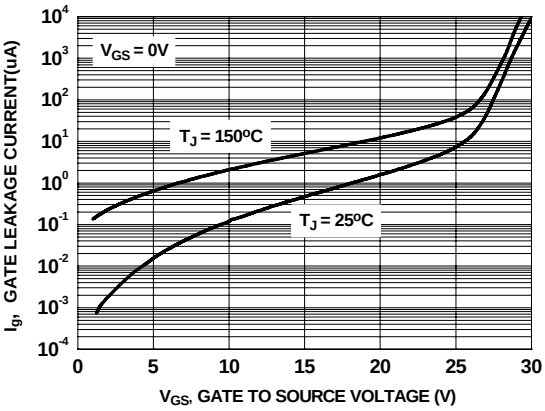


Figure 10. Gate Leakage Current vs Gate to Source Voltage

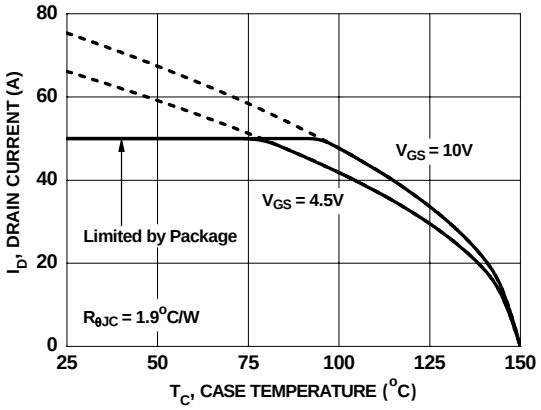


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

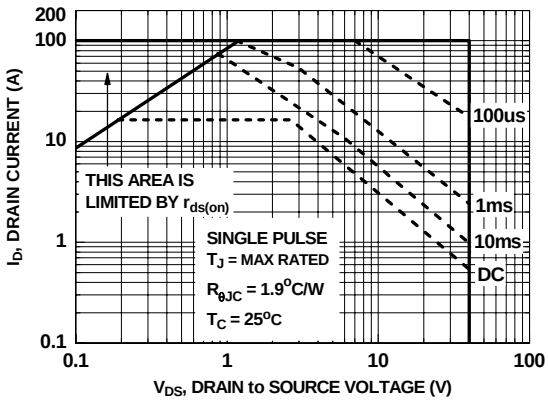


Figure 12. Forward Bias Safe Operating Area

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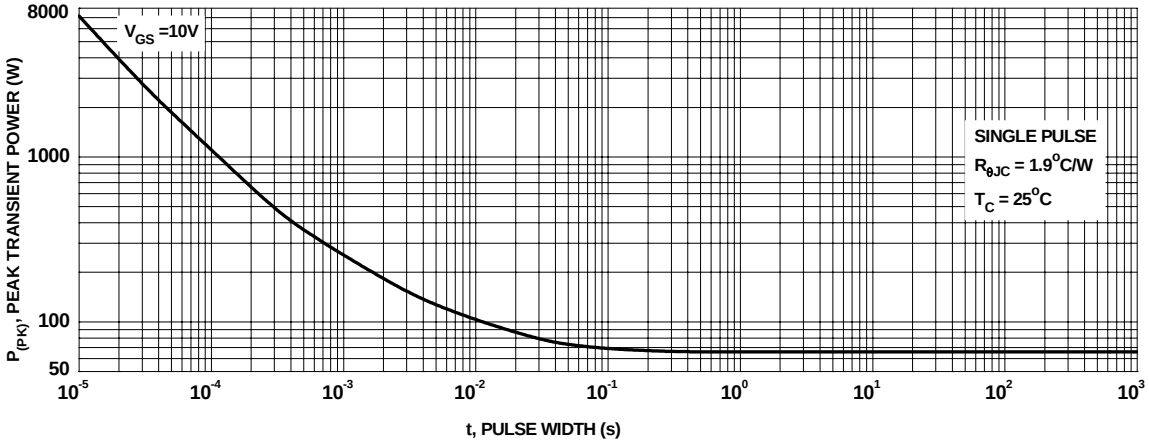


Figure 13. Single Pulse Maximum Power Dissipation

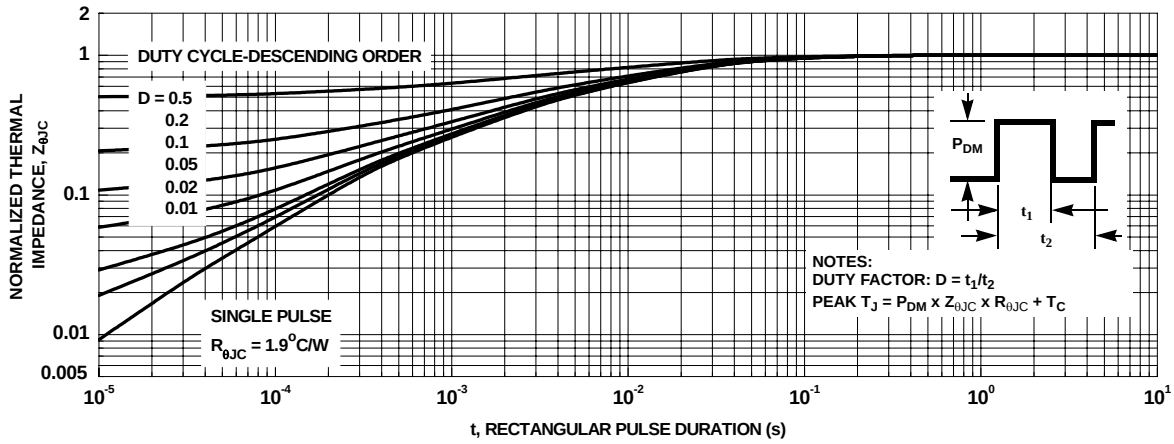


Figure 14. Transient Thermal Response Curve

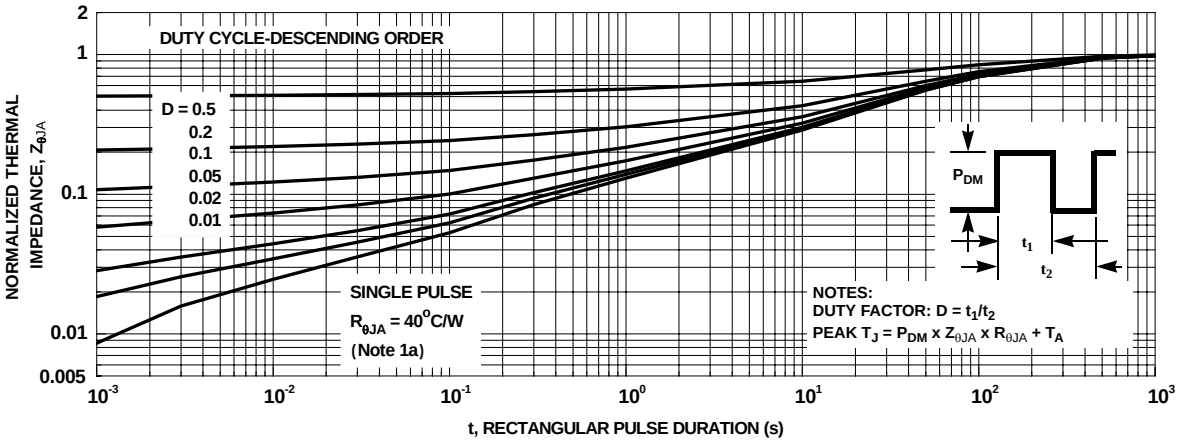


Figure 15. Transient Thermal Response Curve

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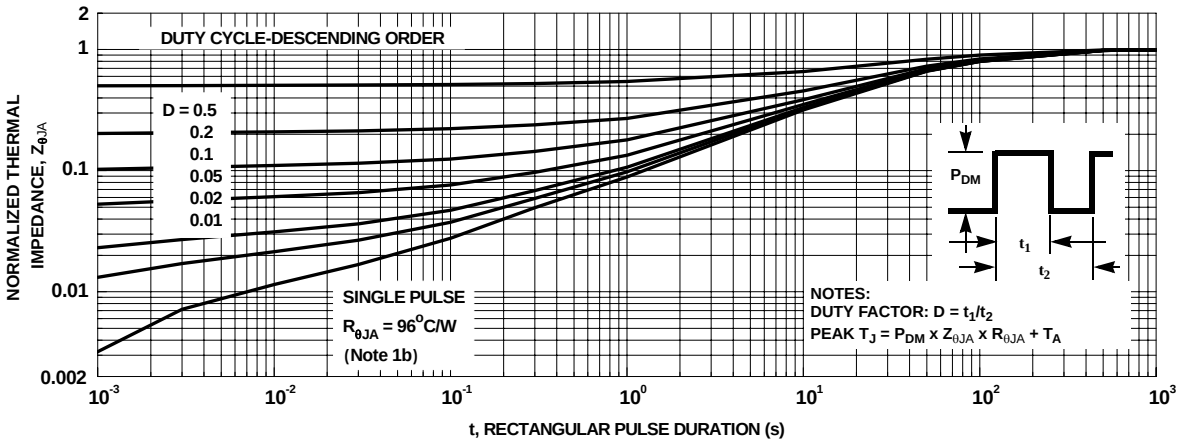
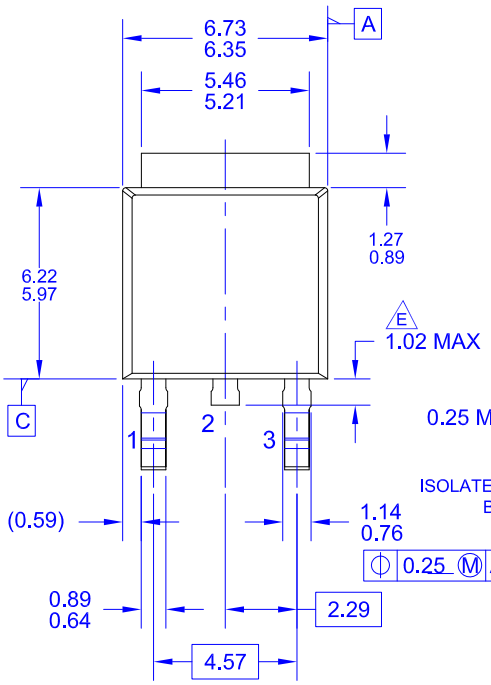
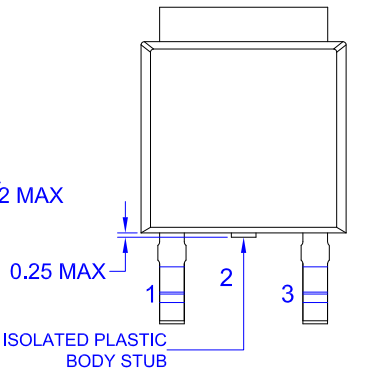


Figure 16. Transient Thermal Response Curve

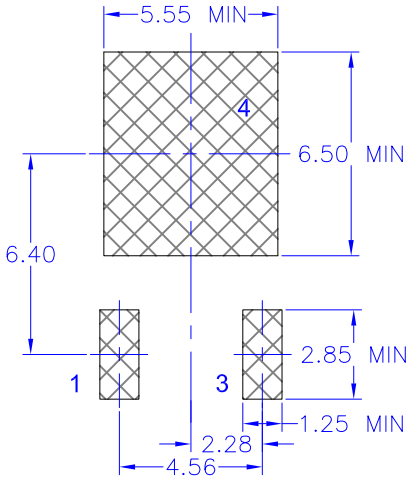
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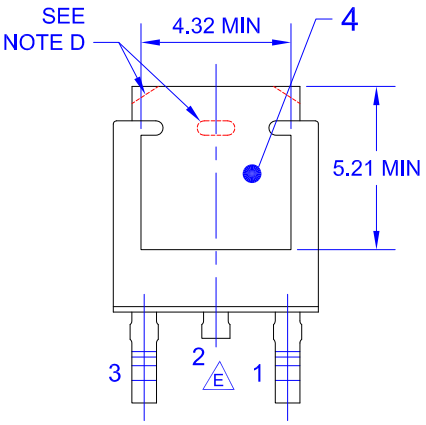
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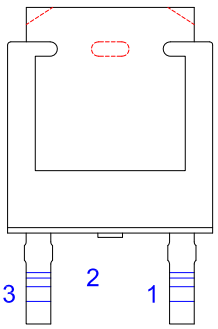
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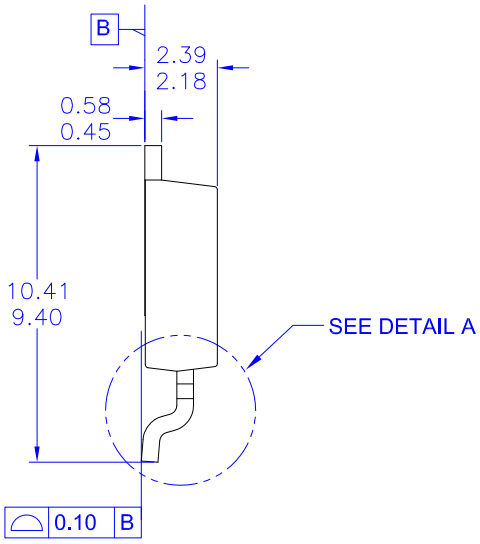
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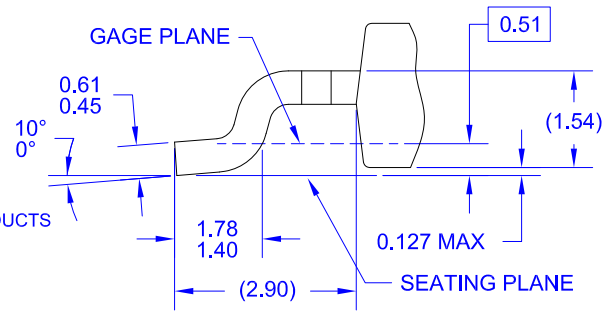


DIODE PRODUCTS VERSION



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D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
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F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
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