*Click **here** to ask an associate for production status of specific part numbers.*

MAX20021/MAX20022

Automotive Quad, Low-Voltage Step-Down DC-DC Converters

General Description

The MAX20021/MAX20022 power-management ICs (PMICs) integrate four low-voltage, high-efficiency, step-down DC-DC converters. Each of the four outputs is factory or resistor programmable between 1.0V to 4.0V and can deliver up to 1.0A of current. The PMICs operate from 3.0V to 5.5V, making them ideal for automotive point-of-load and post-regulation applications.

The PMICs feature fixed-frequency, PWM-mode operation with a switching frequency of 2.2MHz or 3.2MHz. High-frequency operation allows for an all-ceramic capacitor design and small-size external components. The low-resistance, on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Internal current sensing and loop compensation reduce board space and system cost.

The PMICs offer a spread-spectrum option to reduce radiated emissions. Two of the four buck converters operate 180º out-of-phase with the internal clock. This feature reduces the necessary input capacitance and improves EMI as well. All four buck converters operate in constant PWM mode outside the AM band. The PMICs offer a SYNC input to synchronize to an external clock.

The PMICs provide individual enable inputs and power good/reset outputs, as well as factory-programmable $\overline{\text{RESET}}$ times.

The PMICs offer several important protection features including: input overvoltage protection, input undervoltage monitoring, input undervoltage lockout, cycle-by-cycle current limiting, and overtemperature shutdown. The input undervoltage monitor indicates a brownout condition by driving PG_ low when the input falls below the UVM threshold.

The MAX20021/MAX20022 PMICs are available in a 28-pin TQFN package with an exposed pad and are specified for operation over the -40°C to +125°C automotive temperature range.

Applications

- Automotive
- Industrial

Benefits and Features

- Quad Step-Down DC-DC Converters with Integrated FETs
- Operate from 3.0V to 5.5V Supply Voltage
- 1.0V to 4.0V Fixed or Adjustable Output Voltage
- 2.2MHz (MAX20022) or 3.2MHz (MAX20021) Switching Frequency
- Four Channels Capable of Delivering up to 1A Each
- Designed to Improve Automotive EMI Performance
  - Forced-PWM Operation
  - Two Channels 180° Out-of-Phase
  - SYNC Input
  - Spread-Spectrum Option
- Soft-Start and Supply Sequencing Reduces Inrush Current
- Individual Enable Inputs and Power-Good Outputs to Simplify Sequencing
- OV/UV Input-Voltage Monitoring
- Overtemperature and Short-Circuit Protection
- 28-Pin (5mm x 5mm x 0.8mm) TQFN-EP Package
- -40°C to +125°C Operating Temperature Range

For related parts and recommended products to use with this part, refer to the MAX20021 product page.

***Ordering Information** appears at end of data sheet.*

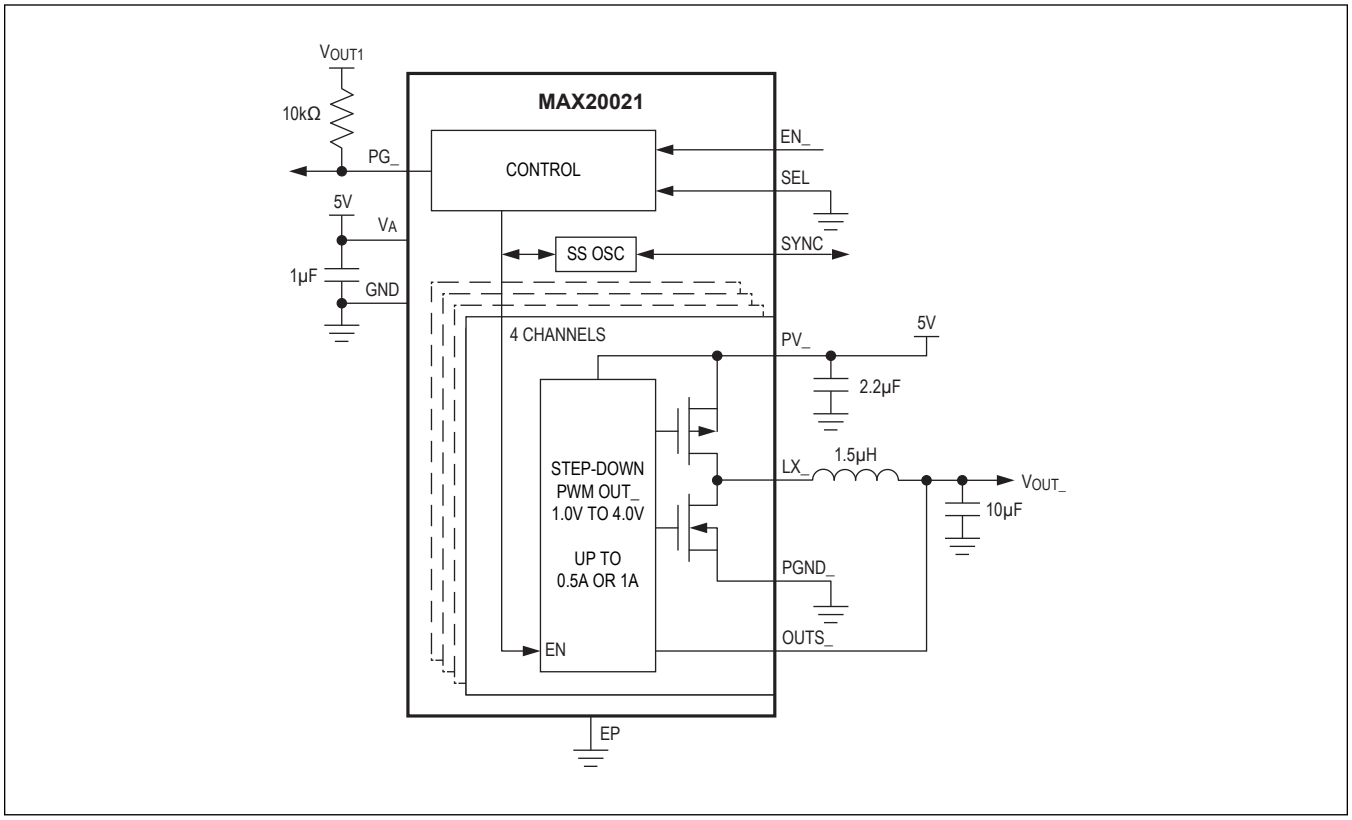
19-6628; Rev 4; 8/23

© 2023 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

One Analog Way, Wilmington, MA 01887 U.S.A. | Tel: 781.329.4700 | © 2023 Analog Devices, Inc. All rights reserved.

Downloaded from Arrow.com.

Simplified Block Diagram



Downloaded from Arrow.com.

Absolute Maximum Ratings

PV_ to PGND_ ..... -0.3V to +6.0V
V_A to GND ..... -0.3V to +6.0V
OUTS_, EN_, PG_, SYNC, SEL to GND ..... -0.3V to V_A + 0.3V
PV_ to PV_ ..... -0.3V to +0.3V
PGND_ to GND ..... -0.3V to +0.3V
LX_ to PGND ..... -1.0V to PV_ + 0.3V
LX_ Continuous RMS Current 2.0A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 28.6mW/ºC above +70ºC) 2285mW
ESD_{HB} ..... ±2kV
ESD_{MM} ..... ±200V
Operating Temperature Range ..... -40ºC to +125ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -65ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC
Soldering Temperature (reflow) ..... +260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

28 TQFN-EP

Package Code	T2855+5
Outline Number	21-0140
Land Pattern Number	90-0027
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	$V_{PV\_}$	Fully operational		3.0		5.5	V
Supply Current	I_{PV0}	No load, no switching, V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = $V_{PV\_}$		2.5	3.8	5	mA
Shut-Off Current	I_{VPSD}	V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = V_{GND}	T_A = +25°C		0.1	2	µA
			T_A = +125°C		2		
Overvoltage Threshold		Rising		5.6	5.8	6	V
		Hysteresis			0.1		
Undervoltage Monitor Threshold		UVM option enabled	$V_{PV\_}$ falling	4.15	4.3	4.45	V
			$V_{PV\_}$ hysteresis		0.1		
UVLO Threshold		$V_{PV\_}$ falling		2.68			V
		$V_{PV\_}$ rising				3.0	

Downloaded from Arrow.com.

Electrical Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}	Switching frequency = 2.2MHz (see the *Ordering Information*)	2.0	2.2	2.4	MHz
		Switching frequency = 3.2MHz (see the *Ordering Information*)	3.0	3.2	3.4	
Spread Spectrum	Df/f	Spread-spectrum option = enabled (see the *Ordering Information*)		+3		%
SYNC Input Frequency Range	f_{SYNC}	PWM switching frequency = 2.2MHz (see the *Ordering Information*)	1.7		2.5	MHz
		PWM switching frequency = 3.2MHz (see the *Ordering Information*)	2.8		3.5	
OUT1, OUT2, OUT3, OUT4—SYNCHRONOUS STEP-DOWN DC-DC CONVERTERS						
Fixed DC Output Accuracy		I_{LOAD} = 0mA		+1.5		%
		I_{LOAD} = 0mA to I_{MAX}	-3		+3	
FB DC Set-Point Accuracy	$V_{SFB\_}$	MAX20022, I_{LOAD} = 0mA		1015		mV
		MAX20022, I_{LOAD} = 0mA to I_{MAX}	970		1030	
Load Regulation		I_{LOAD} = I_{MAX}		-1.5	-2.5	%
Line Regulation		I_{LOAD} = I_{MAX}/2, $V_{PV\_}$ = 4.5V to 5.5V		+0.3		%
pMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		125	250	mΩ
nMOS On-Resistance		$V_{PV\_}$ = 5.0V, $I_{LX\_}$ = 0.2A		100	200	mΩ
pMOS Current-Limit Threshold	I_{LIM}	1.0A channel output (see the *Ordering Information*)	1.4	1.65	2	A
		0.5A channel output (see the *Ordering Information*)	0.8	1.1	1.5	
Soft-Start Ramp Time				3272		Cycles
OUTS Leakage Current	$I_{B\_OUTS\_}$	Externally adjustable output		20		µA
LX Leakage Current		$V_{PV\_}$ = 5.0V, LX_ = $V_{PGND\_}$ or $V_{PV\_}$		0.1		µA
Minimum On-Time				45	66	ns
LX Rise/Fall Time				4		ns
Duty Cycle Range					100	%
OUTS_ Discharge Resistance		$V_{EN\_}$ = VGND		35		Ω
OUT1, OUT2 Phasing		(*Note 2*)		0		Degrees
OUT3, OUT4 Phasing		(*Note 2*)		180		Degrees
THERMAL OVERLOAD						
Thermal-Shutdown Temperature		T_J rising (*Note 3*)		+185		ºC
Hysteresis		(*Note 3*)		15		ºC
OUTPUT POWER-GOOD INDICATORS (PG_)						
Output Overvoltage Threshold		V_{OUT} rising (percentage of nominal output)	106	110	114	%

Downloaded from Arrow.com.

Electrical Characteristics (continued)

($V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V$; $T_A = T_J = -40°C$ to $+125°C$, unless otherwise noted. Typical values are at $T_A = +25°C$ under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Undervoltage Threshold		V_{OUT} falling (percentage of nominal output)	92.5	94	96	%
		V_{OUT} rising (percentage of nominal output)	93.5	95	97	
UV/OV Propagation Delay				15		µs
PG_ Output High Leakage Current				0.1		µA
PG_ Output Low Level		$V_{PV\_}$ = 3.0V, sinking 3mA			0.22	V
ENABLE INPUTS (EN_)						
Input High Level		$V_{PV\_}$ = 5.0V, $V_{EN\_}$ rising	0.7	1.0	1.3	V
Hysteresis		$V_{PV\_}$ = 5.0V, $V_{EN\_}$ falling		50		mV
Pulldown Resistance				100		kΩ
DIGITAL INTERFACE (SYNC, SEL)						
Input Voltage High	V_{INH}		1.5			V
Input Voltage Low	V_{INL}				0.5	V
Input Voltage Hysteresis				70		mV
Pulldown Resistance				100		kΩ

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: Phase measurement is in relation to the rising edge of $V_{LX\_}$.

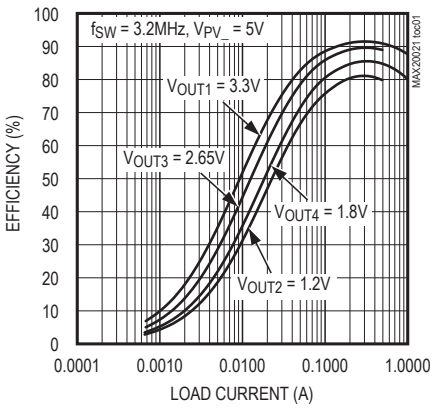
Note 3: Guaranteed by design. Not production tested.

Downloaded from Arrow.com.

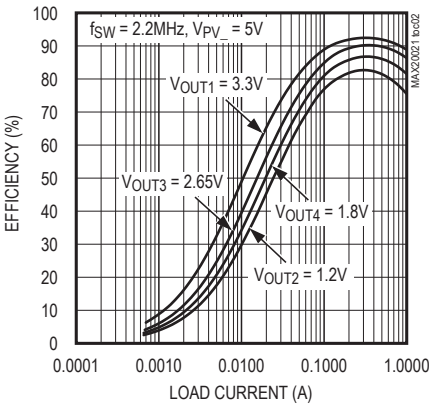
Typical Operating Characteristics

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = +25°C, unless otherwise noted.)

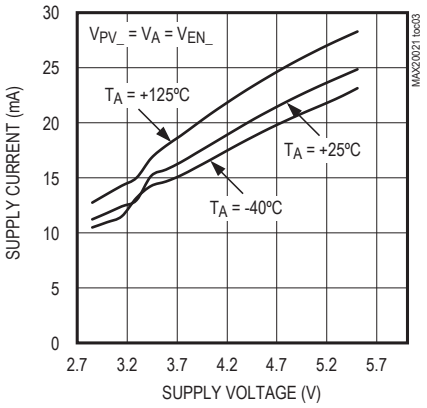
BUCK EFFICIENCY (3.2MHz) vs. LOAD CURRENT



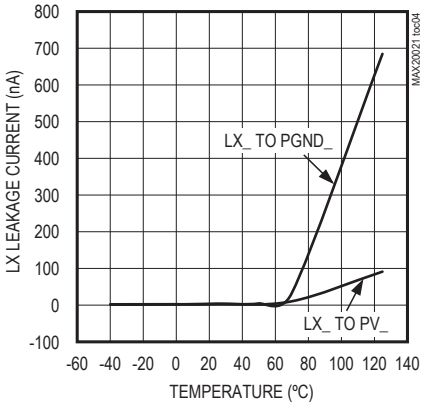
BUCK EFFICIENCY (2.2MHz) vs. LOAD CURRENT



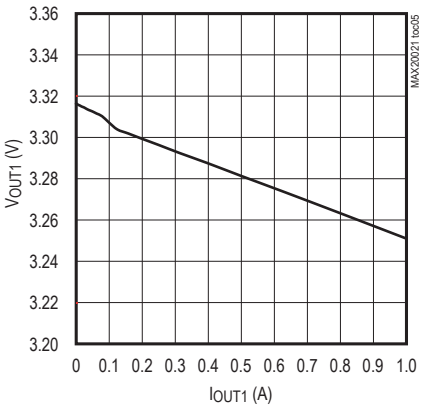
SUPPLY CURRENT vs. SUPPLY VOLTAGE



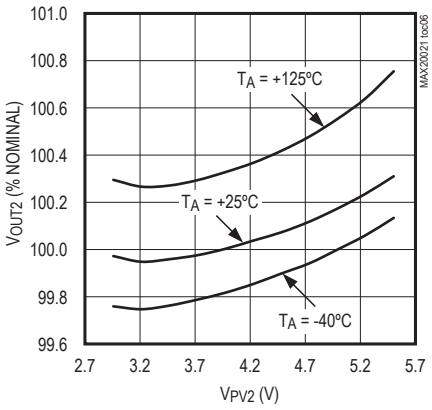
LX LEAKAGE CURRENT vs. TEMPERATURE



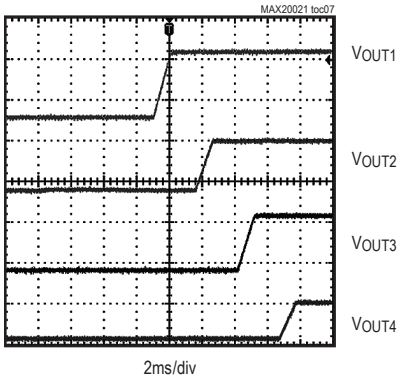
LOAD REGULATION (BUCK 1)



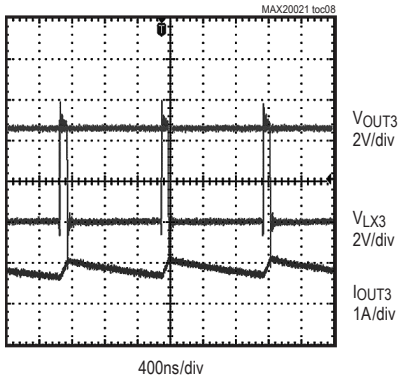
LINE REGULATION (BUCK 2)



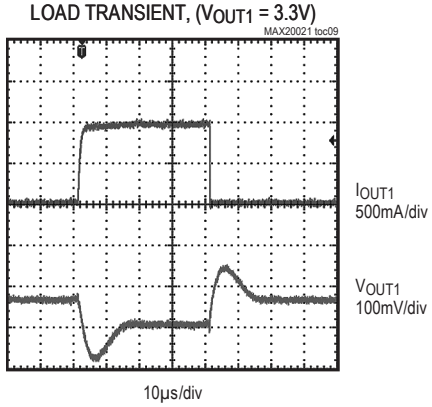
STARTUP SEQUENCE



SHORT-CIRCUIT BEHAVIOR



LOAD TRANSIENT, (V_{OUT1} = 3.3V)

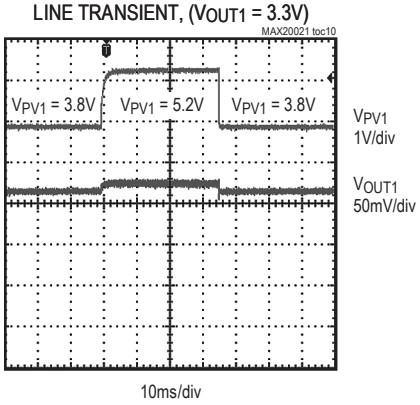


Downloaded from Arrow.com.

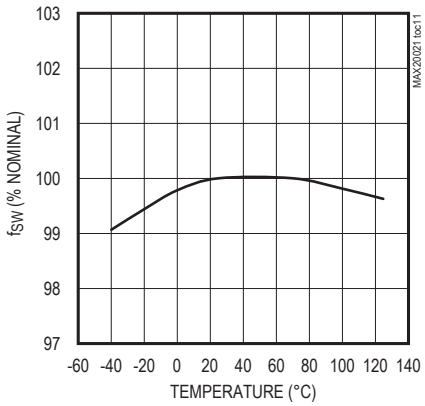
Typical Operating Characteristics (continued)

(V_A = V_{PV1} = V_{PV2} = V_{PV3} = V_{PV4} = 5.0V; T_A = +25ºC, unless otherwise noted.)

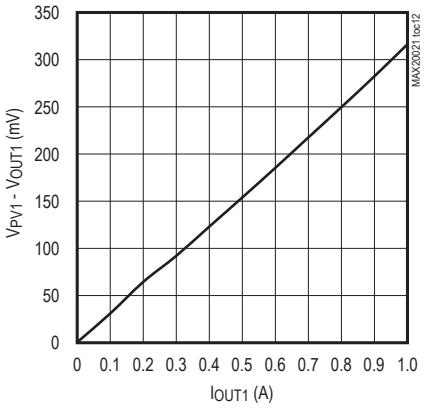
LINE TRANSIENT, (V_{OUT1} = 3.3V)



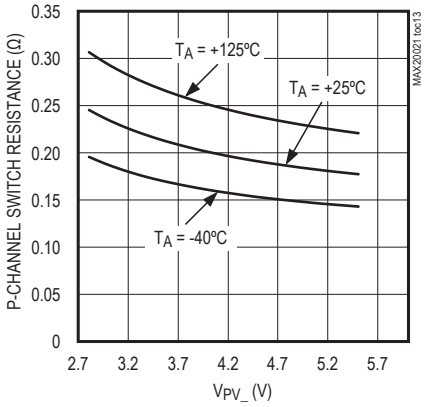
SWITCHING FREQUENCY vs. TEMPERATURE



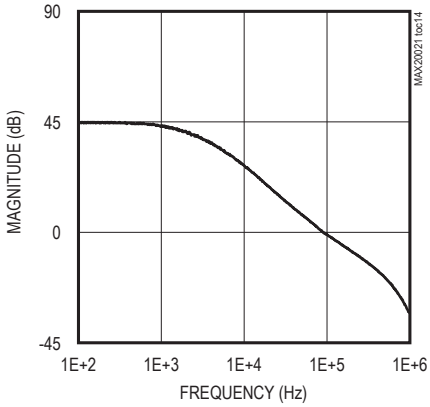
DROPOUT VOLTAGE vs. LOAD CURRENT (BUCK 1)



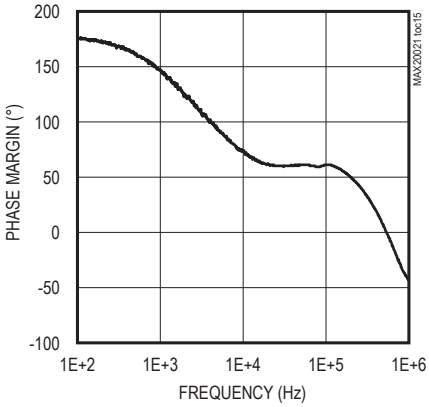
P-CHANNEL SWITCH RESISTANCE vs. SUPPLY VOLTAGE



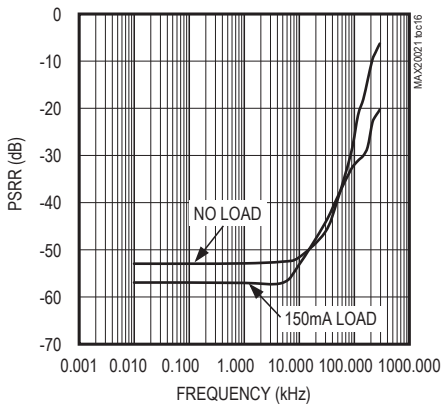
SMALL-SIGNAL GAIN vs. FREQUENCY



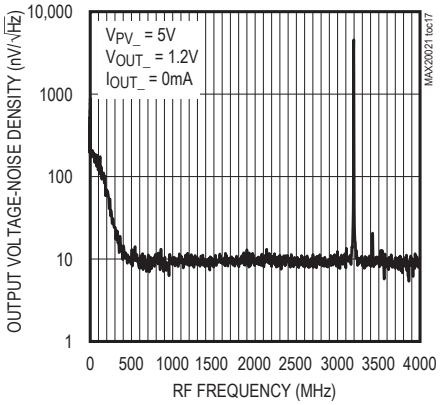
PHASE MARGIN vs. FREQUENCY



PSRR vs. FREQUENCY

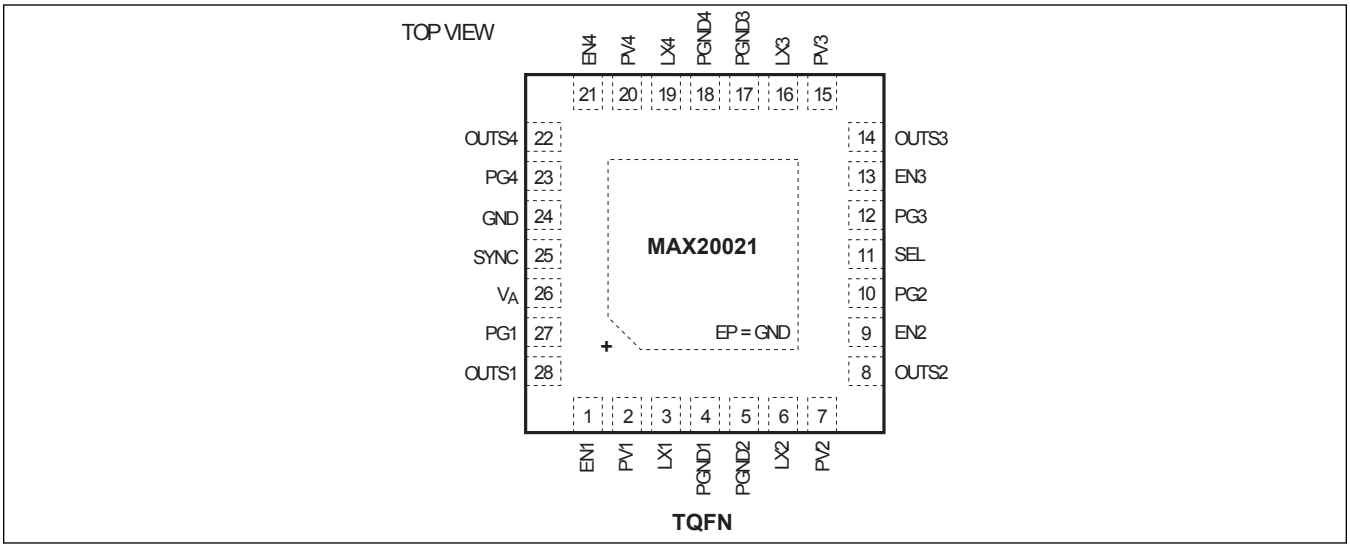


OUTPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY



Downloaded from Arrow.com.

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	EN1	Active-High Digital Enable Input for Buck 1. Driving EN1 high enables Buck 1.
2	PV1	Buck 1 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV1 to PGND1 as close possible to the device.
3	LX1	Buck 1 Switching Node. LX1 is high impedance when the device is off.
4	PGND1	Power Ground for Buck 1
5	PGND2	Power Ground for Buck 2
6	LX2	Buck 2 Switching Node. LX2 is high impedance when the device is off.
7	PV2	Buck 2 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV2 to PGND2 as close as possible to the device.
8	OUTS2	Buck 2 Voltage Sense Input
9	EN2	Active-High Digital Enable Input for Buck 2. Driving EN2 high enables Buck 2.
10	PG2	Open-Drain, Active-High, Power-Good Output for Buck 2. To obtain a logic signal, pull up PG2 with an external resistor connected to a positive voltage equal to or lower than V_A.
11	SEL	Buck 3 Output-Voltage Select Input. Connect SEL to PGND_ for a 1.8V output. Connect SEL to PV_ for a 2.65V output. Do not toggle during normal operation.
12	PG3	Open-Drain, Active-High, Power-Good Output for Buck 3. To obtain a logic signal, pull up PG3 with an external resistor connected to a positive voltage equal to or lower than V_A.
13	EN3	Active-High Digital Enable Input for Buck 3. Driving EN3 high enables Buck 3.
14	OUTS3	Buck 3 Voltage Sense Input
15	PV3	Buck 3 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV3 to PGND3 as close as possible to the device.
16	LX3	Buck 3 Switching Node. LX3 is high impedance when the device is off.
17	PGND3	Power Ground for Buck 3
18	PGND4	Power Ground for Buck 4
19	LX4	Buck 4 Switching Node. LX4 is high impedance when the device is off.

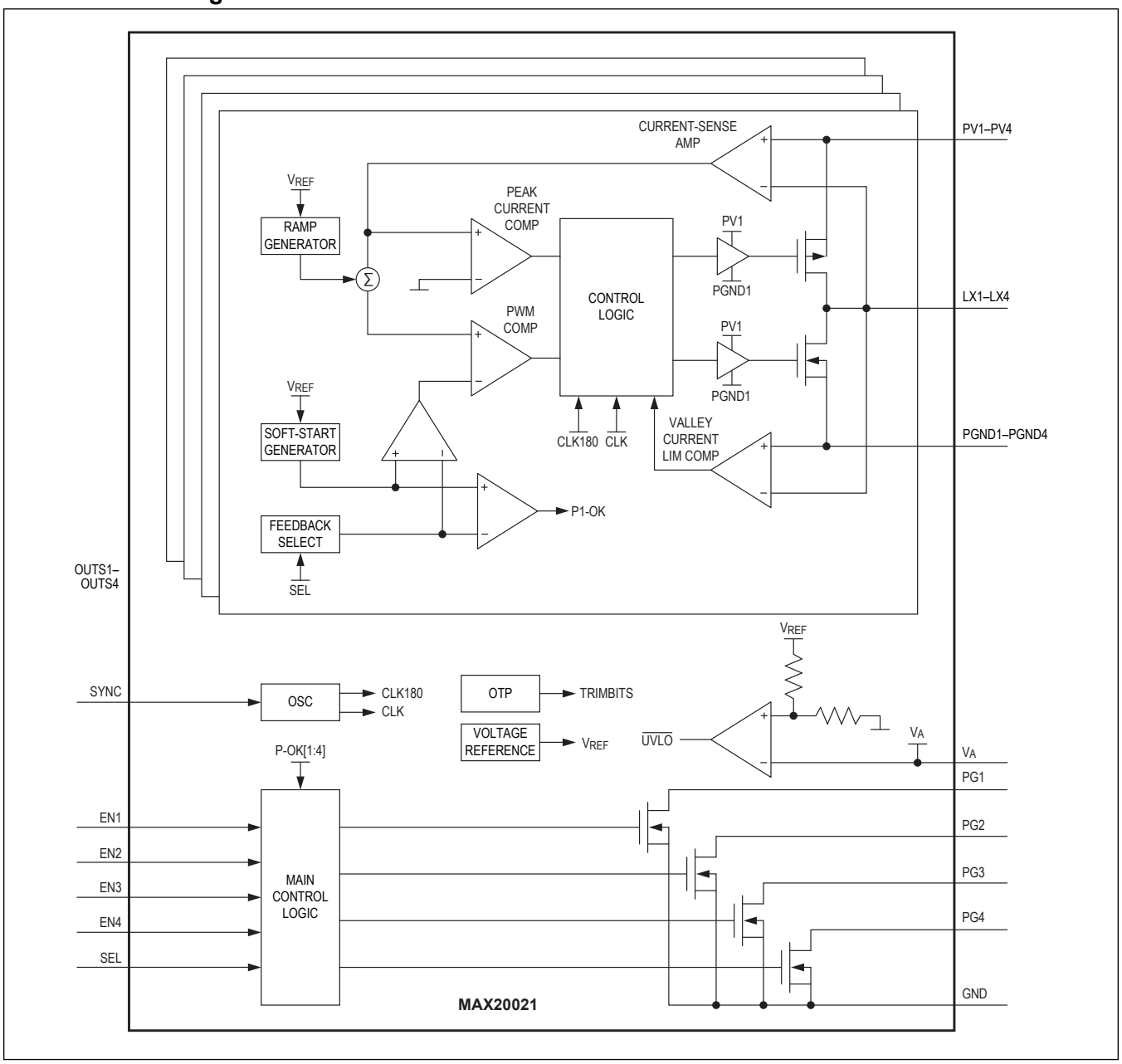
Downloaded from Arrow.com.

Pin Description (continued)

PIN	NAME	FUNCTION
20	PV4	Buck 4 Voltage Input. Connect a 2.2µF or larger ceramic capacitor from PV4 to PGND4 as close as possible to the device.
21	EN4	Active-High Digital Enable Input for Buck 4. Driving EN4 high enables Buck 4.
22	OUTS4	Buck 4 Voltage Sense Input
23	PG4	Open-Drain, Active-High, Power-Good Output for Buck 4. To obtain a logic signal, pull up PG4 with an external resistor connected to a positive voltage equal to or lower than V_A.
24	GND	Analog Ground
25	SYNC	SYNC Input. Supply an external clock to control the switching frequency. Connect SYNC to PGND_ to use the default switching frequency.
26	V_A	Analog Voltage Supply. Connect a 1µF or larger ceramic capacitor from V_A to GND as close as possible to the device. Connect to the same supply as PV_ inputs.
27	PG1	Open-Drain, Active-High, Power-Good Output for Buck 1. To obtain a logic signal, pull up PG1 with an external resistor connected to a positive voltage equal to or lower than V_A.
28	OUTS1	Buck 1 Voltage Sense Input
-	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND1–PGND4 and GND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Downloaded from Arrow.com.

Internal Block Diagram



Downloaded from Arrow.com.

Detailed Description

The MAX20021/MAX20022 PMICs offer four, high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and provide a 1.0V to 4.0V output voltage range. The PMICs deliver up to 1.0A of load current per output. The PMICs achieve ±3% output error over load, line, and temperature ranges.

The PMICs feature fixed-frequency, PWM-mode operation with a 2.2MHz or 3.2MHz switching frequency. An optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency, while a factory-programmable synchronization input (SYNC) allows the device to synchronize to an external clock.

Integrated low R_{DSON} switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions.

The PMICs are offered in factory-preset output voltages to allow customers to achieve ±3% output-voltage accuracy without using expensive 0.1% resistors. In addition, adjustable output-voltage versions can be set to any desired values between 1.0V and 4.0V using an external resistive divider. See the *Ordering Information* for available options.

Additionally, each converter features soft-start, PG_ output, overcurrent, and overtemperature protections (see *Internal Block Diagram*).

Control Scheme

The PMICs use peak current-mode control. The devices feature internal slope compensation and internal loop compensation, both of which reduce board space and allow a very compact solution.

Hybrid Load-Line Architecture

The PMICs feature hybrid load-line architecture to reduce the output capacitance needed, potentially saving system cost and size. This results in a measurable load-transient response (see Figure 1).

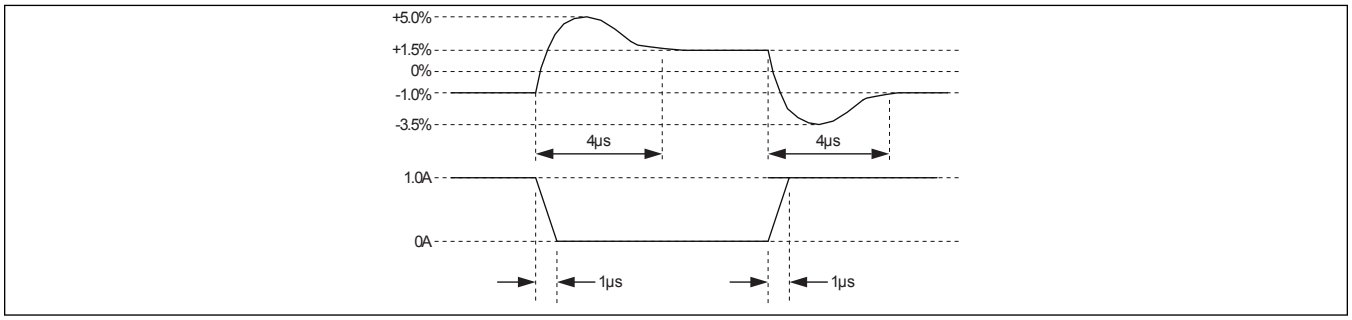


Figure 1. Load-Transient Response

Input Overvoltage Monitoring (OV)

The PMICs feature an input overvoltage-monitoring circuit on the input supply. When the input exceeds 5.8V (typ) all power-good indicators (PG_) go low. When the input supply returns to within the operating range of 5.7V (typ) or less during the timeout period, the power-good indicators go high.

Input Undervoltage Monitoring (UVM)

The MAX20021 features an input undervoltage monitoring circuit on the input supply. When the input drops below 4.3V (typ), all power-good indicators (PG_) go low to indicate a potential brownout condition. The device remains operational down to the UVLO threshold. When the input voltage exceeds the UV threshold above 4.4V (typ), PG_ remains low for the factory-trimmed “active timeout period.” UVM is a factory-selectable option.

Input Undervoltage Lockout (UVLO)

The PMICs feature an undervoltage lockout on the PV_ inputs set at 2.77V (typ) falling. This prevents loss of control of the device by shutting down all outputs. This circuit is only active when at least one buck converter is enabled.

Downloaded from Arrow.com.

Power-Good Outputs (PG_)

The PMICs feature an open-drain power-good output for each of the four buck regulators. PG_ asserts low when the output voltage drops 6% below the regulated voltage or 10% above the regulated voltage for approximately 15µs. PG_ remains asserted for a fixed 20,480 switching cycles after the output returns to its regulated voltage. PG_ asserts low during soft-start and in shutdown. PG_ becomes high impedance when Buck_ is in regulation. Connect PG_ to a logic supply with a 10kΩ resistor.

Soft-Start

The PMICs include a 3272 switching cycle fixed-duration soft-start time. The soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. During soft-start, the converters operate in skip mode to prevent the outputs from discharging.

When the PMICs exit UVLO or thermal shutdown, there is a fixed blanking time for EN2–EN4 to prevent all four outputs from going through soft-start at the same time. After 24,576 switching cycles with $\overline{UVLO}$ high and at least one buck converter enabled, there is no blanking time between EN2–EN4 high and the start of soft-start.

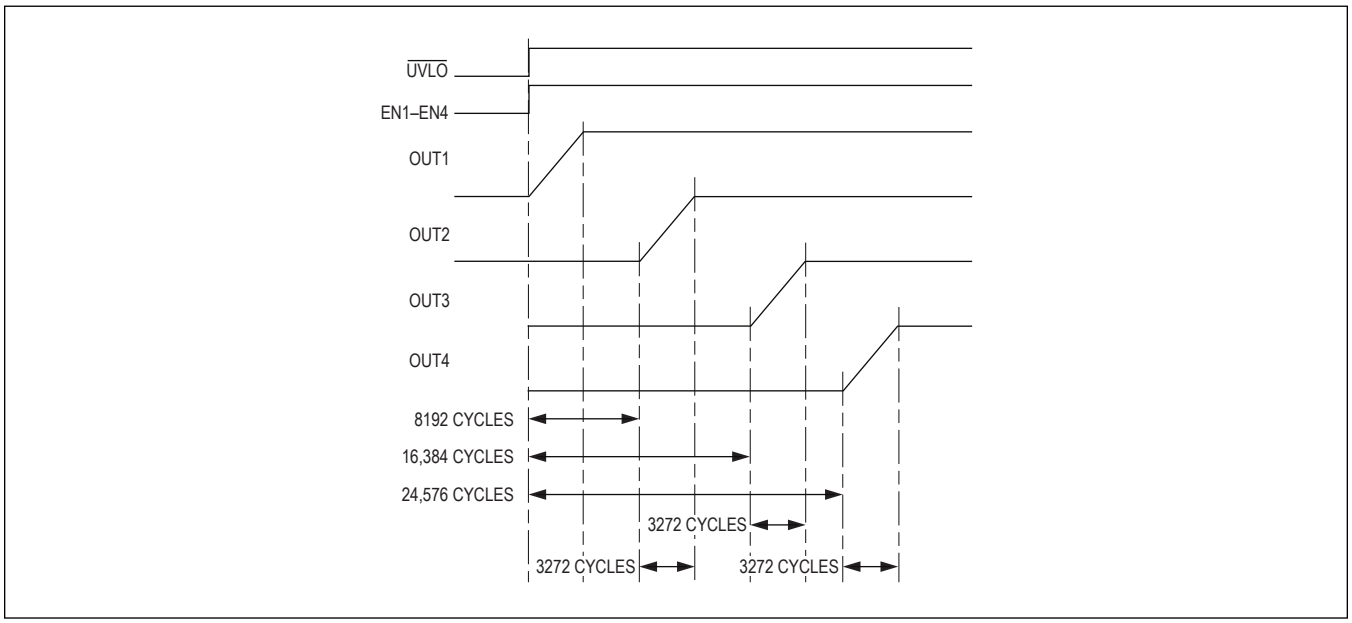


Figure 2. Power-Up Soft-Start Delays

Output 3 Voltage Select (SEL)

The MAX20021 offers a SEL input to allow selection of the OUT3 voltage. For fixed output versions, connect SEL to PGND_ for a 1.8V output or to PV_ for a 2.65V output. There is no soft transition between the two output-voltage settings, so SEL should not be toggled during normal operation. For the MAX20022, connect SEL to PGND_ or leave unconnected.

Spread-Spectrum Option

The PMICs feature a linear spread-spectrum (SS) operation, which varies the internal operating frequency between f_{SW} and (f_{SW} + 3%). The internal oscillator is frequency modulated at a rate of 1.5kHz with a frequency deviation of 3% (see Figure 3). This function does not apply to an oscillation frequency applied externally through the SYNC pin. Spread spectrum is a factory-selectable option. See the *Ordering Information* for available options.

Downloaded from Arrow.com.

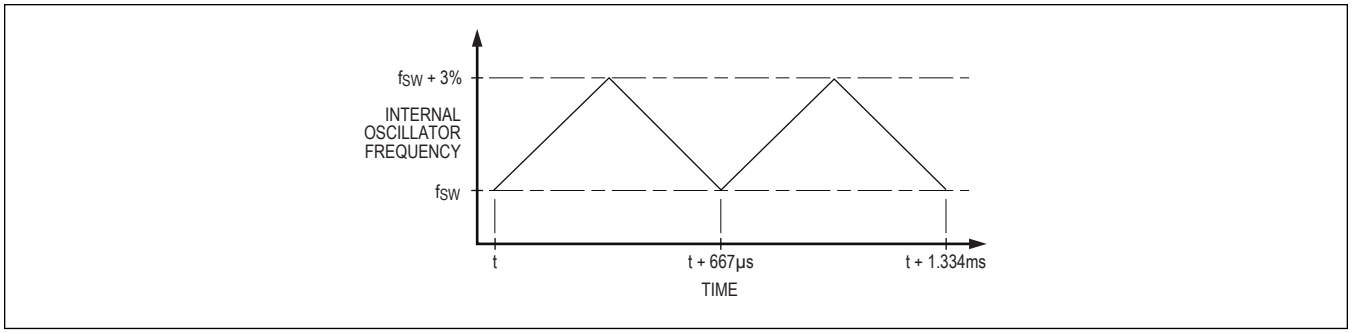


Figure 3. Effect of Spread-Spectrum on Internal Oscillator

Synchronization (SYNC)

The PMICs feature a SYNC input to allow the internal oscillator to synchronize with an external clock. SYNC accepts signal frequencies in the range of 1.7MHz < f_{SYNC} < 2.5MHz (2.2MHz option), or 2.7MHz < f_{SYNC} < 3.5MHz (3.2MHz option). Connect to PGND_ if the SYNC feature is not used.

Current-Limit/Short-Circuit Protection

The PMICs offer a current-limit feature that protects the devices against short-circuit and overload conditions on each output. In the event of a short-circuit or overload condition at an output, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down. The converter allows the high-side MOSFET to turn on only when the inductor current ramps down to the low-side MOSFET's current threshold. This cycle repeats until the short or overload condition is removed.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the PMICs. When the junction temperature exceeds +185°C (typ), an internal thermal sensor shuts down the step-down converters, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C. The IC goes through a standard power-up sequence as defined in the *Soft-Start* section.

Downloaded from Arrow.com.

Applications Information

Adjustable Output-Voltage Option

The MAX20022 features adjustable output voltages (see the *Ordering Information* for more details), which allows the customer to set the outputs to any voltage between 1.0V and $V_{PV\_}$ - 0.5V (up to 4.0V). Connect a resistive divider from output ($V_{OUT\_}$) to OUTS_ to GND to set the output voltage (see Figure 4). Select R2 (OUTS_ to the GND resistor) less than or equal to 100kΩ. Calculate R1 ($V_{OUT\_}$ to the OUTS_ resistor) with the following equation:

$$R1 = R2[(\frac{V_{OUT\_}}{V_{OUTS\_}}) - 1]$$

where $V_{OUTS\_}$ = 1000mV (see the *Electrical Characteristics* table). The output voltage is nominal at 50% load current.

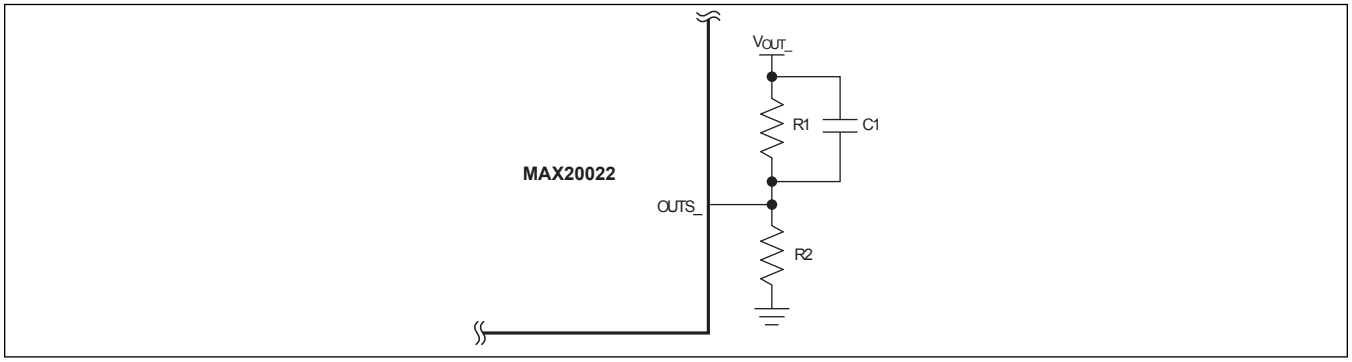


Figure 4. Adjustable Output-Voltage Configuration

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R1 in the resistive divider network. Use the following equation to determine the value of the capacitor:

If $\frac{R2}{R1} > 1$, $C1 = C(\frac{R2}{R1})$

else C1 = C, where C = 15pF

Connect OUTS_ to $V_{OUT\_}$ for a fixed 1.0V output voltage.

Inductor Selection

The PMICs are optimized for use with a 1.5µH inductor for 2.2MHz and 3.2MHz operation. Chip inductors can be used for additional board-space savings.

Input Capacitor

The PMICs are designed to operate with a single 2.2µF ceramic bypass capacitor on each PV_ input. Phase interleaving of the four buck converters contributes to a lower required input capacitance by canceling input ripple currents. Place the bypass capacitors as close as possible to their corresponding PV_ input to ensure the best EMI and jitter performance.

Output Capacitor

All outputs of the PMICs are optimized for use with a 10µF X7R ceramic capacitor. Additional output capacitance can be used if better voltage ripple or load-transient response is required. Due to the soft-start sequence, the device is unable to drive arbitrarily large output capacitors.

Thermal Considerations

How much power the package can dissipate strongly depends on the mounting method of the IC to the PCB and the copper area for cooling. Using the JEDEC test standard, the maximum power dissipation allowed is 2285mW in the

Downloaded from Arrow.com.

TQFN package. More power dissipation can be handled by the package if great attention is given during PCB layout. For example, using the top and bottom copper as a heatsink and connecting the thermal vias to one of the middle layers (GND) transfers the heat from the package into the board more efficiently, resulting in lower junction temperature at high power dissipation in some PMIC applications. Furthermore, the solder mask around the IC area on both top and bottom layers can be removed to radiate the heat directly into the air. The maximum allowable power dissipation in the IC is as follows:

$$P_{MAX} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient air temperature, θ_{JC} (3°C/W for the 28-pin TQFN) is the thermal resistance from the junction to the case, and θ_{CA} is the thermal resistance from the case to the surrounding air through the PCB, copper traces, and the package materials. θ_{CA} is directly related to system-level variables and can be modified to increase the maximum power dissipation.

The TQFN package has an exposed thermal pad on its underside. This pad provides a low thermal-resistance path for heat transfer into the PCB. This low thermally resistive path carries a majority of the heat away from the IC. The PCB is effectively a heatsink for the IC. The exposed pad should be connected to a large ground plane for proper thermal and electrical performance. The minimum size of the ground plane is dependent upon many system variables. To create an efficient path, the exposed pad should be soldered to a thermal landing, which is connected to the ground plane by thermal bias. The thermal landing should be at least as large as the exposed pad and can be made larger depending on the amount of free space from the exposed pad to the other pin landings. A sample layout is available on the MAX20022 evaluation kit to speed designs.

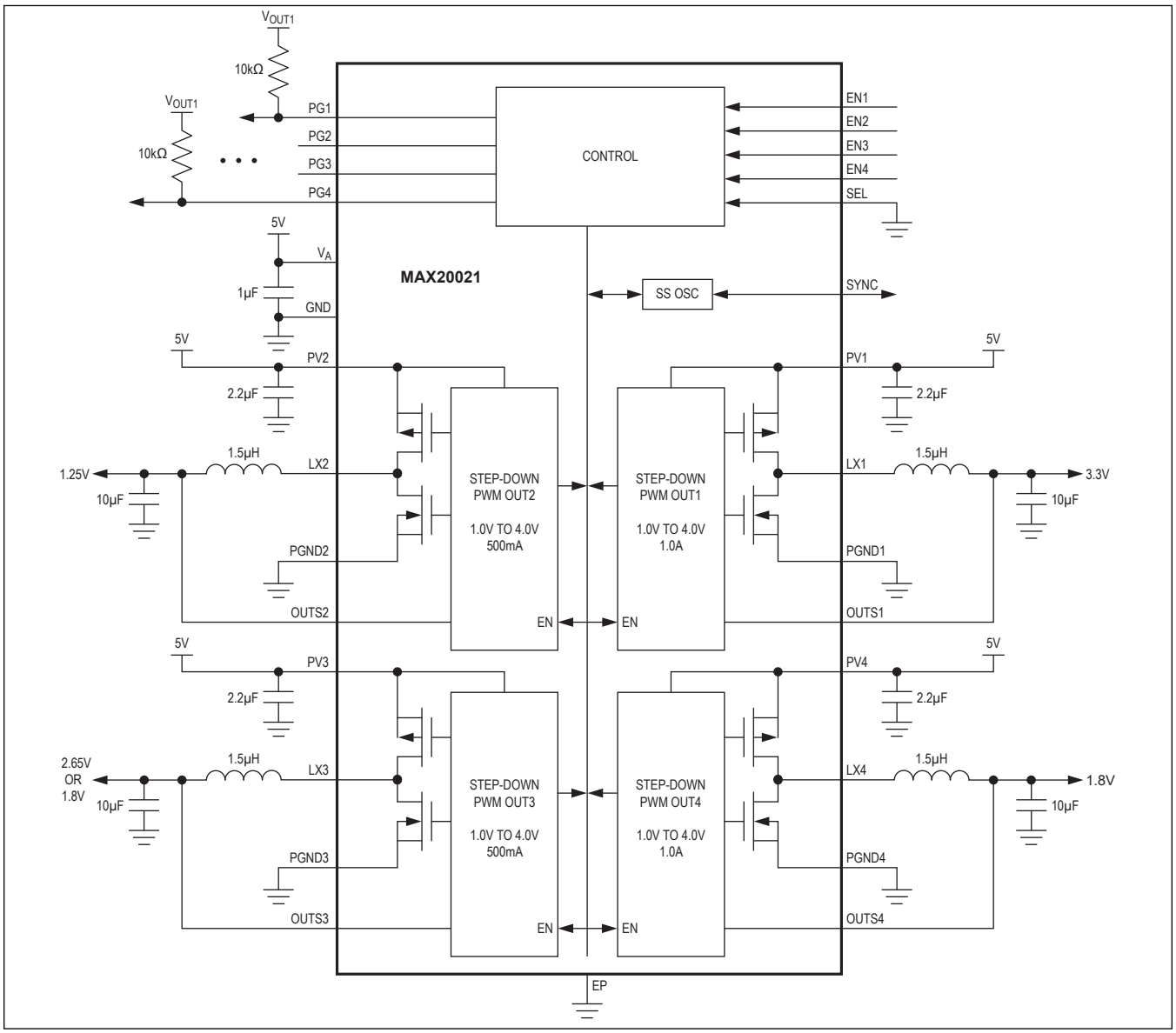
PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1. Use a large contiguous copper plane under the PMIC packages. Ensure that all heat-dissipating components have adequate cooling.
2. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, inductor, and the output capacitor should be as short as possible.
3. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
4. Use a single ground plane to reduce the chance of ground potential differences. With a single ground plane, enough isolation between analog return signals and high-power signals must be maintained.

Downloaded from Arrow.com.

Typical Operating Circuit



Downloaded from Arrow.com.

Ordering Information

PART	CURRENT CONFIGURATION				V_{OUT} (V)				SPREAD SPEC-TRUM	FREQU-ENCY (MHz)	UVM	ACTIVE TIMEOUT PERIOD (CYCLES)
	CH1	CH2	CH3	CH4	CH1	CH2	CH3	CH4				
MAX20021												
MAX20021ATIA/V+	1.0A	0.5A	0.5A	1.0A	3.30	1.25	2.65/1.80	1.80	Disabled	3.2MHz	Enabled	20, 480
MAX20021ATIB/V+	1.0A	0.5A	0.5A	1.0A	3.30	1.25	2.65/1.80	1.80	Enabled	3.2MHz	Enabled	20, 480
MAX20021ATIC/V+	1.0A	0.5A	0.5A	1.0A	3.30	1.20	2.65/1.80	1.50	Disabled	3.2MHz	Enabled	20, 480
MAX20021ATID/V+	1.0A	0.5A	0.5A	1.0A	3.30	1.20	2.65/1.80	1.80	Disabled	3.2MHz	Enabled	20, 480
MAX20022												
MAX20022ATIA+	1.0A	1.0A	1.0A	1.0A	ADJ	ADJ	ADJ	ADJ	Disabled	2.2MHz	Disabled	256
MAX20022ATIA/V+	1.0A	1.0A	1.0A	1.0A	ADJ	ADJ	ADJ	ADJ	Disabled	2.2MHz	Disabled	256
MAX20022ATIB+	1.0A	1.0A	1.0A	1.0A	ADJ	ADJ	ADJ	ADJ	Enabled	2.2MHz	Disabled	256
MAX20022ATIB/V+	1.0A	1.0A	1.0A	1.0A	ADJ	ADJ	ADJ	ADJ	Enabled	2.2MHz	Disabled	256

/V Denotes an automotive-qualified part that conforms to AECQ-100.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**Contact factory for options that are not included. Factory-selectable features include:*

- DC-DC voltages in 100mV steps between 1.0V and 4.0V.

- Spread spectrum enabled or disabled.

- UVM enabled or disabled.

- Number of cycles in active timeout period

- Independent current limit for each channel up to 1A.

Downloaded from Arrow.com.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	4/13	Removed future product reference for the MAX20022	15
2	12/13	Added AEC-Q100 reference to Ordering Information	15
3	8/14	Added two new MAX20021 options to Ordering Information	15
4	8/23	Updated packaging land pattern number and Electrical Characteristics table	3, 4

ANALOG DEVICES
www.analog.com

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

Downloaded from Arrow.com.