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NTE6402

Programmable Unijunction Transistor (PUT)

Description:

The NTE6402 is a 3-terminal silicon planer passivated PNP device available in the standard plastic low cost TO98 and TO92 type packages. The terminals are designated as anode, anode gate, and cathode.

This device has been characterized as a Programmable Unijunction Transistor (PUT), designed to enable the engineer to “program” unijunction characteristics such as R_{BB} , η , I_V , and I_P by merely selecting two resistor values. Applications include thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate.

Features:

- Programmable – R_{BB} , η , I_V , and I_P
- Low On-State Voltage – 1.5V Max @ $I_F = 50\text{mA}$
- Low Gate to Anode Leakage Current – 10nA Max
- High Peak Output Voltage – 11V Typ
- Low Offset Voltage – 0.35V Typ ($R_G = 10\text{k}\Omega$)

Absolute Maximum Ratings: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Power Dissipation, P_F	300mW
Derate Above $+25^\circ\text{C}$	4mW/ $^\circ\text{C}$
DC Forward Anode Current, I_T	150mA
Derate Above $+25^\circ\text{C}$	2.67mA/ $^\circ\text{C}$
DC Gate Current, I_G	$\pm 50\text{V}$
Repetitive Peak Forward Current, I_{TRM}	
Pulse Width = 100 μs , Duty Cycle = 1%	1A
Pulse Width = 20 μs , Duty Cycle = 1%	2A
Non-Repetitive Peak Forward Current (Pulse Width = 10 μs), I_{TSM}	5A
Gate-to-Cathode Forward Voltage, V_{GKF}	+40V
Gate-to-Cathode Reverse Voltage, V_{GKR}	-5V
Gate-to-Anode Reverse Voltage, V_{GAR}	+40V
Anode-to-Cathode Voltage (Note 1), V_{AK}	$\pm 40\text{V}$
Operating Junction Temperature Range, T_J	-50° to $+100^\circ\text{C}$
Storage Temperature Range, T_{stg}	-55° to $+150^\circ\text{C}$
Thermal Resistance, Junction-to-Case, R_{thJC}	75 $^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient, R_{thJA}	200 $^\circ\text{C/W}$
Lead Temperature (During Soldering, 1/16" from case, 10sec max.), T_L	+260 $^\circ\text{C}$

Note 1. Anode positive, $R_{GA} = 100\Omega$
Anode negative, $R_{GA} = \text{Open}$

Electrical Characteristics: ($T_C = +25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Peak Current	I_P	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	–	1.25	2.0	μA
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	–	4.0	5.0	μA
Offset Voltage	V_T	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	0.2	0.7	1.6	V
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	0.2	0.35	0.6	V
Valley Current	I_V	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	–	18	50	μA
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	70	150	–	μA
		$V_S = 10\text{V}, R_G = 200\Omega$	1.5	–	–	mA
Gate-to-Anode Leakage Current	I_{GAO}	$V_S = 40\text{V}, T_A = +25^{\circ}\text{C}, \text{Cathode Open}$	–	1.0	10	nA
		$V_S = 40\text{V}, T_A = +75^{\circ}\text{C}, \text{Cathode Open}$	–	3.0	–	nA
Gate-to-Cathode Leakage Current	I_{GKS}	$V_S = 40\text{V}, \text{Anode-Cathode Short}$	–	5.0	50	nA
Forward Voltage	V_F	$I_F = 50\text{mA Peak}, \text{Note 2}$	–	0.8	1.5	V
Peak Output Voltage	V_O	$V_G = 20\text{V}, C_C = 0.2\mu\text{F}$	6.0	11.0	–	V
Pulse Voltage Rate of Rise	t_r	$V_B = 20\text{V}, C_C = 0.2\mu\text{F}$	–	40	80	ns

Note 2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

