

## 4T4R Direct RF Receiver and Transmitter

### FEATURES

- ▶ Flexible, reconfigurable radio common platform design
  - ▶ Transmitter/receiver channel bandwidth up to 1.2 GHz (4T4R)
  - ▶ RF DAC/RF ADC RF frequency range up to 7.5 GHz
  - ▶ On-chip PLL with multichip synchronization
    - ▶ External RF clock input option
- ▶ Versatile digital features
  - ▶ Selectable interpolation and decimation filters
  - ▶ Configurable DDCs and DUCs
    - ▶ 8 fine complex DUCs (FDUC) and 4 coarse complex DUCs (CDUC)
    - ▶ 8 fine complex DDCs (FDDC) and 4 coarse complex DDCs (CDDC)
    - ▶ FDUCs and FDDCs are fully bypassable
    - ▶ 2 independent 48-bit NCOs per DUC or DDC
  - ▶ Programmable 192-tap PFIR filter for receive equalization
    - ▶ Supports 4 different profile settings loaded via GPIO
  - ▶ Receive AGC support
    - ▶ Fast detect with low latency for fast AGC control
    - ▶ Signal monitor for slow AGC control
    - ▶ Dedicated AGC support pins
  - ▶ Transmit DPD support
    - ▶ Programmable delay and gain per transmit data path
    - ▶ Coarse DDC delay adjust for DPD observation path
  - ▶ Supports real or complex digital data (8-, 12-, or 16-bit)
- ▶ Auxiliary features
  - ▶ ADC clock driver with selectable divide ratios
  - ▶ Power amplifier downstream protection circuitry
  - ▶ On-chip temperature monitoring unit
  - ▶ Programmable GPIO pins support toggling between modes
  - ▶ TDD power savings option and sharing ADCs
- ▶ SERDES JESD204B or JESD204C interface, 16 lanes up to 24.75 Gbps
  - ▶ 8 lanes JESD204B/C transmitter (JT<sub>x</sub>) and 8 lanes JESD204B/C receiver (JR<sub>x</sub>)
  - ▶ Supports Subclass 1
- ▶ Supports multidevice synchronization
- ▶ 15 mm × 15 mm, 324-ball BGA with 0.8 mm pitch

### APPLICATIONS

- ▶ Wireless communications infrastructure
- ▶ W-CDMA, LTE, LTE-A, massive multiple input multiple output (MIMO)
- ▶ Point to point microwave, E-band, and 5G mmWave
- ▶ Broadband communications systems
- ▶ DOCSIS 3.0+ cable modem termination system (CMTS)
- ▶ Communication test and measurement systems

### GENERAL DESCRIPTION

The **AD9988** is a highly integrated device with four 16-bit, 12 GSPS maximum sample rate, RF digital-to-analog converter (DAC) cores, and four 12-bit, 4 GSPS rate, RF analog-to-digital converter (ADC) cores. The device supports four transmitter channels and four receiver channels with a 4T4R configuration. This product is well suited for four-antenna TDD transmitter applications, where the receiver path can be shared between receiver and observation modes. The GPIO pins can be configured and toggled to support different user modes, while phase coherency is maintained. The maximum radio channel bandwidth supported is 1.2 GHz in a 4T4R configuration and a sample resolution of 16 bits. The AD9988 features a 16-lane 24.75 Gbps JESD204C or 15.5 Gbps JESD204B serial data port that allows up to eight lanes per transmit/receive link, an on-chip clock multiplier, and digital signal processing capability targeted at multiband direct to RF radio applications.

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**REVISION HISTORY****7/2021—Rev. 0 to Rev. A**

|                           |    |
|---------------------------|----|
| Changes to Table 20 ..... | 20 |
|---------------------------|----|

**3/2021—Revision 0: Initial Version**

## FUNCTIONAL BLOCK DIAGRAM

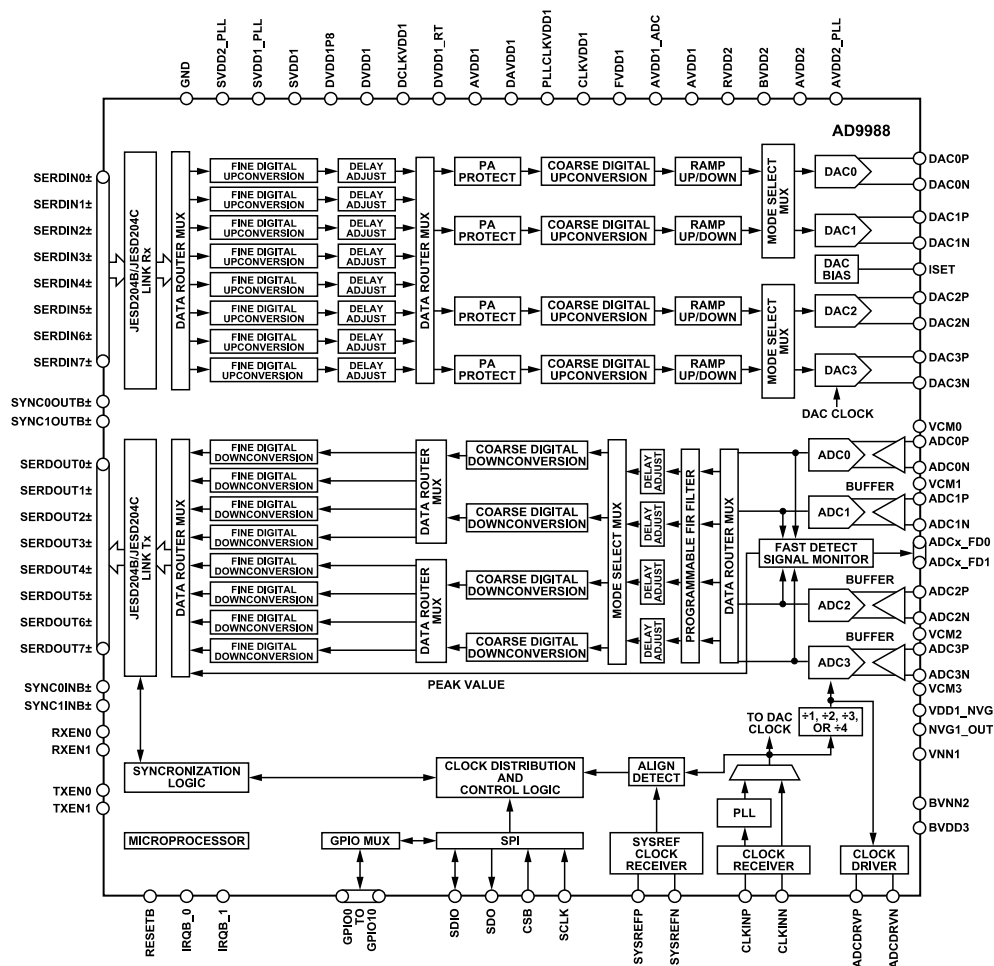


Figure 1.

001

## SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

Successful DAC calibration is required during the device initialization phase that occurs shortly after power-up to ensure long-term reliability of the DAC core circuitry. Refer to [UG-1578](#), the device user guide, for more information on device initialization.

Table 1.

| Parameter                                             | Min  | Typ | Max  | Unit |
|-------------------------------------------------------|------|-----|------|------|
| OPERATING JUNCTION TEMPERATURE ( $T_J$ )              | -40  |     | +120 | °C   |
| ANALOG SUPPLY VOLTAGE RANGE                           |      |     |      |      |
| AVDD2, BVDD2, RVDD2                                   | 1.9  | 2.0 | 2.1  | V    |
| AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, VDD1_NVG1           | 0.95 | 1.0 | 1.05 | V    |
| DIGITAL SUPPLY VOLTAGE RANGE                          |      |     |      |      |
| DVDD1, DVDD1_RT, DCLKVDD1, DAVDD1                     | 0.95 | 1.0 | 1.05 | V    |
| DVDD1P8                                               | 1.7  | 1.8 | 2.1  | V    |
| SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGE RANGE |      |     |      |      |
| SVDD2_PLL                                             | 1.9  | 2.0 | 2.1  | V    |
| SVDD1, SVDD1_PLL                                      | 0.95 | 1.0 | 1.05 | V    |

## POWER CONSUMPTION

Typical at nominal supplies and maximum at 5% supplies. For the minimum and maximum values,  $T_J$  varies between -40°C and +120°C. For the typical values,  $T_A = 25^\circ\text{C}$ , which corresponds to  $T_J = 80^\circ\text{C}$ , unless otherwise noted.

DAC datapath with a complex I/Q data rate frequency ( $f_{IQ\_DATA}$ ) = 1500 MSPS, interpolation of 8 $\times$ , and DAC frequency ( $f_{DAC}$ ) of 12 GSPS. JRx mode of 15C (L = 8, M = 8, F = 2, S = 1, K = 128, E = 1, N = 16, NP = 16).

ADC datapath with a complex  $f_{IQ\_DATA}$  = 1500 MSPS, decimation of 2 $\times$ , and  $f_{ADC}$  of 3 GSPS. JT<sub>x</sub> mode of 16C (L = 8, M = 8, F = 2, S = 1, K = 128, E = 1, N = 16, NP = 16).

Note that the AD9988 does not support the option to bypass the CDUC in the transmit data path and the CDDC in the receive data path.

See the [UG-1578](#) user guide for further information on the JESD204B and JESD204C mode configurations, and a detailed description of the settings referenced throughout this data sheet. A table showing other operational modes and the corresponding typical and maximum power consumption numbers is included.

Table 2.

| Parameter                                                       | Test Conditions/Comments             | Min | Typ  | Max   | Unit |
|-----------------------------------------------------------------|--------------------------------------|-----|------|-------|------|
| CURRENTS                                                        |                                      |     |      |       |      |
| AVDD2 ( $I_{AVDD2}$ )                                           | 2.0 V supply                         |     | 190  | 205   | mA   |
| BVDD2 ( $I_{BVDD2}$ ) + RVDD2 ( $I_{RVDD2}$ )                   | 2.0 V supply                         |     | 295  | 350   | mA   |
| AVDD2_PLL ( $I_{AVDD2\_PLL}$ ) + SVDD2_PLL ( $I_{SVDD2\_PLL}$ ) | 2.0 V supply                         |     | 45   | 55    | mA   |
| Power Dissipation for 2 V Supplies                              | 2.0 V supply total power dissipation |     | 1.06 | 1.22  | W    |
| PLLCLKVDD1 ( $I_{PLLCLKVDD1}$ )                                 | 1.0 V supply                         |     | 15   | 25    | mA   |
| AVDD1 ( $I_{AVDD1}$ ) + DCLKVDD1 ( $I_{DCLKVDD1}$ )             | 1.0 V supply                         |     | 1000 | 1185  | mA   |
| AVDD1_ADC ( $I_{AVDD1\_ADC}$ )                                  | 1.0 V supply                         |     | 1620 | 1900  | mA   |
| CLKVDD1 ( $I_{CLKVDD1}$ )                                       | 1.0 V supply                         |     | 60   | 110   | mA   |
| FVDD1 ( $I_{FVDD1}$ )                                           | 1.0 V supply                         |     | 45   | 65    | mA   |
| VDD1_NVG ( $I_{VDD1\_NVG}$ )                                    | 1.0 V supply                         |     | 280  | 345   | mA   |
| DAVDD1 ( $I_{DAVDD1}$ )                                         | 1.0 V supply                         |     | 1590 | 1835  | mA   |
| DVDD1 ( $I_{DVDD1}$ )                                           | 1.0 V supply                         |     | 2780 | 3805  | mA   |
| DVDD1_RT ( $I_{DVDD1\_RT}$ )                                    | 1.0 V supply                         |     | 565  | 690   | mA   |
| SVDD1 ( $I_{SVDD1}$ ) + SVDD1_PLL ( $I_{SVDD1\_PLL}$ )          | 1.0 V supply                         |     | 1920 | 2570  | mA   |
| Power Dissipation for 1 V Supplies                              | 1.0 V supply total power dissipation |     | 9.88 | 12.53 | W    |

## SPECIFICATIONS

Table 2.

| Parameter                 | Test Conditions/Comments                        | Min | Typ   | Max   | Unit |
|---------------------------|-------------------------------------------------|-----|-------|-------|------|
| DVDD1P8 ( $I_{DVDD1P8}$ ) | 1.8 V supply                                    |     | 7     | 10    | mA   |
| Total Power Dissipation   | Total power dissipation of 2 V and 1 V supplies |     | 10.95 | 13.77 | W    |

## DAC DC SPECIFICATIONS

Nominal supplies with DAC output full-scale current ( $I_{OUTFS}$ ) = 26 mA, unless otherwise noted. ADC setup in 4 GSPS, full BW mode (all digital downconverters bypassed). For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$ , and for the typical values,  $T_A = 25^{\circ}\text{C}$ , which corresponds to  $T_J = 80^{\circ}\text{C}$ , unless otherwise noted.

Table 3. DAC DC Specifications

| Parameter                                                      | Test Conditions/Comments                                                                                                                                                                                         | Min  | Typ  | Max             | Unit     |
|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-----------------|----------|
| DAC RESOLUTION                                                 |                                                                                                                                                                                                                  | 16   |      |                 | Bit      |
| DAC ACCURACY                                                   |                                                                                                                                                                                                                  |      |      |                 |          |
| Gain Error                                                     |                                                                                                                                                                                                                  |      | 1.5  |                 | %FSR     |
| Gain Matching                                                  |                                                                                                                                                                                                                  |      | 0.7  |                 | %FSR     |
| Integral Nonlinearity (INL)                                    | Shuffling disabled                                                                                                                                                                                               |      | 8.0  |                 | LSB      |
| Differential Nonlinearity (DNL)                                | Shuffling disabled                                                                                                                                                                                               |      | 3.5  |                 | LSB      |
| DAC ANALOG OUTPUTS                                             | DACxP and DACxN                                                                                                                                                                                                  |      |      |                 |          |
| Full-Scale Output Current Range                                | AC coupling, setting resistance ( $R_{SET}$ ) = 5 k $\Omega$                                                                                                                                                     |      |      |                 |          |
| AC Coupling                                                    | Output common-mode voltage ( $V_{CM}$ ) = 0 V                                                                                                                                                                    | 6.43 | 26.5 | 37.75           | mA       |
| DC Coupling                                                    | 50 $\Omega$ shunt to a negative supply, forcing $V_{CM} = 0$ V                                                                                                                                                   | 6.43 |      | 37.75           | mA       |
| DC Coupling                                                    | 50 $\Omega$ shunt to GND, forcing $V_{CM} = 0.3$ V                                                                                                                                                               | 6.43 |      | 20 <sup>1</sup> | mA       |
| Full-Scale Sinewave Output Power with AC Coupling <sup>2</sup> | Ideal 2:1 balun interface to 50 $\Omega$                                                                                                                                                                         |      |      |                 |          |
| $I_{OUTFS} = 26$ mA                                            |                                                                                                                                                                                                                  |      | 3.3  |                 | dBm      |
| $I_{OUTFS} = 40$ mA                                            |                                                                                                                                                                                                                  |      | 7    |                 | dBm      |
| Common-Mode Output Voltage ( $V_{CMOUT}$ )                     |                                                                                                                                                                                                                  |      | 0    |                 | V        |
| AC Coupling                                                    | Bias each output to GND across a shunt inductor                                                                                                                                                                  |      | 0    |                 | V        |
| DC Coupling                                                    | Bias each output to a negative voltage rail across a 25 $\Omega$ to 200 $\Omega$ resistor, selected such that $V_{CMOUT} = 0$ V; $V_{CMOUT} = 0.3$ V is with a 25 $\Omega$ resistor to GND and $I_{FSC} = 20$ mA |      | 0    | 0.3             | V        |
| Differential Resistance                                        |                                                                                                                                                                                                                  |      | 100  |                 | $\Omega$ |

<sup>1</sup> For dc-coupled applications, the maximum full-scale output current is limited by the maximum  $V_{CMOUT}$  specification.

<sup>2</sup> The actual measured full-scale power is frequency dependent due to DAC sinc response, impedance mismatch loss, and balun insertion loss.

## SPECIFICATIONS

## ADC DC SPECIFICATIONS

Nominal supplies with DAC output full-scale current ( $I_{OUTFS}$ ) = 26 mA, unless otherwise noted. ADC setup in 4 GSPS, full BW mode (all digital downconverters bypassed). For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$ , and for the typical values,  $T_A = 25^{\circ}\text{C}$ , which corresponds to  $T_J = 80^{\circ}\text{C}$ , unless otherwise noted.

Table 4. ADC DC Specifications

| Parameter                                | Test Conditions/Comments                                                      | Min | Typ        | Max | Unit          |
|------------------------------------------|-------------------------------------------------------------------------------|-----|------------|-----|---------------|
| ADC RESOLUTION                           |                                                                               | 12  |            |     | Bit           |
| ADC ACCURACY                             |                                                                               |     |            |     |               |
| No Missing Codes                         |                                                                               |     | Guaranteed |     |               |
| Offset Error                             |                                                                               |     | -0.20      |     | %FSR          |
| Offset Matching                          |                                                                               |     | +0.05      |     | %FSR          |
| Gain Error                               |                                                                               |     | -0.71      |     | %FSR          |
| Gain Matching                            |                                                                               |     | +1.2       |     | %FSR          |
| DNL                                      |                                                                               |     | $\pm 1.9$  |     | LSB           |
| INL                                      |                                                                               |     | $\pm 0.5$  |     | LSB           |
| ADC ANALOG INPUTS                        | ADCxP and ADCxN                                                               |     |            |     |               |
| Differential Input Voltage               |                                                                               |     | 1.4        |     | V p-p         |
| Full-Scale Sine Wave Input Power         | Input power level resulting 0 dBFS tone level on fast Fourier transform (FFT) |     | 3.9        |     | dBm           |
| Common-Mode Input Voltage ( $V_{CMIN}$ ) | AC-coupled, equal to voltage at VCMx for ADCx input                           |     | 1          |     | V             |
| Differential Input Impedance             |                                                                               |     | 100//0.4   |     | $\Omega$ //pF |
| Return Loss                              | <2.7 GHz                                                                      |     | -4.3       |     | dB            |
|                                          | 2.7 GHz to 3.8 GHz                                                            |     | -3.6       |     | dB            |
|                                          | 3.8 GHz to 5.4 GHz                                                            |     | -2.9       |     | dB            |

## SPECIFICATIONS

## CLOCK INPUTS AND OUTPUTS

For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply, unless otherwise noted.

Table 5. Clock Input and Outputs

| Parameter                                          | Test Conditions/Comments | Min | Typ | Max      | Unit         |
|----------------------------------------------------|--------------------------|-----|-----|----------|--------------|
| CLOCK INPUTS                                       | CLKINP and CLKINN        |     |     |          |              |
| Differential Input Power                           | Direct RF clock          |     |     |          |              |
| Minimum                                            |                          |     |     | 0        | dBm          |
| Maximum                                            |                          |     |     | 6        | dBm          |
| Common-Mode Voltage                                | AC-coupled               |     |     | 0.5      | V            |
| Differential Input Impedance                       |                          |     |     | 100//0.3 | $\Omega$ /pF |
| CLOCK OUTPUTS (ADC CLOCK DRIVER)                   | ADCDRVP and ADCDRVN      |     |     |          |              |
| Differential Output Voltage Magnitude <sup>1</sup> | 1.5 GHz                  |     |     | 740      | mV p-p       |
|                                                    | 2.0 GHz                  |     |     | 690      | mV p-p       |
|                                                    | 3.0 GHz                  |     |     | 640      | mV p-p       |
|                                                    | 6.0 GHz                  |     |     | 490      | mV p-p       |
| Differential Output Resistance                     |                          |     |     | 100      | $\Omega$     |
| Common-Mode Voltage                                | AC-coupled               |     |     | 0.5      | $\Omega$     |

<sup>1</sup> Measured with differential 100  $\Omega$  load and less than 2 mm of printed circuit board (PCB) trace from package ball.

## CLOCK INPUT AND PHASE-LOCKED LOOP (PLL) FREQUENCY SPECIFICATIONS

For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply, unless otherwise noted.

Table 6.

| Parameter                                                | Test Conditions/Comments     | Min               | Typ | Max   | Unit |
|----------------------------------------------------------|------------------------------|-------------------|-----|-------|------|
| CLOCK INPUTS (CLKINP, CLKINN) FREQUENCY RANGES           |                              | 25                |     | 12000 | MHz  |
| PHASE FREQUENCY DETECTOR (PFD) INPUT FREQUENCY RANGES    |                              | 25                |     | 750   | MHz  |
| FREQUENCY RANGES ACCORDING TO CLOCK PATH CONFIGURATION   |                              |                   |     |       |      |
| Direct Clock (PLL Off)                                   |                              | 2900 <sup>1</sup> |     | 12000 | MHz  |
| PLL Reference Clock (PLL On)                             | M divider set to divide by 1 | 25                |     | 750   | MHz  |
|                                                          | M divider set to divide by 2 | 50                |     | 1500  | MHz  |
|                                                          | M divider set to divide by 3 | 75                |     | 2250  | MHz  |
|                                                          | M divider set to divide by 4 | 100               |     | 3000  | MHz  |
| PLL VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES |                              |                   |     |       |      |
| VCO Output                                               |                              |                   |     |       |      |
| Divide by 1                                              | D divider set to divide by 1 | 5.8               |     | 12    | GHz  |
| Divide by 2                                              | D divider set to divide by 2 | 2.9               |     | 6     | GHz  |
| Divide by 3                                              | D divider set to divide by 3 | 1.93333           |     | 4     | GHz  |
| Divide by 4                                              | D divider set to divide by 4 | 1.45              |     | 3     | GHz  |

<sup>1</sup> The minimum direct clock frequency is limited by the minimum DAC (core) sample rate, as specified in Table 7. The clock receiver can accommodate the full range between the minimum PLL reference clock frequency and the maximum direct clock frequency.

## DAC SAMPLE RATE SPECIFICATIONS

Nominal supplies. For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply. For the typical values,  $T_A = 25^{\circ}\text{C}$ , which corresponds to  $T_J = 80^{\circ}\text{C}$ , unless otherwise noted.

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Table 7. DAC Sample Rate Specifications

| Parameter                    | Min | Typ | Max | Unit |
|------------------------------|-----|-----|-----|------|
| DAC SAMPLE RATE <sup>1</sup> |     |     |     |      |
| Minimum                      |     |     | 2.9 | GSPS |
| Maximum                      | 12  |     |     | GSPS |

<sup>1</sup> Pertains to the update rate of the DAC core, independent of datapath and JESD204 mode configuration.



SPECIFICATIONS

ADC SAMPLE RATE SPECIFICATIONS

Nominal supplies. For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply. For the typical values,  $T_A = 25^{\circ}\text{C}$ , which corresponds to  $T_J = 80^{\circ}\text{C}$ , unless otherwise noted.

Table 8. ADC Sample Rate Specifications

| Parameter                    | Min | Typ | Max  | Unit   |
|------------------------------|-----|-----|------|--------|
| ADC SAMPLE RATE <sup>1</sup> |     |     |      |        |
| Minimum                      |     |     | 1.45 | GSPS   |
| Maximum                      | 4   |     |      | GSPS   |
| Aperture Jitter <sup>2</sup> |     | 65  |      | fs rms |

<sup>1</sup> Pertains to the update rate of the ADC core, independent of datapath and JESD204 mode configuration.

<sup>2</sup> Measured using a signal-to-noise ratio (SNR) degradation method with the DAC disabled, clock divider = 1, ADC frequency ( $f_{\text{ADC}}$ ) = 4 GSPS, and input frequency ( $f_{\text{IN}}$ ) = 5.55 GHz.

## SPECIFICATIONS

## INPUT DATA RATES SPECIFICATIONS

For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply, unless otherwise noted.

Table 9.

| Parameter <sup>1 2</sup>                                                 | Test Conditions/Comments                                                                                                                                                                                     | Min | Typ | Max  | Unit |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| MAXIMUM DATA RATE PER NUMBER OF ACTIVE DAC OUTPUTS                       | Single DAC, FDUC bypassed, 1 CDUC enabled (not bypassable), 12-bit or 16-bit resolution; limited by the maximum DAC clock rate and the minimum total interpolation of 2× inside the CDUC block               |     |     | 6000 | MSPS |
|                                                                          | Quad DAC, FDUC bypassed, 4 CDUCs enabled (not bypassable), 12-bit resolution; limited by the maximum JESD204C link throughput (M = 8, L = 8) and the minimum total interpolation of 2× inside the CDUC block |     |     | 2000 | MSPS |
| MAXIMUM COMPLEX (I/Q) DATA RATE PER NUMBER OF ACTIVE INPUT DATA CHANNELS | 1 channel: FDUC bypassed, 1 CDUC enabled, 12-bit or 16-bit resolution; limited by the maximum CDUC NCO clock rate                                                                                            |     |     | 6000 | MSPS |
|                                                                          | 2 channels: FDUC bypassed, 2 CDUCs enabled, 12-bit resolution; limited by the maximum JESD204C link throughput (M = 4, L = 8)                                                                                |     |     | 4000 | MSPS |
|                                                                          | 4 channels: FDUC bypassed, 4 CDUCs enabled, 12-bit resolution; limited by the maximum JESD204C link throughput (M = 8, L = 8)                                                                                |     |     | 2000 | MSPS |
|                                                                          | 8 channels: 8 FDUCs enabled, one or more CDUC enabled, 12-bit or 16-bit resolution; limited by the maximum FDUC NCO clock rate divided by the minimum 2x interpolation rate required to enable the FDUC      |     |     | 750  | MSPS |

<sup>1</sup> The values listed for these parameters are the maximum possible when considering all JESD204 modes of operation. Some modes are more limiting, based on other parameters.

<sup>2</sup> The interpolation filters in the Tx datapath have a total complex filter bandwidth of 80% of the data rate, combining the 40% bandwidth in the I path and 40% bandwidth in the Q path. Similarly, the decimation stages inside the Rx datapath use filters with a total complex filter bandwidth of 81.4%. Therefore, the maximum allowed instantaneous complex signal bandwidth (iBW) per channel is calculated as  $iBW = [\text{Complex I/Q Data Rate per Channel}] \times [\text{Total Complex Filter Bandwidth}]$ .

## SPECIFICATIONS

## NCO FREQUENCY SPECIFICATIONS

For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply, unless otherwise noted.

Table 10.

| Parameter                                                  | Test Conditions/Comments                                                | Min  | Typ | Max  | Unit |
|------------------------------------------------------------|-------------------------------------------------------------------------|------|-----|------|------|
| MAXIMUM NUMERICALLY CONTROLLED OSCILLATOR (NCO) CLOCK RATE |                                                                         |      |     |      |      |
| FDUC NCO                                                   |                                                                         |      |     | 1.5  | GHz  |
| CDUC NCO                                                   |                                                                         |      |     | 12   | GHz  |
| FDDC NCO                                                   |                                                                         |      |     | 1.5  | GHz  |
| CDDC NCO                                                   |                                                                         |      |     | 4    | GHz  |
| MAXIMUM NCO SHIFT FREQUENCY RANGE                          |                                                                         |      |     |      |      |
| FDUC NCO                                                   | channel interpolation rate must be $> 1\times$                          | -750 |     | +750 | MHz  |
| CDUC NCO                                                   | $f_{DAC} = 12\text{ GHz}$ , main interpolation rate must be $> 1\times$ | -6   |     | +6   | GHz  |
| FDDC NCO                                                   | channel decimation rate must be $> 1\times$                             | -750 |     | +750 | MHz  |
| CDDC NCO                                                   | $f_{ADC} = 4\text{ GHz}$ , main decimation rate must be $> 1\times$     | -2   |     | +2   | GHz  |
| MAXIMUM FREQUENCY SPACING BETWEEN CHANNELIZER CHANNELS     |                                                                         |      |     |      |      |
| Tx FDUC Channels                                           | Maximum FDUC NCO clock rate $\times 0.8^1$                              |      |     | 1200 | MHz  |
| Rx FDDC Channels                                           | Maximum FDDC NCO clock rate $\times 0.814^2$                            |      |     | 1221 | MHz  |

<sup>1</sup> The 0.8 factor is because the total complex pass-band of the first interpolation filter is 80% of the filter input data rate.

<sup>2</sup> The 0.814 factor is because the total complex pass-band of the decimation filter is 81.4% of the filter output data rate.

## JESD204B AND JESD204C INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

Nominal supplies. For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$  and  $\pm 5\%$  of nominal supply, and for the typical values,  $T_A = 25^{\circ}\text{C}$ , which corresponds to  $T_J = 80^{\circ}\text{C}$ , unless otherwise noted.

Table 11. Serial Interface Rate Specifications

| Parameter                      | Test Conditions/Comments                      | Min  | Typ | Max    | Unit |
|--------------------------------|-----------------------------------------------|------|-----|--------|------|
| JESD204B SERIAL INTERFACE RATE | Serial lane rate (bit repeat option disabled) | 1.0  |     | 15.5   | Gbps |
| Unit Interval                  |                                               | 64.5 |     | 1000.0 | ps   |
| JESD204C SERIAL INTERFACE RATE | Serial lane rate (bit repeat option disabled) | 6.0  |     | 24.75  | Gbps |
| Unit Interval                  |                                               | 40.4 |     | 166.67 | ps   |

Table 12. JESD204 Receiver (JR<sub>x</sub>) Electrical Specifications

| Parameter                                  | Test Conditions/Comments                | Min | Typ                                              | Max | Unit   |
|--------------------------------------------|-----------------------------------------|-----|--------------------------------------------------|-----|--------|
| JESD204x DATA INPUTS                       | SERDIN <sub>x</sub> ±, where x = 0 to 7 |     |                                                  |     |        |
| Standards Compliance                       |                                         |     | JESD204B and JESD204C                            |     |        |
| Differential Voltage, $R_{V\text{DIFF}}$   |                                         |     | 800                                              |     | mV p-p |
| Differential Impedance, $Z_{R\text{DIFF}}$ | At dc                                   |     | 98                                               |     | Ω      |
| Termination Voltage, $V_{TT}$              | AC-coupled                              |     | 0.97                                             |     | V      |
| SYNCxOUTB± OUTPUTS <sup>1</sup>            | Where x = 0 or 1                        |     |                                                  |     |        |
| Output Differential Voltage, $V_{OD}$      | Driving 100 Ω differential load         |     | 400                                              |     | mV     |
| Output Offset Voltage, $V_{OS}$            |                                         |     | DVDD1P8/2 + 0.2                                  |     | V      |
| SYNCxOUTB+ OUTPUT                          | CMOS output option                      |     | Refer to <a href="#">CMOS Pin Specifications</a> |     |        |

<sup>1</sup> IEEE 1596.3 standard LVDS compatible.

Table 13. JESD204 Transmitter (JT<sub>x</sub>) Electrical Specifications

| Parameter             | Test Conditions/Comments                 | Min | Typ | Max | Unit |
|-----------------------|------------------------------------------|-----|-----|-----|------|
| JESD204x DATA OUTPUTS | SERDOUT <sub>x</sub> ±, where x = 0 to 7 |     |     |     |      |

## SPECIFICATIONS

Table 13. JESD204 Transmitter (JT<sub>x</sub>) Electrical Specifications

| Parameter                          | Test Conditions/Comments   | Min | Typ                                              | Max  | Unit   |
|------------------------------------|----------------------------|-----|--------------------------------------------------|------|--------|
| Standards Compliance               |                            |     | JESD204B and JESD204C                            |      |        |
| Differential Output Voltage        | Maximum strength           |     | 675                                              |      | mV p-p |
| Differential Termination Impedance |                            | 80  | 108                                              | 120  | Ω      |
| Rise Time, $t_R$                   | 20% to 80% into 100 Ω load |     | 18                                               |      | ps     |
| Fall Time, $t_F$                   | 20% to 80% into 100 Ω load |     | 18                                               |      | ps     |
| SYNCxINB± INPUT <sup>1</sup>       | Where x = 0 or 1           |     |                                                  |      |        |
| Logic Compliance                   |                            |     | LVDS                                             |      |        |
| Differential Input Voltage         |                            | 240 | 0.7                                              | 1900 | mV p-p |
| Input Common-Mode Voltage          | DC-coupled                 |     | 0.675                                            | 2    | V      |
| $R_{IN}$ (Differential)            |                            |     | 18                                               |      | kΩ     |
| Input Capacitance (Differential)   |                            |     | 1                                                |      | pF     |
| SYNCxINB+ INPUT                    | CMOS input option          |     | Refer to <a href="#">CMOS Pin Specifications</a> |      |        |

<sup>1</sup> IEEE 1596.3 standard LVDS compatible.

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Table 14. SYSREF Electrical Specifications

| Parameter                                | Test Conditions/Comments | Min | Typ                      | Max | Unit     |
|------------------------------------------|--------------------------|-----|--------------------------|-----|----------|
| SYSREF+ AND SYSREF- INPUTS               |                          |     |                          |     |          |
| Logic Compliance                         |                          |     | LVDS/LVPECL <sup>1</sup> |     |          |
| Differential Input Voltage               |                          |     | 0.7                      | 1.9 | V p-p    |
| Input Common-Mode Voltage Range          | DC-coupled               |     | 0.675                    | 2   | V        |
| Input Reference, $R_{IN}$ (Differential) |                          |     | 100                      |     | $\Omega$ |
| Input Capacitance (Differential)         |                          |     | 1                        |     | pF       |

<sup>1</sup> LVDS means low voltage differential signaling and LVPECL means low voltage positive/pseudo emitter-coupled logic.

## SPECIFICATIONS

## CMOS PIN SPECIFICATIONS

For the minimum and maximum values,  $T_J = -40^{\circ}\text{C}$  to  $+120^{\circ}\text{C}$ ,  $1.7\text{ V} \leq \text{DVDD1P8} \leq 2.1\text{ V}$ , other supplies nominal, unless otherwise noted.

Table 15.

| Parameter         | Symbol   | Test Conditions/Comments                                                                         | Min                          | Typ | Max                         | Unit       |
|-------------------|----------|--------------------------------------------------------------------------------------------------|------------------------------|-----|-----------------------------|------------|
| INPUTS            |          | SDIO, SCLK, CSB, RESETB, RXEN0, RXEN1, TXEN0, TXEN1, SYNC0INB $\pm$ , SYNC1INB $\pm$ , and GPIOx |                              |     |                             |            |
| Logic 1 Voltage   | $V_{IH}$ |                                                                                                  | $0.70 \times \text{DVDD1P8}$ |     |                             | V          |
| Logic 0 Voltage   | $V_{IL}$ |                                                                                                  |                              |     | $0.3 \times \text{DVDD1P8}$ | V          |
| Input Resistance  |          |                                                                                                  | 40                           |     |                             | k $\Omega$ |
| OUTPUTS           |          | SDIO, SDO, GPIOx, ADCx_FDX, ADCx_SMONx, SYNC0OUTB $\pm$ , and SYNC1OUTB $\pm$ , 4 mA load        |                              |     |                             |            |
| Logic 1 Voltage   | $V_{OH}$ |                                                                                                  | $\text{DVDD1P8} - 0.45$      |     |                             | V          |
| Logic 0 Voltage   | $V_{OL}$ |                                                                                                  |                              |     | 0.45                        | V          |
| INTERRUPT OUTPUTS |          | IRQB_0 and IRQB_1, pull-up resistor of 5 k $\Omega$ to DVDD1P8                                   |                              |     |                             |            |
| Logic 1 Voltage   | $V_{OH}$ |                                                                                                  | 1.35                         |     |                             | V          |
| Logic 0 Voltage   | $V_{OL}$ |                                                                                                  |                              |     | 0.48                        | V          |

## DAC AC SPECIFICATIONS

Nominal supplies with  $T_A = 25^{\circ}\text{C}$ . Specifications represent the average of all four DAC channels with the DAC  $I_{OUTFS} = 26\text{ mA}$ , unless otherwise noted.

Table 16.

| Parameter                                      | Test Conditions/Comments                            | Min | Typ | Max | Unit |
|------------------------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| SPURIOUS-FREE DYNAMIC RANGE (SFDR)             |                                                     |     |     |     |      |
| Single-Tone, $f_{DAC} = 12\text{ GSPS}$        | -7 dBFS digital back off, shuffle enabled, 15C mode |     |     |     |      |
| Output Frequency ( $f_{OUT}$ ) = 70 MHz        |                                                     | 63  | 80  |     | dBc  |
| $f_{OUT} = 100\text{ MHz}$                     |                                                     |     | 77  |     | dBc  |
| $f_{OUT} = 500\text{ MHz}$                     |                                                     |     | 76  |     | dBc  |
| $f_{OUT} = 900\text{ MHz}$                     |                                                     |     | 77  |     | dBc  |
| $f_{OUT} = 1900\text{ MHz}$                    |                                                     | 61  | 79  |     | dBc  |
| $f_{OUT} = 2600\text{ MHz}$                    |                                                     |     | 75  |     | dBc  |
| $f_{OUT} = 3700\text{ MHz}$                    |                                                     |     | 69  |     | dBc  |
| $f_{OUT} = 4500\text{ MHz}$                    |                                                     |     | 68  |     | dBc  |
| Single-Tone, $f_{DAC} = 9\text{ GSPS}$         | -7 dBFS digital back off, shuffle enabled, 15C mode |     |     |     |      |
| $f_{OUT} = 100\text{ MHz}$                     |                                                     |     | 78  |     | dBc  |
| $f_{OUT} = 500\text{ MHz}$                     |                                                     |     | 78  |     | dBc  |
| $f_{OUT} = 900\text{ MHz}$                     |                                                     |     | 77  |     | dBc  |
| $f_{OUT} = 1900\text{ MHz}$                    |                                                     |     | 80  |     | dBc  |
| $f_{OUT} = 2600\text{ MHz}$                    |                                                     |     | 80  |     | dBc  |
| $f_{OUT} = 3700\text{ MHz}$                    |                                                     |     | 72  |     | dBc  |
| Single-Tone, $f_{DAC} = 6\text{ GSPS}$         | -7 dBFS digital back off, shuffle enabled, 15C mode |     |     |     |      |
| $f_{OUT} = 100\text{ MHz}$                     |                                                     |     | 84  |     | dBc  |
| $f_{OUT} = 500\text{ MHz}$                     |                                                     |     | 81  |     | dBc  |
| $f_{OUT} = 900\text{ MHz}$                     |                                                     |     | 82  |     | dBc  |
| $f_{OUT} = 1900\text{ MHz}$                    |                                                     |     | 81  |     | dBc  |
| ADJACENT CHANNEL LEAKAGE RATIO                 |                                                     |     |     |     |      |
| Single Carrier 20 MHz LTE Downlink Test Vector | -1 dBFS digital back off, 256 QAM                   |     |     |     |      |
| $f_{DAC} = 12\text{ GSPS}$                     | $f_{OUT} = 1840\text{ MHz}$                         |     | 77  |     | dBc  |
|                                                | $f_{OUT} = 2650\text{ MHz}$                         |     | 76  |     | dBc  |

## SPECIFICATIONS

Table 16.

| Parameter                                                                                  | Test Conditions/Comments | Min  | Typ | Max | Unit   |
|--------------------------------------------------------------------------------------------|--------------------------|------|-----|-----|--------|
| $f_{DAC} = 9$ GSPS                                                                         | $f_{OUT} = 3500$ MHz     |      | 73  |     | dBc    |
|                                                                                            | $f_{OUT} = 1900$ MHz     |      | 77  |     | dBc    |
|                                                                                            | $f_{OUT} = 2650$ MHz     |      | 77  |     | dBc    |
| $f_{DAC} = 6$ GSPS                                                                         | $f_{OUT} = 750$ MHz      |      | 79  |     | dBc    |
|                                                                                            | $f_{OUT} = 1840$ MHz     |      | 77  |     | dBc    |
| THIRD-ORDER INTERMODULATION DISTORTION (IMD3)                                              |                          |      |     |     |        |
| Two tone test, 1 MHz spacing, 0 dBFS digital back off, -6 dBFS per tone                    |                          |      |     |     |        |
| $f_{DAC} = 12$ GSPS                                                                        | $f_{OUT} = 1900$ MHz     | -69  |     | -62 | dBc    |
|                                                                                            | $f_{OUT} = 2600$ MHz     | -72  |     |     | dBc    |
|                                                                                            | $f_{OUT} = 3700$ MHz     | -72  |     |     | dBc    |
| $f_{DAC} = 9$ GSPS                                                                         | $f_{OUT} = 1900$ MHz     | -79  |     |     | dBc    |
|                                                                                            | $f_{OUT} = 2600$ MHz     | -76  |     |     | dBc    |
| $f_{DAC} = 6$ GSPS                                                                         | $f_{OUT} = 900$ MHz      | -79  |     |     | dBc    |
|                                                                                            | $f_{OUT} = 1900$ MHz     | -90  |     |     | dBc    |
| NOISE SPECTRAL DENSITY (NSD)                                                               |                          |      |     |     |        |
| 0 dBFS, NSD measurement taken at 10% away from $f_{OUT}$ , shuffle off                     |                          |      |     |     |        |
| Single-Tone, $f_{DAC} = 12$ GSPS                                                           |                          |      |     |     |        |
| $f_{OUT} = 150$ MHz                                                                        |                          | -168 |     |     | dBc/Hz |
| $f_{OUT} = 500$ MHz                                                                        |                          | -167 |     |     | dBc/Hz |
| $f_{OUT} = 950$ MHz                                                                        |                          | -165 |     |     | dBc/Hz |
| $f_{OUT} = 1840$ MHz                                                                       |                          | -162 |     |     | dBc/Hz |
| $f_{OUT} = 2650$ MHz                                                                       |                          | -160 |     |     | dBc/Hz |
| $f_{OUT} = 3700$ MHz                                                                       |                          | -155 |     |     | dBc/Hz |
| $f_{OUT} = 4500$ MHz                                                                       |                          | -154 |     |     | dBc/Hz |
| Single-Tone, $f_{DAC} = 9$ GSPS                                                            |                          |      |     |     |        |
| $f_{OUT} = 150$ MHz                                                                        |                          | -168 |     |     | dBc/Hz |
| $f_{OUT} = 500$ MHz                                                                        |                          | -166 |     |     | dBc/Hz |
| $f_{OUT} = 950$ MHz                                                                        |                          | -164 |     |     | dBc/Hz |
| $f_{OUT} = 1840$ MHz                                                                       |                          | -160 |     |     | dBc/Hz |
| $f_{OUT} = 2650$ MHz                                                                       |                          | -158 |     |     | dBc/Hz |
| $f_{OUT} = 3700$ MHz                                                                       |                          | -154 |     |     | dBc/Hz |
| Single-Tone, $f_{DAC} = 6$ GSPS                                                            |                          |      |     |     |        |
| $f_{OUT} = 150$ MHz                                                                        |                          | -168 |     |     | dBc/Hz |
| $f_{OUT} = 500$ MHz                                                                        |                          | -165 |     |     | dBc/Hz |
| $f_{OUT} = 950$ MHz                                                                        |                          | -163 |     |     | dBc/Hz |
| $f_{OUT} = 1840$ MHz                                                                       |                          | -159 |     |     | dBc/Hz |
| $f_{OUT} = 2650$ MHz                                                                       |                          | -157 |     |     | dBc/Hz |
| SINGLE SIDEBAND PHASE NOISE OFFSET (PLL DISABLED)                                          |                          |      |     |     |        |
| Direct device clock input at 6 dBm<br>Rohde & Schwarz SMA100B B711 option                  |                          |      |     |     |        |
| $f_{OUT} = 3.6$ GHz, $f_{DAC} = 12$ GSPS, CLKINx Frequency ( $f_{CLKIN}$ ) = 12 GHz        |                          |      |     |     |        |
| 1 kHz                                                                                      |                          | -118 |     |     | dBc/Hz |
| 10 kHz                                                                                     |                          | -129 |     |     | dBc/Hz |
| 100 kHz                                                                                    |                          | -137 |     |     | dBc/Hz |
| 600 kHz                                                                                    |                          | -144 |     |     | dBc/Hz |
| 1.2 MHz                                                                                    |                          | -148 |     |     | dBc/Hz |
| 1.8 MHz                                                                                    |                          | -149 |     |     | dBc/Hz |
| 6 MHz                                                                                      |                          | -153 |     |     | dBc/Hz |
| SINGLE SIDEBAND PHASE NOISE OFFSET (PLL ENABLED)                                           |                          |      |     |     |        |
| Loop filter component values include<br>$C1 = 22$ nF, $R1 = 226$ $\Omega$ , $C2 = 2.2$ nF, |                          |      |     |     |        |

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Table 16.

| Parameter                                                                                 | Test Conditions/Comments                                 | Min | Typ  | Max | Unit   |
|-------------------------------------------------------------------------------------------|----------------------------------------------------------|-----|------|-----|--------|
| $f_{OUT} = 1.8 \text{ GHz}$ , $f_{DAC} = 12 \text{ GSPS}$ , $f_{CLKIN} = 0.5 \text{ GHz}$ | C3 = 33 nF, and phase detector frequency (PFD) = 500 MHz |     |      |     |        |
| 1 kHz                                                                                     |                                                          |     | -106 |     | dBc/Hz |
| 10 kHz                                                                                    |                                                          |     | -113 |     | dBc/Hz |
| 100 kHz                                                                                   |                                                          |     | -120 |     | dBc/Hz |
| 600 kHz                                                                                   |                                                          |     | -127 |     | dBc/Hz |
| 1.2 MHz                                                                                   |                                                          |     | -134 |     | dBc/Hz |
| 1.8 MHz                                                                                   |                                                          |     | -138 |     | dBc/Hz |
| 6 MHz                                                                                     |                                                          |     | -150 |     | dBc/Hz |

## ADC AC SPECIFICATIONS

Nominal supplies with  $T_A = 25^\circ\text{C}$ . Input amplitude ( $A_{IN}$ ) = -1 dBFS, full bandwidth (no decimation) mode. For the minimum and maximum values,  $T_J = -40^\circ\text{C}$  to  $+120^\circ\text{C}$ . Specifications represent average of four ADC channels with DACs powered on. See the [AN-835 Application Note](#), *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

Table 17.

| Parameter                              | 3 GSPS |                      |     | 4 GSPS |                     |     | Unit    |
|----------------------------------------|--------|----------------------|-----|--------|---------------------|-----|---------|
|                                        | Min    | Typ                  | Max | Min    | Typ                 | Max |         |
| NOISE DENSITY <sup>1</sup>             |        | -150.3               |     |        | -151.5              |     | dBFS/Hz |
| NOISE FIGURE <sup>2</sup>              |        | 28                   |     |        | 26.8                |     | dB      |
| CODE ERROR RATE (CER)                  |        | $<1 \times 10^{-30}$ |     |        | $1 \times 10^{-20}$ |     | Errors  |
| SIGNAL-TO-NOISE RATIO (SNR)            |        |                      |     |        |                     |     |         |
| $f_{IN} = 450 \text{ MHz}$             |        | 57.8                 |     |        | 57.9                |     | dBFS    |
| $f_{IN} = 900 \text{ MHz}$             |        | 57.7                 |     |        | 57.5                |     | dBFS    |
| $f_{IN} = 1800 \text{ MHz}$            |        | 56.9                 |     |        | 56.0                |     | dBFS    |
| $f_{IN} = 2700 \text{ MHz}$            |        | 55.9                 |     | 52.4   | 54.5                |     | dBFS    |
| $f_{IN} = 3600 \text{ MHz}$            |        | 55.1                 |     |        | 52.9                |     | dBFS    |
| $f_{IN} = 4500 \text{ MHz}$            |        | 53.9                 |     |        | 51.4                |     | dBFS    |
| $f_{IN} = 5400 \text{ MHz}$            |        | 53.2                 |     |        | 50.5                |     | dBFS    |
| $f_{IN} = 6300 \text{ MHz}$            |        | 52.3                 |     |        | 49.3                |     | dBFS    |
| $f_{IN} = 7200 \text{ MHz}$            |        | 51.3                 |     |        | 48.5                |     | dBFS    |
| SIGNAL-TO-NOISE-AND-DISTORTION (SINAD) |        |                      |     |        |                     |     |         |
| $f_{IN} = 450 \text{ MHz}$             |        | 57.5                 |     |        | 57.7                |     | dBFS    |
| $f_{IN} = 900 \text{ MHz}$             |        | 57.2                 |     |        | 57.3                |     | dBFS    |
| $f_{IN} = 1800 \text{ MHz}$            |        | 56.1                 |     |        | 55.8                |     | dBFS    |
| $f_{IN} = 2700 \text{ MHz}$            |        | 54.5                 |     | 51.0   | 54.2                |     | dBFS    |
| $f_{IN} = 3600 \text{ MHz}$            |        | 53.2                 |     |        | 52.3                |     | dBFS    |
| $f_{IN} = 4500 \text{ MHz}$            |        | 48.4                 |     |        | 50.1                |     | dBFS    |
| $f_{IN} = 5400 \text{ MHz}$            |        | 47.8                 |     |        | 48.6                |     | dBFS    |
| $f_{IN} = 6300 \text{ MHz}$            |        | 46.1                 |     |        | 45.5                |     | dBFS    |
| $f_{IN} = 7200 \text{ MHz}$            |        | 44.8                 |     |        | 44.3                |     | dBFS    |
| SECOND-ORDER HARMONIC DISTORTION (HD2) |        |                      |     |        |                     |     |         |
| $f_{IN} = 450 \text{ MHz}$             |        | -73                  |     |        | -86                 |     | dBFS    |
| $f_{IN} = 900 \text{ MHz}$             |        | -76                  |     |        | -78                 |     | dBFS    |
| $f_{IN} = 1800 \text{ MHz}$            |        | -71                  |     |        | -78                 |     | dBFS    |
| $f_{IN} = 2700 \text{ MHz}$            |        | -65                  |     |        | -67                 | -53 | dBFS    |
| $f_{IN} = 3600 \text{ MHz}$            |        | -61                  |     |        | -61                 |     | dBFS    |
| $f_{IN} = 4500 \text{ MHz}$            |        | -55                  |     |        | -56                 |     | dBFS    |



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Table 17.

| Parameter                                                                                 | 3 GSPS |     |     | 4 GSPS |     |     | Unit |
|-------------------------------------------------------------------------------------------|--------|-----|-----|--------|-----|-----|------|
|                                                                                           | Min    | Typ | Max | Min    | Typ | Max |      |
| $f_{IN} = 5400 \text{ MHz}$                                                               |        | -50 |     |        | -53 |     | dBFS |
| $f_{IN} = 6300 \text{ MHz}$                                                               |        | -48 |     |        | -48 |     | dBFS |
| $f_{IN} = 7200 \text{ MHz}$                                                               |        | -46 |     |        | -46 |     | dBFS |
| THIRD-ORDER HARMONIC DISTORTION (HD3)                                                     |        |     |     |        |     |     |      |
| $f_{IN} = 450 \text{ MHz}$                                                                |        | -78 |     |        | -76 |     | dBFS |
| $f_{IN} = 900 \text{ MHz}$                                                                |        | -79 |     |        | -76 |     | dBFS |
| $f_{IN} = 1800 \text{ MHz}$                                                               |        | -78 |     |        | -75 |     | dBFS |
| $f_{IN} = 2700 \text{ MHz}$                                                               |        | -76 |     |        | -73 | -66 | dBFS |
| $f_{IN} = 3600 \text{ MHz}$                                                               |        | -71 |     |        | -76 |     | dBFS |
| $f_{IN} = 4500 \text{ MHz}$                                                               |        | -62 |     |        | -64 |     | dBFS |
| $f_{IN} = 5400 \text{ MHz}$                                                               |        | -60 |     |        | -60 |     | dBFS |
| $f_{IN} = 6300 \text{ MHz}$                                                               |        | -59 |     |        | -57 |     | dBFS |
| $f_{IN} = 7200 \text{ MHz}$                                                               |        | -58 |     |        | -54 |     | dBFS |
| WORST OTHER, EXCLUDING HD2, HD3, AND INTERLEAVING SPURS                                   |        |     |     |        |     |     |      |
| $f_{IN} = 450 \text{ MHz}$                                                                |        | -78 |     |        | -88 |     | dBFS |
| $f_{IN} = 900 \text{ MHz}$                                                                |        | -78 |     |        | -87 |     | dBFS |
| $f_{IN} = 1800 \text{ MHz}$                                                               |        | -78 |     |        | -81 |     | dBFS |
| $f_{IN} = 2700 \text{ MHz}$                                                               |        | -78 |     |        | -79 | -64 | dBFS |
| $f_{IN} = 3600 \text{ MHz}$                                                               |        | -78 |     |        | -77 |     | dBFS |
| $f_{IN} = 4500 \text{ MHz}$                                                               |        | -77 |     |        | -75 |     | dBFS |
| $f_{IN} = 5400 \text{ MHz}$                                                               |        | -78 |     |        | -74 |     | dBFS |
| $f_{IN} = 6300 \text{ MHz}$                                                               |        | -74 |     |        | -72 |     | dBFS |
| $f_{IN} = 7200 \text{ MHz}$                                                               |        | -73 |     |        | -72 |     | dBFS |
| INTERLEAVING SPUR ( $f_{IN} \pm f_S/2$ ) <sup>3</sup>                                     |        |     |     |        |     |     |      |
| $f_{IN} = 450 \text{ MHz}$                                                                |        | -97 |     |        | -93 |     | dBFS |
| $f_{IN} = 900 \text{ MHz}$                                                                |        | -94 |     |        | -93 |     | dBFS |
| $f_{IN} = 1800 \text{ MHz}$                                                               |        | -96 |     |        | -90 |     | dBFS |
| $f_{IN} = 2700 \text{ MHz}$                                                               |        | -86 |     |        | -86 |     | dBFS |
| $f_{IN} = 3600 \text{ MHz}$                                                               |        | -84 |     |        | -81 |     | dBFS |
| $f_{IN} = 4500 \text{ MHz}$                                                               |        | -53 |     |        | -85 |     | dBFS |
| $f_{IN} = 5400 \text{ MHz}$                                                               |        | -78 |     |        | -86 |     | dBFS |
| $f_{IN} = 6300 \text{ MHz}$                                                               |        | -77 |     |        | -79 |     | dBFS |
| $f_{IN} = 7200 \text{ MHz}$                                                               |        | -78 |     |        | -74 |     | dBFS |
| DIGITAL COUPLING SPUR ( $f_{IN} \pm f_S/4$ )                                              |        |     |     |        |     |     |      |
| $f_{IN} = 450 \text{ MHz}$                                                                |        | -83 |     |        | -94 |     | dBFS |
| $f_{IN} = 900 \text{ MHz}$                                                                |        | -79 |     |        | -91 |     | dBFS |
| $f_{IN} = 1800 \text{ MHz}$                                                               |        | -73 |     |        | -89 |     | dBFS |
| $f_{IN} = 2700 \text{ MHz}$                                                               |        | -70 |     |        | -86 | -67 | dBFS |
| $f_{IN} = 3600 \text{ MHz}$                                                               |        | -68 |     |        | -87 |     | dBFS |
| $f_{IN} = 4500 \text{ MHz}$                                                               |        | -66 |     |        | -83 |     | dBFS |
| $f_{IN} = 5400 \text{ MHz}$                                                               |        | -65 |     |        | -82 |     | dBFS |
| $f_{IN} = 6300 \text{ MHz}$                                                               |        | -64 |     |        | -80 |     | dBFS |
| $f_{IN} = 7200 \text{ MHz}$                                                               |        | -63 |     |        | -79 |     | dBFS |
| TWO-TONE INTERMODULATION DISTORTION (IMD3, $2f_{IN1} - f_{IN2}$ OR $2f_{IN2} - f_{IN1}$ ) |        |     |     |        |     |     |      |
| $A_{IN1}$ AND $A_{IN2} = -7 \text{ dBFS}$                                                 |        |     |     |        |     |     |      |
| $f_{IN1} = 1775 \text{ MHz}, f_{IN2} = 1825 \text{ MHz}$                                  |        | -81 |     |        | -84 |     | dBFS |
| $f_{IN1} = 2675 \text{ MHz}, f_{IN2} = 2725 \text{ MHz}$                                  |        | -77 |     |        | -78 |     | dBFS |

## SPECIFICATIONS

Table 17.

| Parameter                                                   | 3 GSPS |     |     | 4 GSPS |     |     | Unit |
|-------------------------------------------------------------|--------|-----|-----|--------|-----|-----|------|
|                                                             | Min    | Typ | Max | Min    | Typ | Max |      |
| $f_{IN1} = 3575 \text{ MHz}$ , $f_{IN2} = 3625 \text{ MHz}$ |        | -73 |     |        | -74 |     | dBFS |
| $f_{IN1} = 5375 \text{ MHz}$ , $f_{IN2} = 5425 \text{ MHz}$ |        | -66 |     |        | -66 |     | dBFS |
| ANALOG BANDWIDTH <sup>4</sup>                               |        | 7.5 |     |        | 7.5 |     | GHz  |

<sup>1</sup> Noise density is measured at 250 MHz input frequency at -30 dBFS, where timing jitter does not degrade noise floor.

<sup>2</sup> Noise figure is based on a nominal full-scale input power of 4.5 dBm with an input span of 1.4 V p-p and  $R_{IN} = 100 \Omega$ .

<sup>3</sup> With background interleaving calibration converged.

<sup>4</sup> Analog input bandwidth is the bandwidth of operation in which the full-scale input frequency response rolls off by -3 dB based on a de-embedded model of the ADC extracted from the measured frequency response on evaluation board. This bandwidth requires optimized matching network to achieve this upper bandwidth.

## TIMING SPECIFICATIONS

For the minimum and maximum values,  $T_J = -40^\circ\text{C}$  to  $+120^\circ\text{C}$  and  $\pm 5\%$  of nominal supply, unless otherwise noted.

Table 18.

| Parameter                                   | Symbol                    | Test Conditions/Comments                    | Min | Typ | Max | Unit |
|---------------------------------------------|---------------------------|---------------------------------------------|-----|-----|-----|------|
| SERIAL PORT INTERFACE (SPI) WRITE OPERATION |                           |                                             |     |     |     |      |
| Maximum SCLK Clock Rate                     | $f_{SCLK}$ , $1/t_{SCLK}$ |                                             | 33  |     |     | MHz  |
| SCLK Clock High                             | $t_{PWH}$                 | SCLK = 33 MHz                               | 8   |     |     | ns   |
| SCLK Clock Low                              | $t_{PWL}$                 | SCLK = 33 MHz                               | 8   |     |     | ns   |
| SDIO to SCLK Setup Time                     | $t_{DS}$                  |                                             | 4   |     |     | ns   |
| SCLK to SDIO Hold Time                      | $t_{DH}$                  |                                             | 4   |     |     | ns   |
| CSB to SCLK Setup Time                      | $t_S$                     |                                             | 4   |     |     | ns   |
| CLK to CSB Hold Time                        | $t_H$                     |                                             | 4   |     |     | ns   |
| SPI READ OPERATION                          |                           |                                             |     |     |     |      |
| LSB First Data Format                       |                           |                                             |     |     |     |      |
| Maximum SCLK Clock Rate                     | $f_{SCLK}$ , $1/t_{SCLK}$ |                                             | 33  |     |     | MHz  |
| SCLK Clock High                             | $t_{PWH}$                 |                                             | 8   |     |     | ns   |
| SCLK Clock Low                              | $t_{PWL}$                 |                                             | 8   |     |     | ns   |
| MSB First Data Format                       |                           |                                             |     |     |     |      |
| Maximum SCLK Clock Rate                     | $f_{SCLK}$ , $1/t_{SCLK}$ |                                             | 15  |     |     | MHz  |
| SCLK Clock High                             | $t_{PWH}$                 |                                             | 30  |     |     | ns   |
| SCLK Clock Low                              | $t_{PWL}$                 |                                             | 30  |     |     | ns   |
| SDIO to SCLK Setup Time                     | $t_{DS}$                  |                                             | 4   |     |     | ns   |
| SCLK to SDIO Hold Time                      | $t_{DH}$                  |                                             | 4   |     |     | ns   |
| CSB to SCLK Setup Time                      | $t_S$                     |                                             | 4   |     |     | ns   |
| SCLK to SDIO Data Valid Time                | $t_{DV}$                  |                                             | 20  |     |     | ns   |
| SCLK to SDO Data Valid Time                 | $t_{DV\_SDO}$             |                                             | 20  |     |     | ns   |
| CSB to SDIO Output Valid to High-Z          | $t_Z$                     |                                             | 20  |     |     | ns   |
| CSB to SDO Output Valid to High-Z           | $t_{Z\_SDO}$              |                                             | 20  |     |     | ns   |
| RESETB                                      |                           | Minimum hold time to trigger a device reset | 40  |     |     | ns   |

SPECIFICATIONS

Timing Diagrams

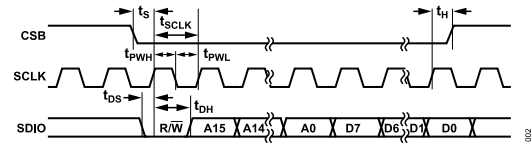


Figure 2. Timing Diagram for 3-Wire Write Operation

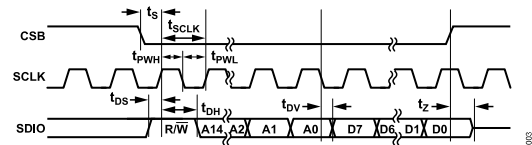


Figure 3. Timing Diagram for 3-Wire Read Operation

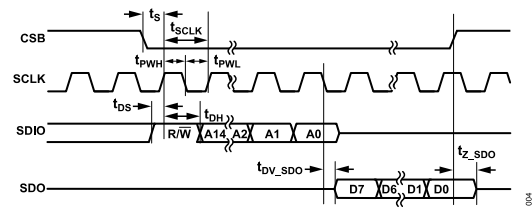


Figure 4. Timing Diagram for 4-Wire Read Operation

## ABSOLUTE MAXIMUM RATINGS

Table 19.

| Parameter                                                                                                                                                                                                                                                                        | Rating                       |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| IS <sub>ET</sub> , DAC <sub>xP</sub> , DAC <sub>xN</sub> , TDP, TDN                                                                                                                                                                                                              | −0.3 V to AVDD2 + 0.3 V      |
| VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG                                                                                                                                                                                                                                          | −0.3 V to AVDD2_PLL + 0.3 V  |
| R <sub>x</sub> Input Power (ADC0P/N, ADC1P/N, ADC2P/N, ADC3P/N) <sup>1</sup>                                                                                                                                                                                                     | 22 dBm                       |
| VCM0, VCM1                                                                                                                                                                                                                                                                       | −0.3 V to RVDD2 + 0.3 V      |
| CLKINP, CLKINN                                                                                                                                                                                                                                                                   | −0.2 V to PLLCLKVDD1 + 0.2 V |
| ADCD <sub>RVN</sub> , ADCD <sub>RVP</sub>                                                                                                                                                                                                                                        | −0.2 V to CLKVDD1 + 0.2 V    |
| SERDIN <sub>x±</sub> , SERDOUT <sub>x±</sub>                                                                                                                                                                                                                                     | −0.2 V to SVDD1 + 0.2 V      |
| SYSREFP, SYSREFN, and SYNCxINB <sub>±</sub>                                                                                                                                                                                                                                      | −0.2 V to +2.5 V             |
| SYNCxOUTB <sub>±</sub> , SYNCxINB <sub>±</sub> , RESETB, TXEN <sub>x</sub> , RXEN <sub>x</sub> , IRQB <sub>x</sub> , CSB, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, ADC <sub>x</sub> _SMON0, ADC <sub>x</sub> _SMON1, ADC <sub>x</sub> _FD0, ADC <sub>x</sub> _FD1, GPIO <sub>x</sub> | −0.3 V to DVDD1P8 + 0.3 V    |
| AVDD2, AVDD2_PLL, BVDD2, RVDD2, SVDD2_PLL, DVDD1P8                                                                                                                                                                                                                               | −0.3 V to +2.2 V             |
| PLLCLKVDD1, AVDD1, AVDD1_ADC, CLKVDD1, FVDD1, DAVDD1, DVDD1_RT, DCLKVDD1, SVDD1, SVDD1_PLL                                                                                                                                                                                       | −0.2 V to +1.2 V             |
| VNN1                                                                                                                                                                                                                                                                             | −1.1 V to +0.2 V             |
| Temperature Ranges                                                                                                                                                                                                                                                               |                              |
| Maximum Junction (T <sub>J</sub> ) <sup>2</sup>                                                                                                                                                                                                                                  | 120°C                        |
| Storage                                                                                                                                                                                                                                                                          | −65°C to +150°C              |

<sup>1</sup> Tested continuously for 1000 hours with  $f_{IN} = 4.7$  GHz pulsed and continuous tone at maximum allowed junction temperature (T<sub>J</sub>). Refer to [UG-1578](#), the device user guide, for more information.

<sup>2</sup> Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T<sub>J</sub> does not exceed the limits shown in [Table 19](#).

θ<sub>JA</sub> is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ<sub>JC\_TOP</sub> is the junction to case, thermal resistance.

θ<sub>JB</sub> is the junction to board, thermal resistance.

Table 20. Simulated Thermal Resistance<sup>1</sup>

| PCB Type         | Airflow Velocity (m/sec) | θ <sub>JA</sub> | θ <sub>JC_TOP</sub> | θ <sub>JB</sub> | Unit |
|------------------|--------------------------|-----------------|---------------------|-----------------|------|
| JEDEC 2s2p Board | 0.0                      | 14.9            | 0.70                | 1.8             | °C/W |

<sup>1</sup> Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

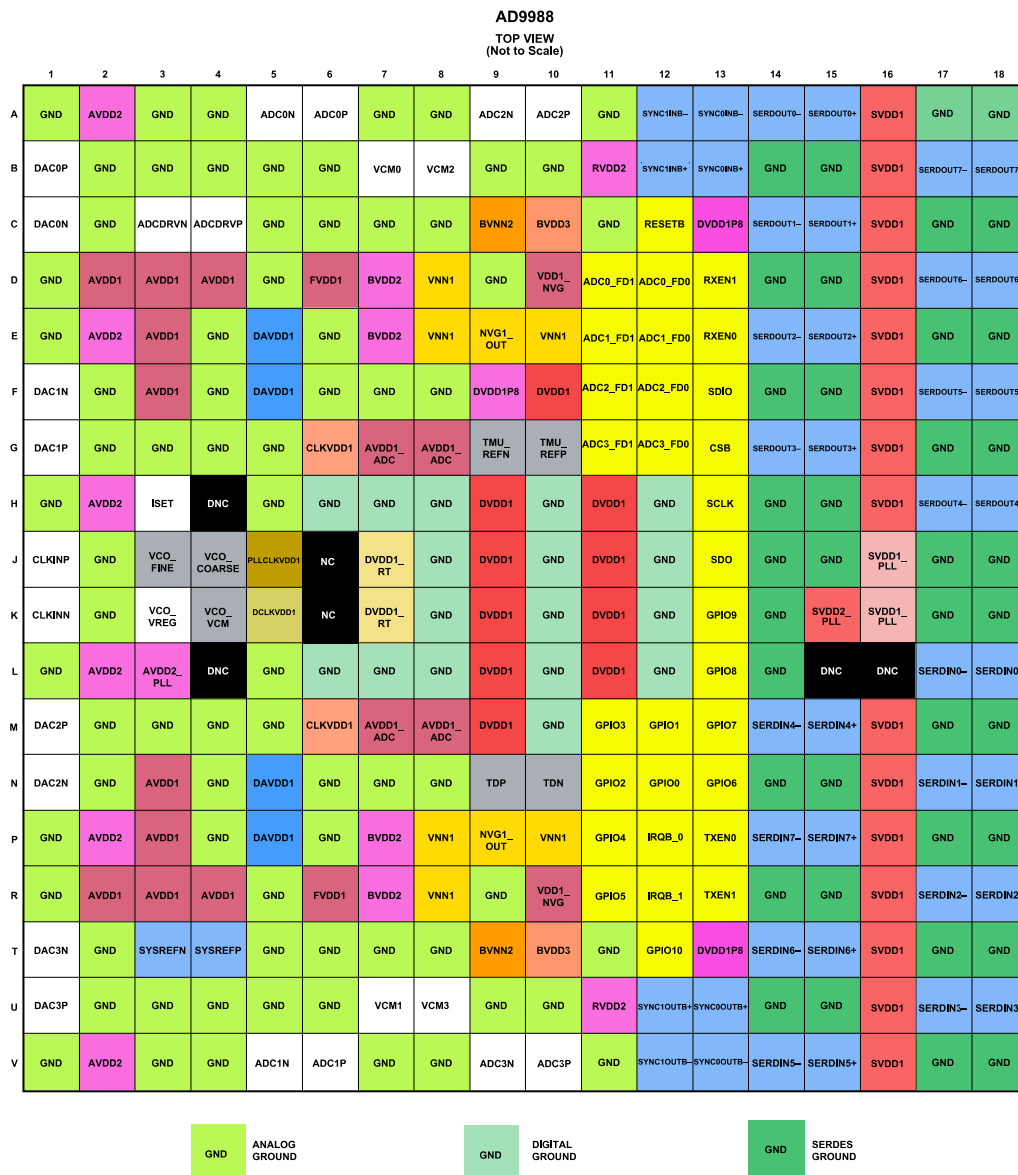


Figure 5. Pin Configuration

Table 21. Pin Function Descriptions

| Pin No.                                | Mnemonic   | Type  | Description                                                          |
|----------------------------------------|------------|-------|----------------------------------------------------------------------|
| <b>Power Supplies</b>                  |            |       |                                                                      |
| A2, E2, H2, L2, P2, V2                 | AVDD2      | Input | Analog 2.0 V Supply Inputs for DAC.                                  |
| L3                                     | AVDD2_PLL  | Input | Analog 2.0 V Supply Input for Clock PLL Low Dropout (LDO) Regulator. |
| D7, E7, P7, R7                         | BVDD2      | Input | Analog 2.0 V Supply Inputs for ADC Buffer.                           |
| B11, U11                               | RVDD2      | Input | Analog 2.0 V Supply Inputs for ADC Reference.                        |
| J5                                     | PLLCLKVDD1 | Input | Analog 1.0 V Supply Input for Clock PLL.                             |
| D2, D3, D4, E3, F3, N3, P3, R2, R3, R4 | AVDD1      | Input | Analog 1.0 V Supply Inputs for DAC Clock.                            |
| G7, G8, M7, M8                         | AVDD1_ADC  | Input | Analog 1.0 V Supply Inputs for ADC.                                  |
| G6, M6                                 | CLKVDD1    | Input | Analog 1.0 V Supply Inputs for ADC Clock.                            |
| D6, R6                                 | FVDD1      | Input | Analog 1.0 V Supply Inputs for ADC Reference.                        |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 21. Pin Function Descriptions

| Pin No.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Mnemonic               | Type         | Description                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D10, R10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | VDD1_NVG               | Input        | Analog 1.0 V Supply Inputs for Negative Voltage Generator (NVG) Used to Generate -1 V Output.                                                                                                         |
| E9, P9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NVG1_OUT               | Output       | Analog -1 V Supply Outputs from NVG. Decouple NVG1_OUT to GND with a 0.1 $\mu$ F capacitor.                                                                                                           |
| D8, E8, E10, P8, R8, P10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | VNN1                   | Input        | Analog -1 V Supply Inputs for ADC Buffer and Reference. Connect these pins to the adjacent NVG1_OUT pins.                                                                                             |
| C9, T9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | BVNN2                  | Output       | Decoupling Pin for the Internally Generated Analog -2 V ADC Buffer Supply. Decouple each BVNN2 pin to GND with a 0.1 $\mu$ F capacitor.                                                               |
| C10, T10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | BVDD3                  | Output       | Decoupling Pin for the Internally Generated Analog 3 V ADC Buffer Supply. Decouple BVDD3 to GND with a 0.1 $\mu$ F capacitor.                                                                         |
| E5, F5, N5, P5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | DAVDD1                 | Input        | Digital Analog 1.0 V Supply Inputs.                                                                                                                                                                   |
| F10, H9, H11, J9, J11, K9, K11, L9, L11, M9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | DVDD1                  | Input        | Digital 1.0 V Supply Inputs.                                                                                                                                                                          |
| J7, K7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DVDD1_RT               | Input        | Digital 1.0 V Supply Inputs for Retimer Block.                                                                                                                                                        |
| K5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | DCLKVDD1               | Input        | Digital 1.0 V Clock Generation Supply.                                                                                                                                                                |
| A16, B16, C16, D16, E16, F16, G16, H16, M16, N16, P16, R16, T16, U16, V16                                                                                                                                                                                                                                                                                                                                                                                                                                                   | SVDD1                  | Input        | Digital 1.0 V Supply Inputs for SERDES Deserializer and Serializer.                                                                                                                                   |
| K15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | SVDD2_PLL              | Input        | Digital 2.0 V Supply Input for SERDES LDO Regulator.                                                                                                                                                  |
| J16, K16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | SVDD1_PLL              | Input        | Digital 1.0 V Supply Inputs for SERDES Clock Generation and PLL.                                                                                                                                      |
| C13, F9, T13                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | DVDD1P8                | Input        | Digital Interface and Temperature Monitoring Unit (TMU) Supply Inputs (Nominal 1.8 V).                                                                                                                |
| A1, A3, A4, A7, A8, A11, A17, A18, B2 to B6, B9, B10, B14, B15, C2, C5 to C8, C11, C17, C18, D1, D5, D9, D14, D15, E1, E4, E6, E17, E18, F2, F4, F6 to F8, F14, F15, G2 to G5, G17, G18, H1, H5 to H8, H10, H12, H14, H15, J2, J8, J10, J12, J14, J15, J17, J18, K2, K8, K10, K12, K14, K17, K18, L1, L5 to L8, L10, L12, L14, M2 to M5, M10, M17, M18, N2, N4, N6 to N8, N14, N15, P1, P4, P6, P17, P18, R1, R5, R9, R14, R15, T2, T5 to T8, T11, T17, T18, U2 to U6, U9, U10, U14, U15, V1, V3, V4, V7, V8, V11, V17, V18 | GND                    | Input/output | Ground References.                                                                                                                                                                                    |
| <b>Analog Outputs</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                        |              |                                                                                                                                                                                                       |
| B1, C1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DAC0P, DAC0N           | Output       | DAC0 Output Currents, Ground Referenced. Tie these pins to GND if unused.                                                                                                                             |
| G1, F1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DAC1P, DAC1N           | Output       | DAC1 Output Currents, Ground Referenced. Tie these pins to GND if unused.                                                                                                                             |
| M1, N1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DAC2P, DAC2N           | Output       | DAC2 Output Currents, Ground Referenced. Tie these pins to GND if unused.                                                                                                                             |
| U1, T1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | DAC3P, DAC3N           | Output       | DAC3 Output Currents, Ground Referenced. Tie these pins to GND if unused.                                                                                                                             |
| H3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | ISSET                  | Output       | DAC Bias Current Setting Pin. Connect this pin with a 5 k $\Omega$ resistor to GND.                                                                                                                   |
| C4, C3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | ADCDRVP, ADCDRVN       | Output       | Optional Clock Output. These pins are disabled by default but can be used as a clock source for an external ADC or another device that requires a reference clock. Leave the pins floating if unused. |
| B7, U7, B8, U8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VCM0, VCM1, VCM2, VCM3 | Output       | ADC Buffer Common-Mode Output Voltage. Decouple these pins to GND with a 0.1 $\mu$ F capacitor.                                                                                                       |
| K3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | VCO_VREG               | Output       | PLL LDO Regulator Output. Decouple this pin to GND with a 2.2 $\mu$ F capacitor.                                                                                                                      |
| G9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | TMU_REFN               | Output       | TMU ADC Negative Reference. Connect this pin to GND.                                                                                                                                                  |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 21. Pin Function Descriptions

| Pin No.                                    | Mnemonic           | Type         | Description                                                                                                                                                                                                                                                                                    |
|--------------------------------------------|--------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| G10                                        | TMU_REFP           | Output       | TMU ADC Positive Reference. Connect this pin to DVDD1P8.                                                                                                                                                                                                                                       |
| <b>Analog Inputs</b>                       |                    |              |                                                                                                                                                                                                                                                                                                |
| A6, A5                                     | ADC0P, ADC0N       | Input        | ADC0 Differential Inputs with Internal 100 $\Omega$ Differential Resistor. Leave these pins floating if unused.                                                                                                                                                                                |
| V6, V5                                     | ADC1P, ADC1N       | Input        | ADC1 Differential Inputs with Internal 100 $\Omega$ Differential Resistor. Leave these pins floating if unused.                                                                                                                                                                                |
| A10, A9                                    | ADC2P, ADC2N       | Input        | ADC2 Differential Inputs with Internal 100 $\Omega$ Differential Resistor. Leave these pins floating if unused.                                                                                                                                                                                |
| V10, V9                                    | ADC3P, ADC3N       | Input        | ADC3 Differential Inputs with Internal 100 $\Omega$ Differential Resistor. Leave these pins floating if unused.                                                                                                                                                                                |
| J3                                         | VCO_FINE           | Input        | On-Chip Device Clock Multiplier and PLL Fine Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.                                                                                                                               |
| J4                                         | VCO_COARSE         | Input        | On-Chip Device Clock Multiplier and PLL Coarse Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.                                                                                                                             |
| K4                                         | VCO_VCM            | Input        | On-Chip Device Clock Multiplier and VCO Common-Mode Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.                                                                                                                                    |
| N9, N10                                    | TDP, TDN           | Input        | Anode and Cathode of Temperature Diodes. This feature is not supported. Tie TDP and TDN to GND.                                                                                                                                                                                                |
| J1, K1                                     | CLKINP, CLKINN     | Input        | Differential Clock Inputs with Nominal 100 $\Omega$ Termination. These self biased inputs require ac coupling. When the on-chip clock multiplier PLL is enabled, this input is the reference clock input. If the PLL is disabled, an RF clock equal to the DAC output sample rate is required. |
| <b>CMOS Inputs and Outputs<sup>1</sup></b> |                    |              |                                                                                                                                                                                                                                                                                                |
| G13                                        | CSB                | Input        | Serial Port Enable Input. Active low.                                                                                                                                                                                                                                                          |
| H13                                        | SCLK               | Input        | Serial Plot Clock Input.                                                                                                                                                                                                                                                                       |
| F13                                        | SDIO               | Input/output | Serial Port Bidirectional Data Input/Output.                                                                                                                                                                                                                                                   |
| J13                                        | SDO                | Output       | Serial Port Data Output.                                                                                                                                                                                                                                                                       |
| C12                                        | RESETB             | Input        | Active Low Reset Input. RESETB places digital logic and SPI registers in a known default state. RESETB must be connected to a digital IC that is capable of issuing a reset signal for the first step in the device initialization process.                                                    |
| E13, D13                                   | RXEN0, RXEN1       | Input        | Active High ADC and Receive Datapath Enable Inputs. RXENx is also SPI configurable.                                                                                                                                                                                                            |
| P13, R13                                   | TXEN0, TXEN1       | Input        | Active High DAC and Transmit Datapath Enable Inputs. TXENx is also SPI configurable.                                                                                                                                                                                                           |
| D12, D11                                   | ADC0_FD0, ADC0_FD1 | Output       | ADC0 Fast Detect Outputs by Default. Do not connect if unused.                                                                                                                                                                                                                                 |
| E12, E11                                   | ADC1_FD0, ADC1_FD1 | Output       | ADC1 Fast Detect Outputs by Default. Do not connect if unused.                                                                                                                                                                                                                                 |
| F12, F11                                   | ADC2_FD0, ADC2_FD1 | Output       | ADC2 Fast Detect Outputs by Default. Do not connect if unused.                                                                                                                                                                                                                                 |
| G12, G11                                   | ADC3_FD0, ADC3_FD1 | Output       | ADC3 Fast Detect Outputs by Default. Do not connect if unused.                                                                                                                                                                                                                                 |
| P12, R12                                   | IRQB_0, IRQB_1     | Output       | Interrupt Request Outputs. These pins are open-drain, active low outputs (CMOS levels with respect to DVDD1P8). Connect a >5 k $\Omega$ pull-up resistor to DVDD1P8 to prevent these pins from floating when unused.                                                                           |
| N12, M12, N11, M11, P11, R11               | GPIO0 to GPIO5     | Input/output | General-Purpose Input or Output Pins. These pins control auxiliary functions related to the Tx datapaths.                                                                                                                                                                                      |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 21. Pin Function Descriptions

| Pin No.                                                                             | Mnemonic               | Type         | Description                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------------|------------------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| N13, M13, L13, K13, T12                                                             | GPIO6 to GPIO10        | Input/output | General-Purpose Input or Output Pins. These pins control auxiliary functions related to the Rx datapaths and ADCs.                                                                                                                                                                                |
| JESD204B- or JESD204C-Compatible SERDES Data Lanes and Control Signals <sup>2</sup> |                        |              |                                                                                                                                                                                                                                                                                                   |
| L18, L17                                                                            | SERDIN0+, SERDIN0-     | Input        | JRx Lane 0 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| N18, N17                                                                            | SERDIN1+, SERDIN1-     | Input        | JRx Lane 1 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| R18, R17                                                                            | SERDIN2+, SERDIN2-     | Input        | JRx Lane 2 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| U18, U17                                                                            | SERDIN3+, SERDIN3-     | Input        | JRx Lane 3 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| M15, M14                                                                            | SERDIN4+, SERDIN4-     | Input        | JRx Lane 4 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| V15, V14                                                                            | SERDIN5+, SERDIN5-     | Input        | JRx Lane 5 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| T15, T14                                                                            | SERDIN6+, SERDIN6-     | Input        | JRx Lane 6 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| P15, P14                                                                            | SERDIN7+, SERDIN7-     | Input        | JRx Lane 7 Inputs, Data True/Complement.                                                                                                                                                                                                                                                          |
| U13, V13                                                                            | SYNC0OUTB+, SYNC0OUTB- | Output       | JRx Link 0 Synchronization Outputs for JESD204B interface. These pins are LVDS or CMOS configurable. These pins can also provide differential 100 $\Omega$ output impedance in LVDS mode.                                                                                                         |
| U12, V12                                                                            | SYNC1OUTB+, SYNC1OUTB- | Output       | JRx Link 1 Synchronization Outputs for JESD204B Interface or CMOS Input to Control the Transmit Fast Frequency Hopping (FFH) Feature. For JRx link synchronization, these pins can be configured as LVDS or CMOS outputs and can provide differential 100 $\Omega$ output impedance in LVDS mode. |
| A15, A14                                                                            | SERDOUT0+, SERDOUT0-   | Output       | JTx Lane 0 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| C15, C14                                                                            | SERDOUT1+, SERDOUT1-   | Output       | JTx Lane 1 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| E15, E14                                                                            | SERDOUT2+, SERDOUT2-   | Output       | JTx Lane 2 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| G15, G14                                                                            | SERDOUT3+, SERDOUT3-   | Output       | JTx Lane 3 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| H18, H17                                                                            | SERDOUT4+, SERDOUT4-   | Output       | JTx Lane 4 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| F18, F17                                                                            | SERDOUT5+, SERDOUT5-   | Output       | JTx Lane 5 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| D18, D17                                                                            | SERDOUT6+, SERDOUT6-   | Output       | JTx Lane 6 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| B18, B17                                                                            | SERDOUT7+, SERDOUT7-   | Output       | JTx Lane 7 Outputs, Data True/Complement.                                                                                                                                                                                                                                                         |
| B13, A13                                                                            | SYNC0INB+, SYNC0INB-   | Input        | JTx Link 0 Synchronization Inputs for JESD204B interface. These pins are LVDS or CMOS configurable and have selectable internal 100 $\Omega$ input impedance for LVDS operation.                                                                                                                  |
| B12, A12                                                                            | SYNC1INB+, SYNC1INB-   | Input        | JTx Link 1 Synchronization Inputs for JESD204B interface or CMOS Inputs for Receive FFH via GPIOx pins. These pins are LVDS or CMOS configurable and have selectable internal 100 $\Omega$ input impedance for LVDS operation.                                                                    |
| T4, T3                                                                              | SYSREFP, SYSREFN       | Input        | Active High JESD204B/C System Reference Inputs. These pins are configurable for differential current mode logic (CML), PECL, and LVDS with internal 100 $\Omega$ termination or single-ended CMOS.                                                                                                |



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**Table 21. Pin Function Descriptions**

| Pin No.                         | Mnemonic | Type | Description                                           |
|---------------------------------|----------|------|-------------------------------------------------------|
| No Connects and Do Not Connects |          |      |                                                       |
| J6, K6                          | NC       | NC   | No Connect. These pins can be left open or connected. |
| H4, L4, L15, L16                | DNC      | DNC  | Do Not Connect. The pins must be kept open.           |

<sup>1</sup> CMOS inputs do not have pull-up or pull-down resistors.

<sup>2</sup> SERDINx± and SERDOUTx± include 100  $\Omega$  internal termination resistors.

## TYPICAL PERFORMANCE CHARACTERISTICS

## DAC

The data curves represent the average performance across all outputs with harmonics and spurs falling in the first Nyquist zone ( $< f_{\text{DAC}}/2$ ). All SFDR, IMD3, and NSD data measured on a laboratory evaluation board. All data for phase noise and ACLR is measured on the AD9081-FMCA-EBZ or the AD9082-FMCA-EBZ customer evaluation board. For additional information on the JESD204B and JESD204C mode configurations see the [UG-1578](#) user guide.

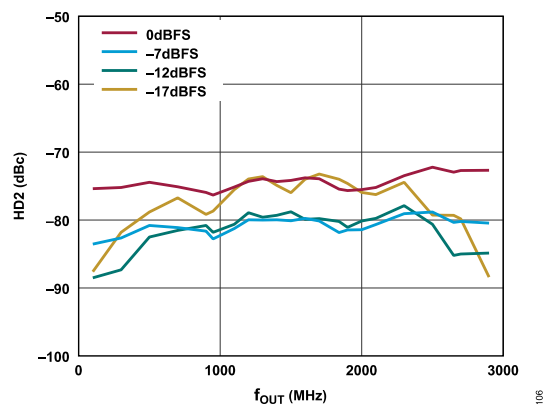


Figure 6. HD2 vs.  $f_{\text{OUT}}$  over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 4x, Mode 15C

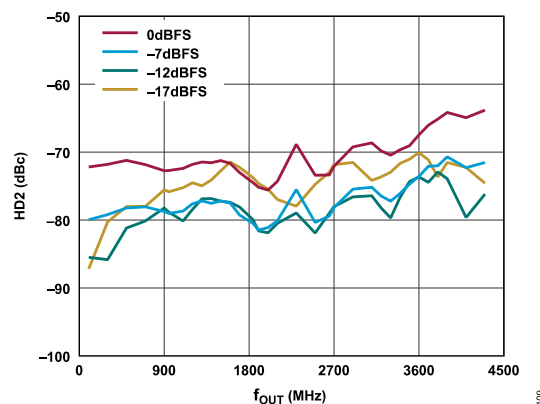


Figure 9. HD2 vs.  $f_{\text{OUT}}$  over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 6x, Mode 15C

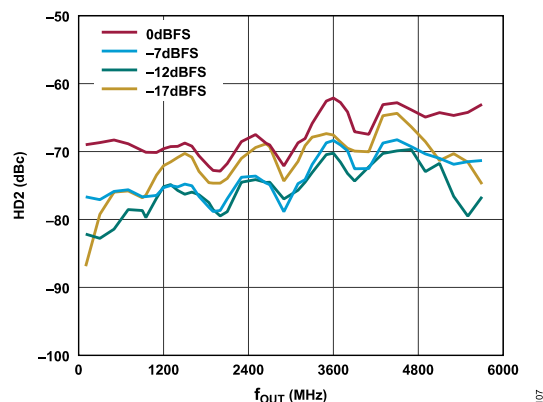


Figure 7. HD2 vs.  $f_{\text{OUT}}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 8x, Mode 15C

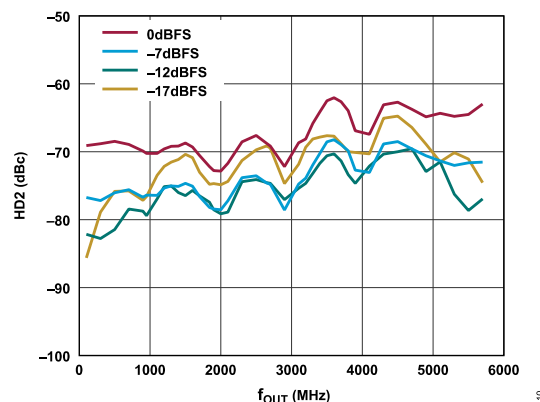


Figure 10. HD2 vs.  $f_{\text{OUT}}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x, Mode 16B

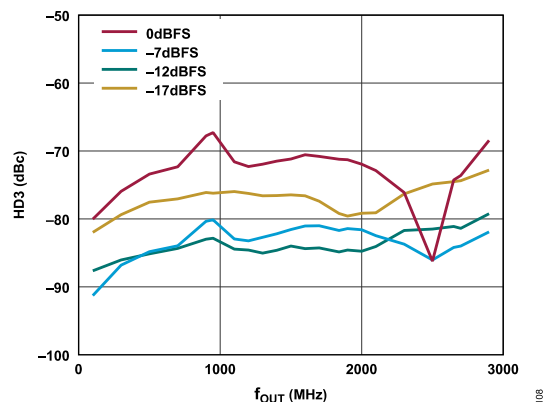


Figure 8. HD3 vs.  $f_{\text{OUT}}$  over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 4x, Mode 15C

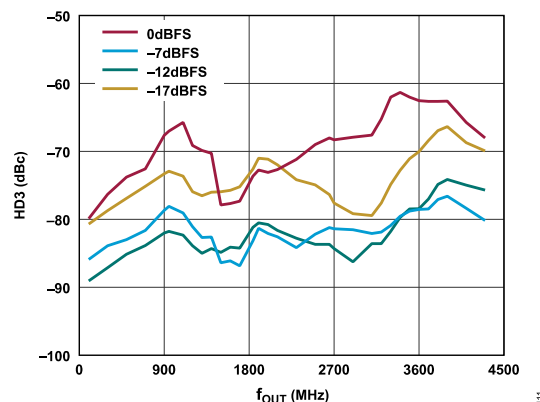


Figure 11. HD3 vs.  $f_{\text{OUT}}$  over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 6x, Mode 15C

## TYPICAL PERFORMANCE CHARACTERISTICS

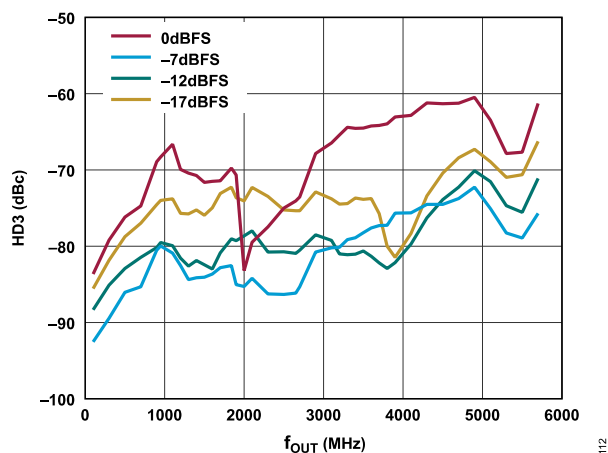


Figure 12. HD3 vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 8x, Mode 15C

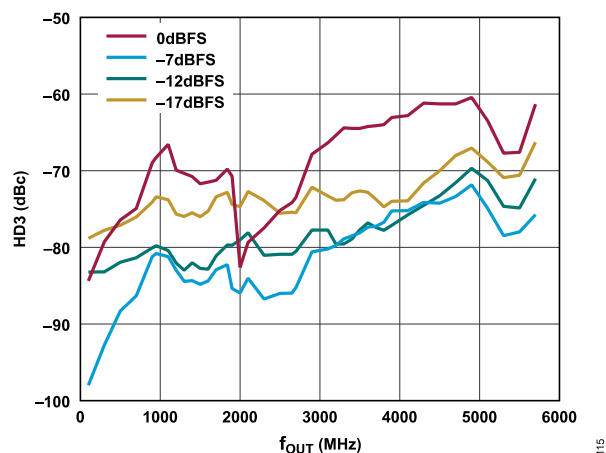


Figure 15. HD3 vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x, Mode 16B

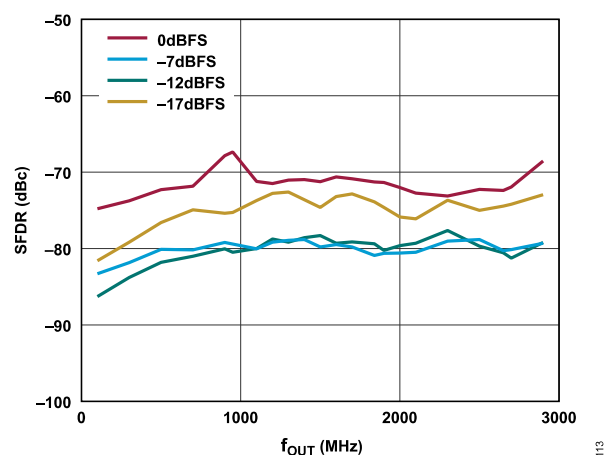


Figure 13. SFDR, Worst Spurious vs.  $f_{OUT}$  over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 4x, Mode 15C

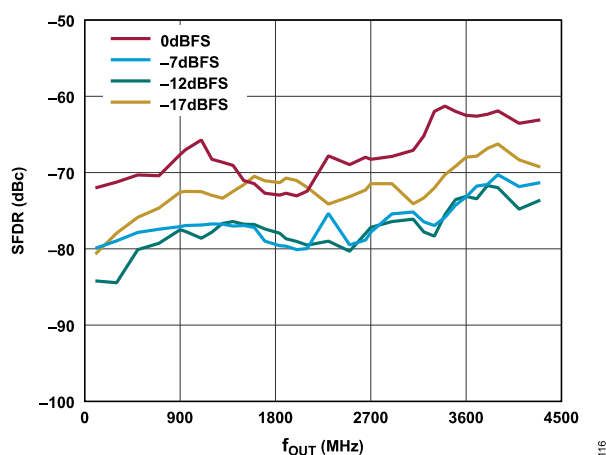


Figure 16. SFDR, Worst Spurious vs.  $f_{OUT}$  over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 6x, Mode 15C

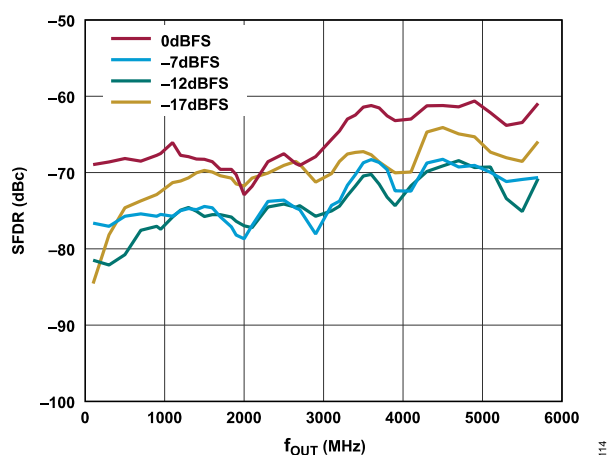


Figure 14. SFDR, Worst Spurious vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1x, Main Interpolation 8x, Mode 15C

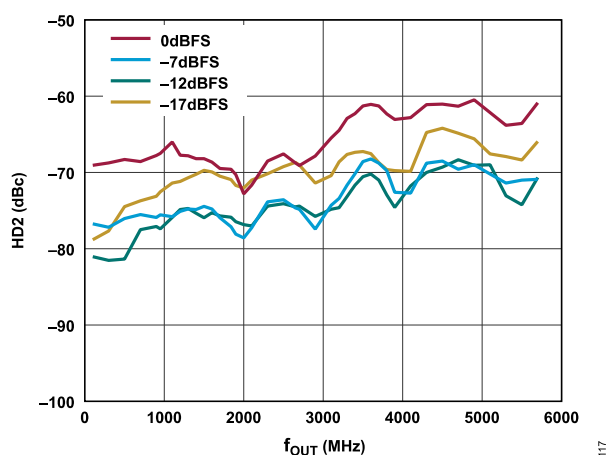


Figure 17. SFDR, Worst Spurious vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4x, Main Interpolation 8x, Mode 16B

## TYPICAL PERFORMANCE CHARACTERISTICS

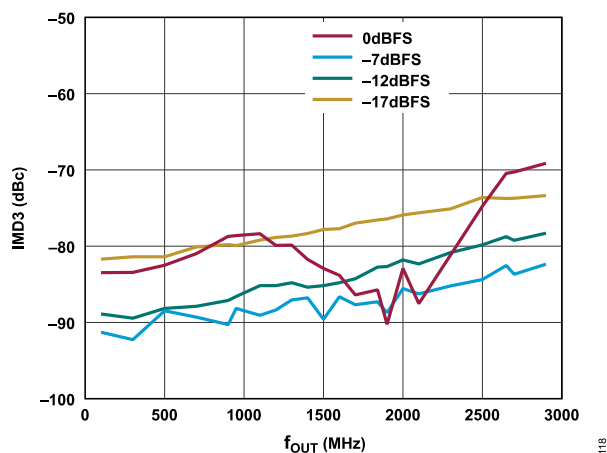


Figure 18. IMD3 vs.  $f_{OUT}$  over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1 $\times$ , Main Interpolation 4 $\times$ , Mode 15C; IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

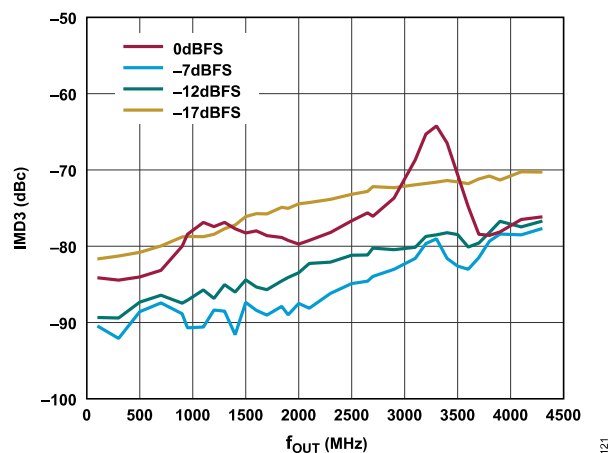


Figure 21. IMD3 vs.  $f_{OUT}$  over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1 $\times$ , Main Interpolation 6 $\times$ , Mode 15C; IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

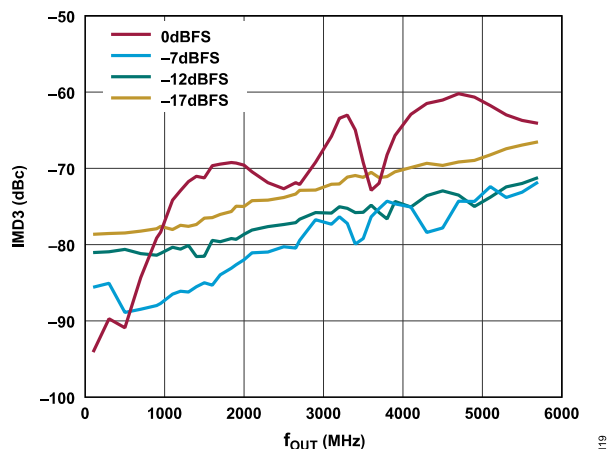


Figure 19. IMD3 vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1 $\times$ , Main Interpolation 8 $\times$ , Mode 15C; IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

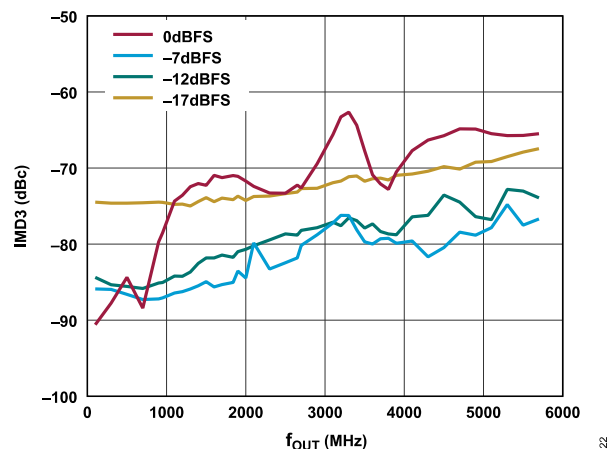


Figure 22. IMD3 vs.  $f_{OUT}$  over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4 $\times$ , Main Interpolation 8 $\times$ , Mode 16B; IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

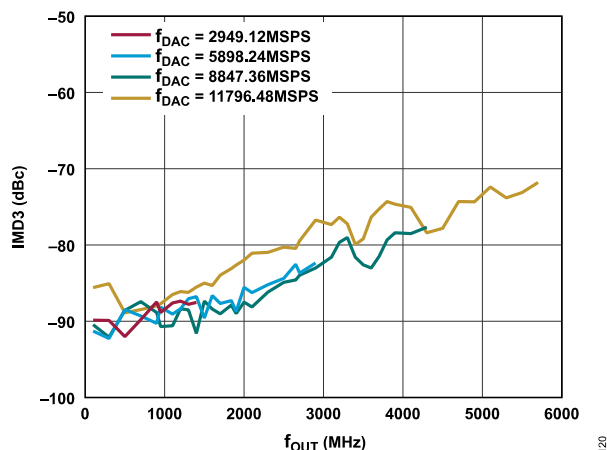


Figure 20. IMD3 vs.  $f_{OUT}$  over  $f_{DAC}$ , Digital Scale -7 dBFS; IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

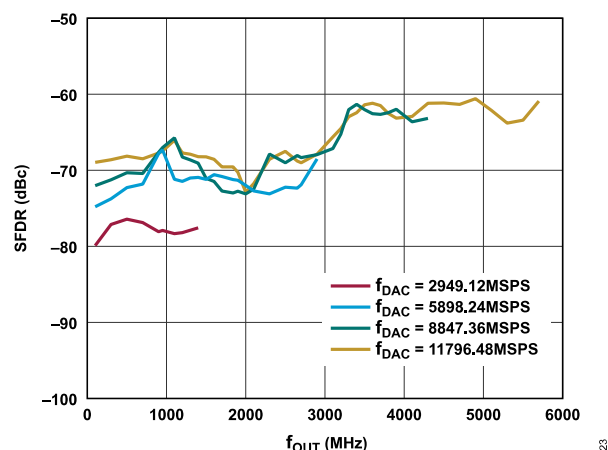


Figure 23. SFDR, Worst In-Band Spurious vs.  $f_{OUT}$  over  $f_{DAC}$ , with 0 dBFS Tone Level

## TYPICAL PERFORMANCE CHARACTERISTICS

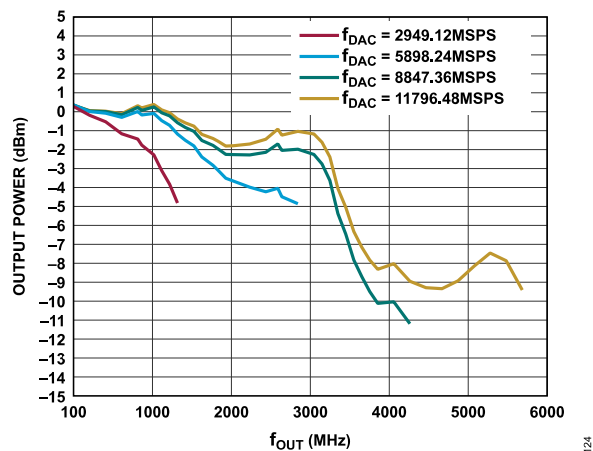


Figure 24. DAC0 Fundamental Output Power vs.  $f_{OUT}$  Across  $f_{DAC}$ , at 0 dBFS Digital Back Off, Measured on a Laboratory Evaluation Board; the AD9081-FMCA-EBZ or AD9082-FMCA-EBZ Evaluation Board has a Different PCB Layout and Results in a Different Frequency Response when Compared to a Laboratory Evaluation Board

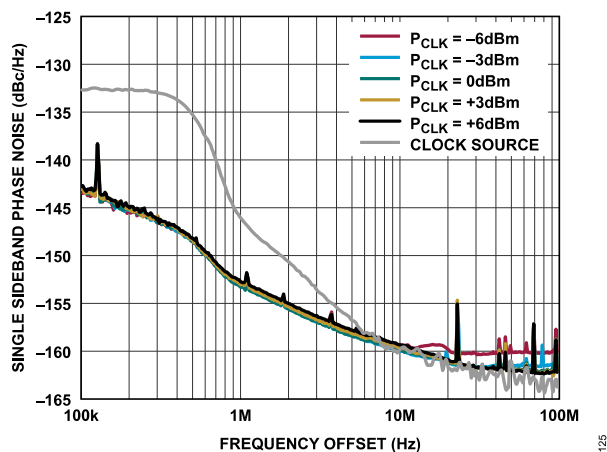


Figure 25. Single Sideband Phase Noise vs. Frequency Offset for Different Clock Input Power ( $P_{CLK}$ ),  $f_{OUT} = 1.8$  GHz, External 12 GHz Clock Input with Clock PLL Disabled

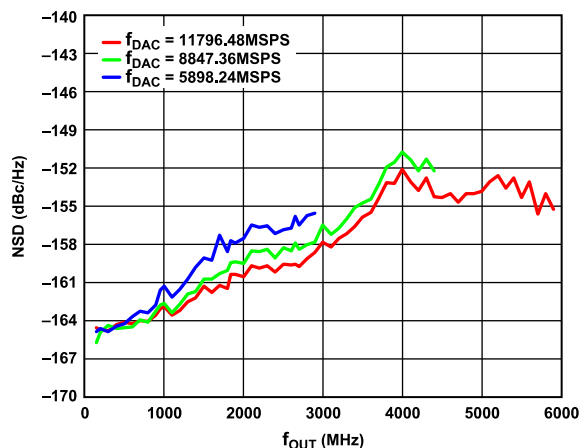


Figure 26. Single-Tone NSD Measured at 10% Offset from  $f_{OUT}$  vs.  $f_{OUT}$  over  $f_{DAC}$ , Shuffle On, 16-Bit Resolution, Mode 15C

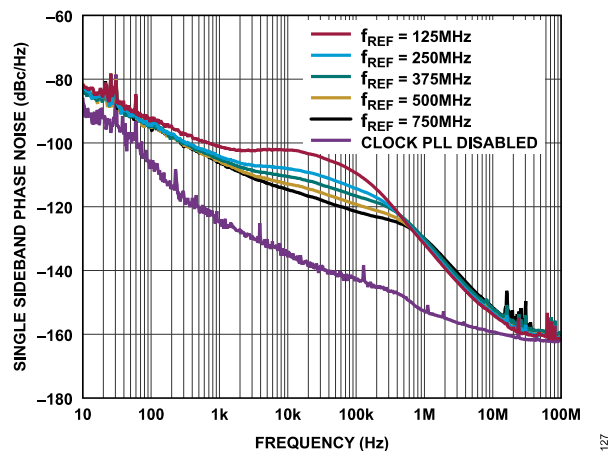


Figure 27. Single Sideband Phase Noise vs. Frequency Offset for Different PLL Reference Clocks ( $f_{REF}$ ),  $f_{OUT} = 1.8$  GHz,  $f_{DAC} = 12$  GSPS, PLL Enabled with Exception of External 12 GHz Clock Input with Clock PLL Disabled

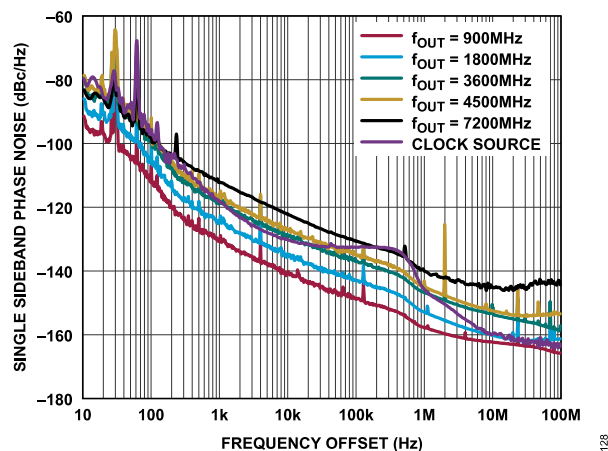


Figure 28. Single Sideband Phase Noise vs. Frequency Offset for Different DAC Output Frequencies ( $f_{OUT}$ ), External 12 GHz Clock Input with Clock PLL Disabled

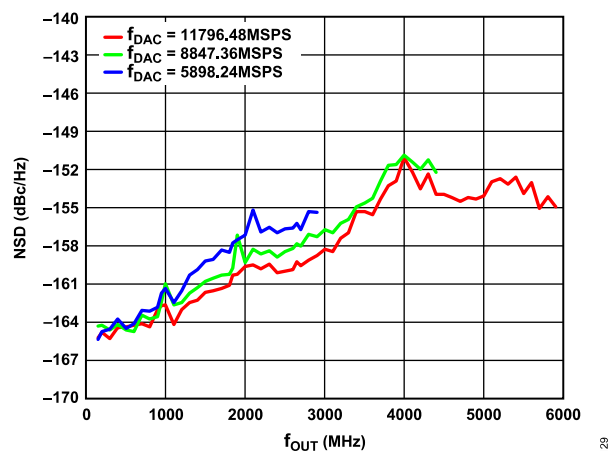


Figure 29. Single-Tone NSD Measured at 10% Offset from  $f_{OUT}$  vs.  $f_{OUT}$  over  $f_{DAC}$ , 12-Bit Resolution, Shuffle On, Mode 24C

## TYPICAL PERFORMANCE CHARACTERISTICS

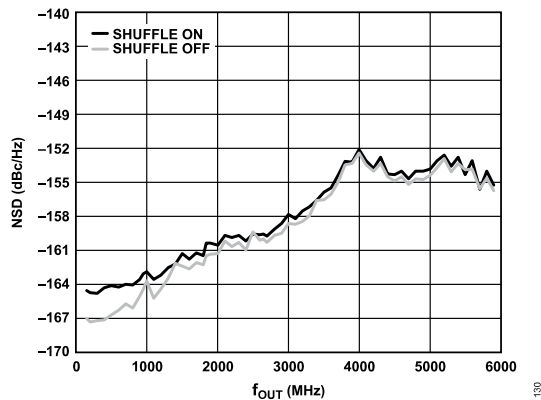


Figure 30. Single-Tone NSD Measured at 10% Offset from  $f_{OUT}$  vs.  $f_{OUT}$ , Shuffle Off vs. Shuffle On,  $f_{DAC} = 11796.48$  MSPS, 16-Bit Resolution, Mode 15C

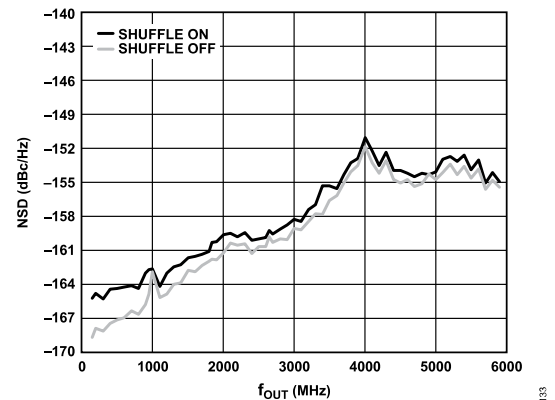


Figure 33. Single-Tone NSD Measured at 10% Offset from  $f_{OUT}$  vs.  $f_{OUT}$ , Shuffle Off vs. Shuffle On,  $f_{DAC} = 11796.48$  MSPS, 12-Bit Resolution, Mode 24C

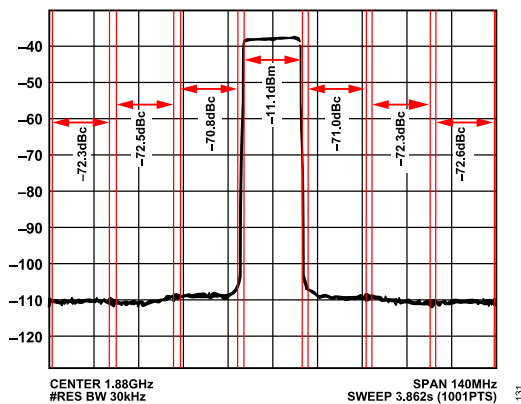


Figure 31. Dual Band ACLR Performance for Two 20 MHz LTE carriers at  $f_{OUT} = 1.88$  GHz and  $f_{OUT} = 2.145$  GHz refer to figure 32 for a wideband plot); Showing a Close Up of One Carrier at  $f_{OUT} = 1.88$  GHz,  $f_{DAC} = 11.796$  GSPS, Test Vector PAR = 7.7 dB with -1 dBFS Back Off, Channel Interpolation 3 $\times$ , Main Interpolation 8 $\times$ , Mode 9C

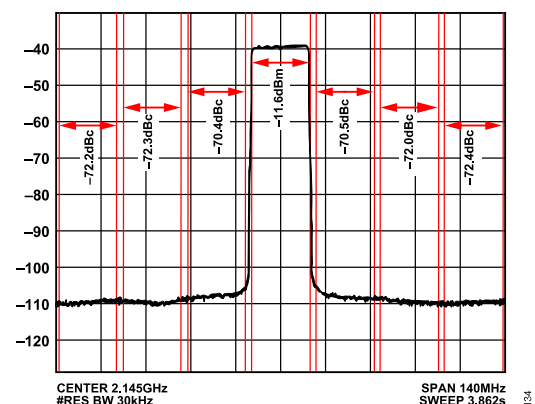


Figure 34. Dual Band ACLR Performance for two 20 MHz LTE carriers at  $f_{OUT} = 1.88$  GHz and  $f_{OUT} = 2.145$  GHz (Refer to Figure 32 for a Wideband Plot); Showing a Close-up of One Carrier at  $f_{OUT} = 2.145$  GHz,  $f_{DAC} = 11.796$  GSPS, Test Vector PAR = 7.7 dB with -1 dBFS Back Off, Channel Interpolation 3 $\times$ , Main Interpolation 8 $\times$ , Mode 9C

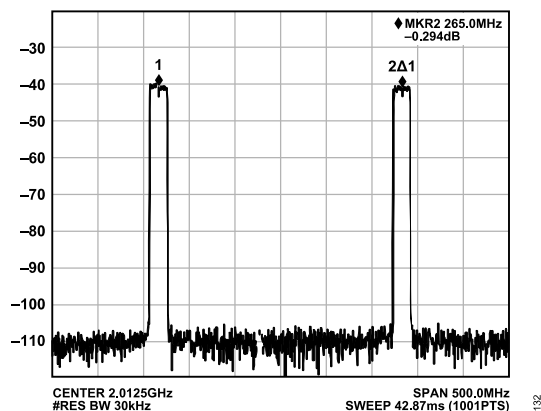


Figure 32. Dual Band Wideband Plot for Two 20 MHz LTE Carriers at  $f_{OUT} = 1.88$  GHz and  $f_{OUT} = 2.145$  GHz (3GPP Bands, B1 and B3, Respectively), at  $f_{DAC} = 11.796$  GSPS, Test Vector PAR = 7.7 dB with -1 dBFS Back Off, Channel Interpolation 3 $\times$ , Main Interpolation 8 $\times$ , Mode 9C

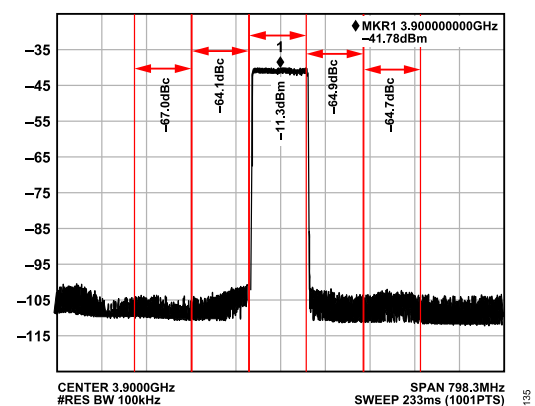
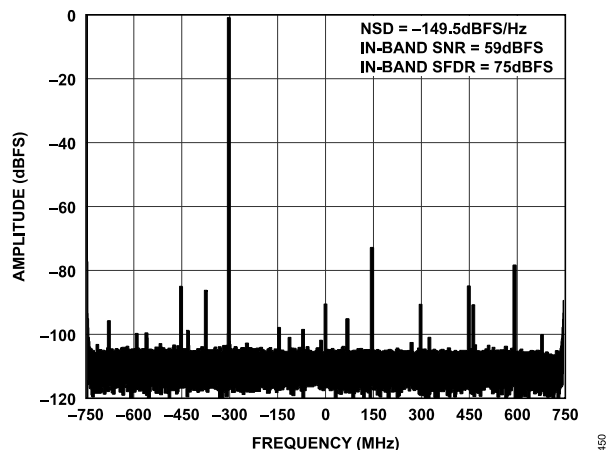
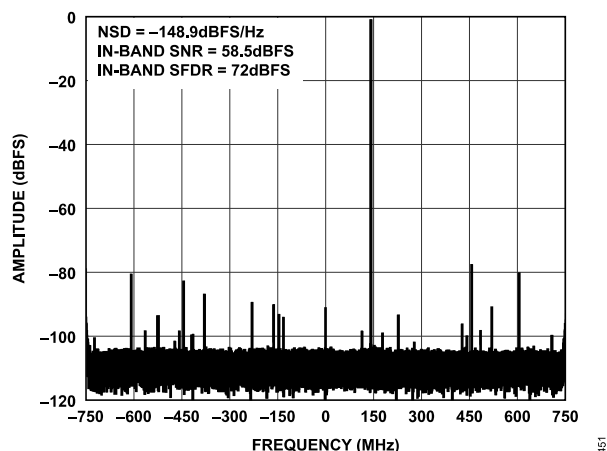
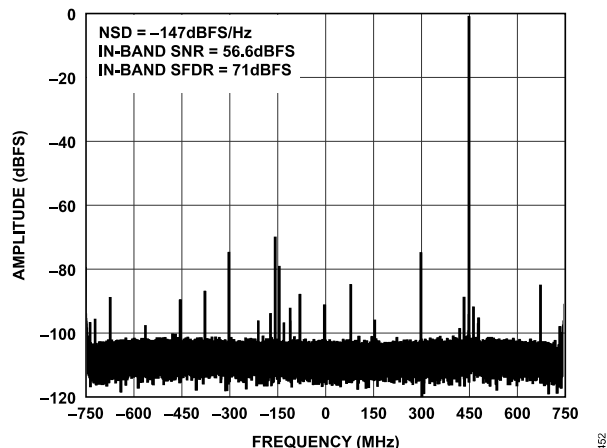
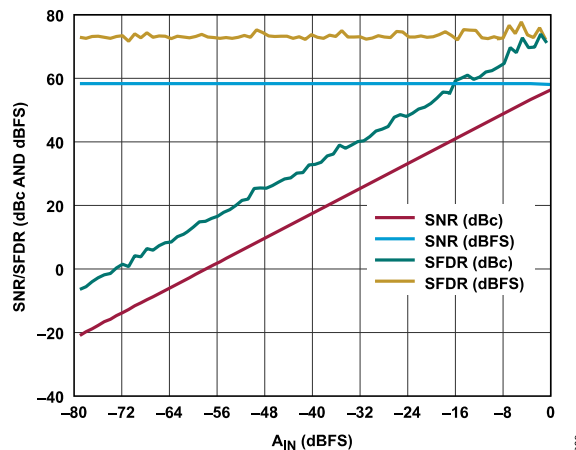
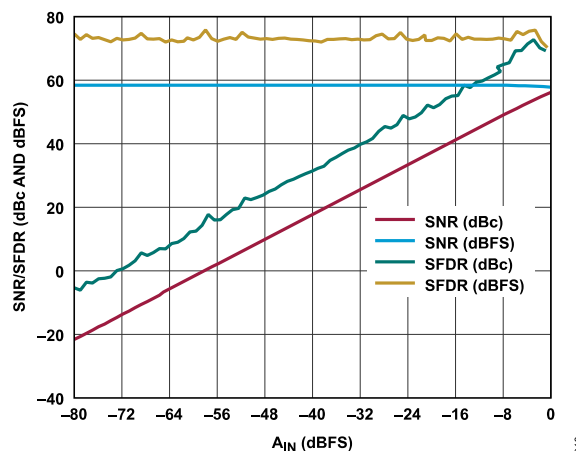
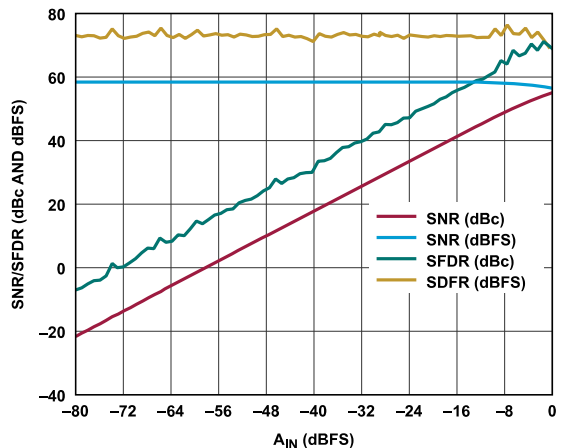


Figure 35. Adjacent Channel Leakage Ratio (ACLR) Performance for 100 MHz 5G Test Vector at  $f_{OUT} = 3.9$  GHz and  $f_{DAC} = 11.898$  GSPS, Test Vector Peak to RMS = 11.7 dB with -1 dBFS Back Off (Mode 9C), Channel Interpolation 3 $\times$ , Main Interpolation 8 $\times$

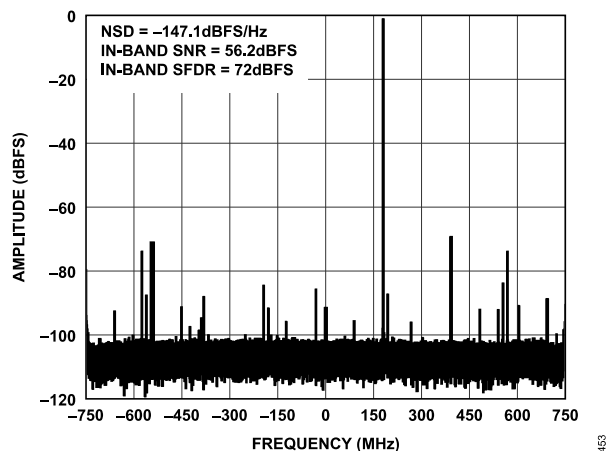
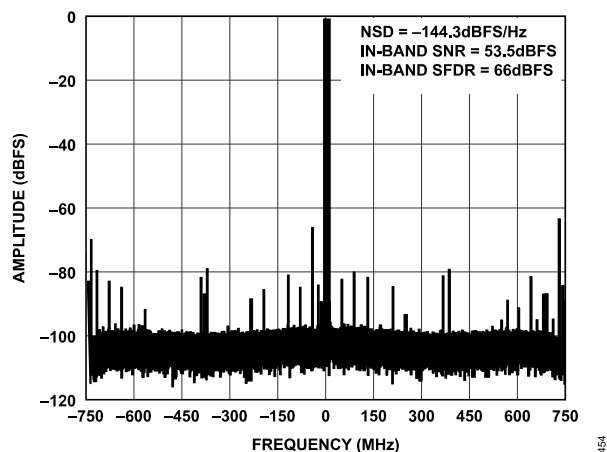
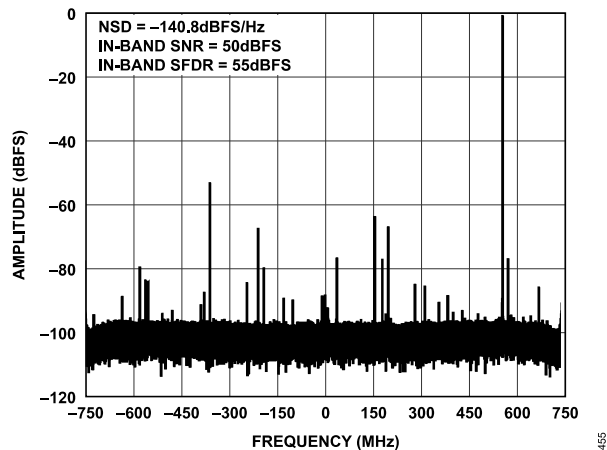
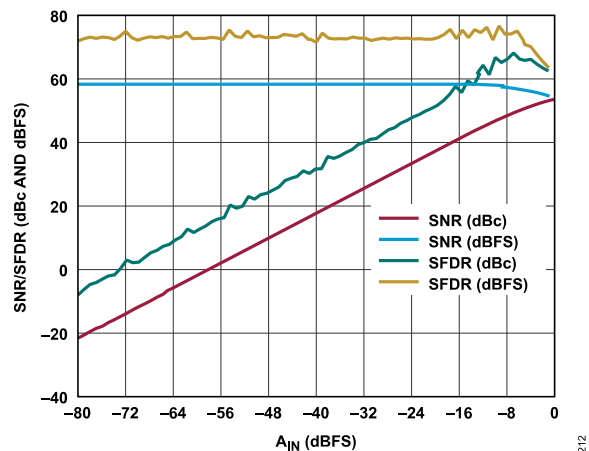
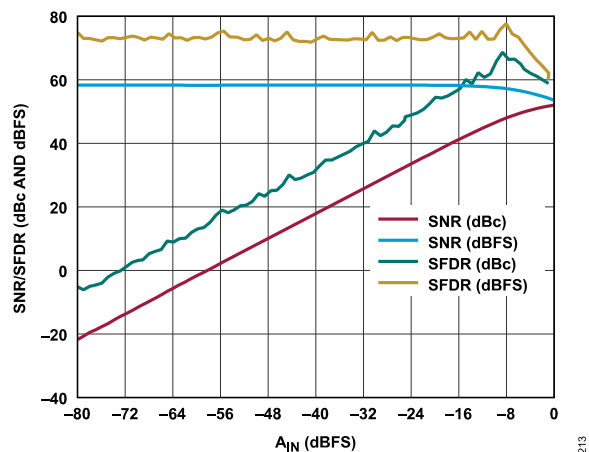
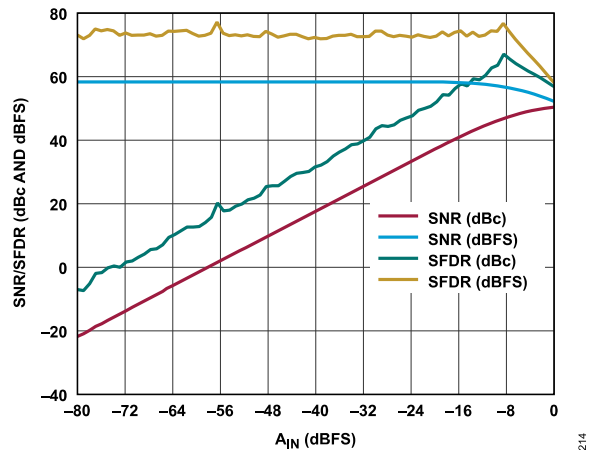
## TYPICAL PERFORMANCE CHARACTERISTICS

## ADC

Nominal supplies, sampling rate (sample frequency ( $f_S$ ) or  $f_{ADC}$ ) = 3 GSPS with DAC clock frequency ( $f_{CLK}$ ) = 12 GHz, direct RF clock. The ADC datapath is configured for a complex I/Q data rate ( $f_{IQ\_DATA}$ ) = 1500 MSPS and decimation of 2× with NCO tuned to  $f_S/4$  ( $f_S/4$  means the same as  $f_{ADC}/4$ ). JTx mode of 16C (L = 8, M = 8, F = 2, S = 1, K = 128, E = 1, N = 16, NP = 16),  $T_J = 80^\circ\text{C}$  ( $T_A = 25^\circ\text{C}$ ), 128k FFT sample with five averages, and  $A_{IN} = -1$  dBFS, unless otherwise noted.

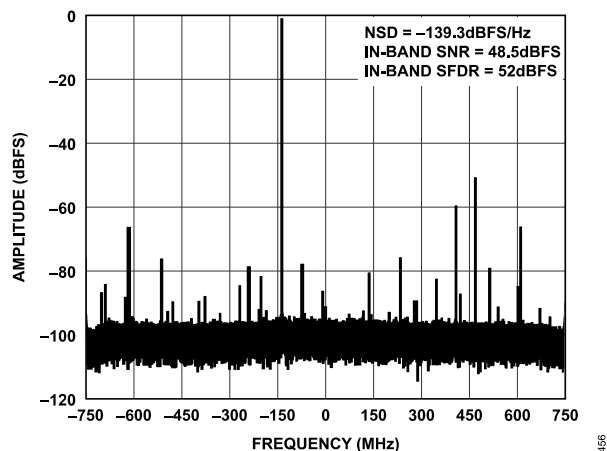
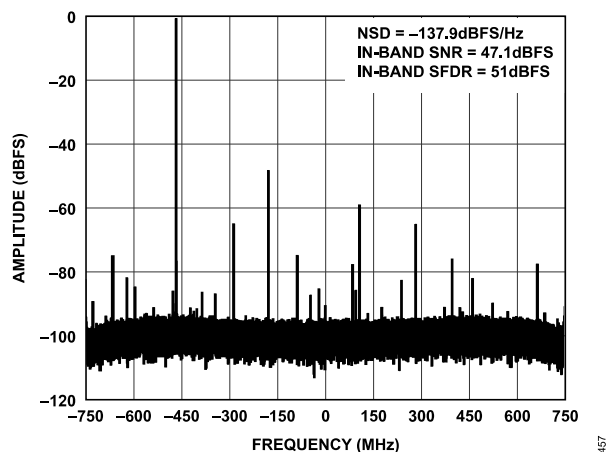
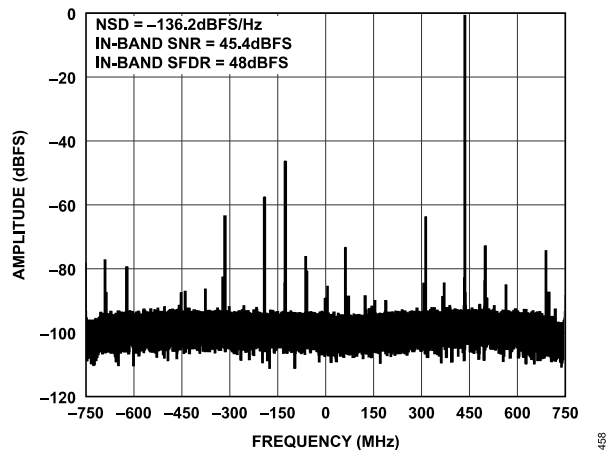
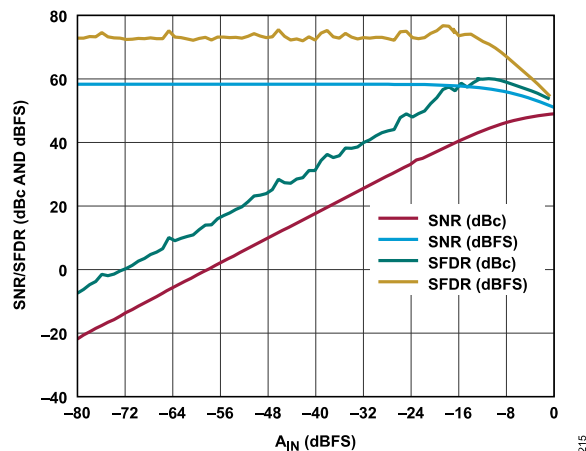
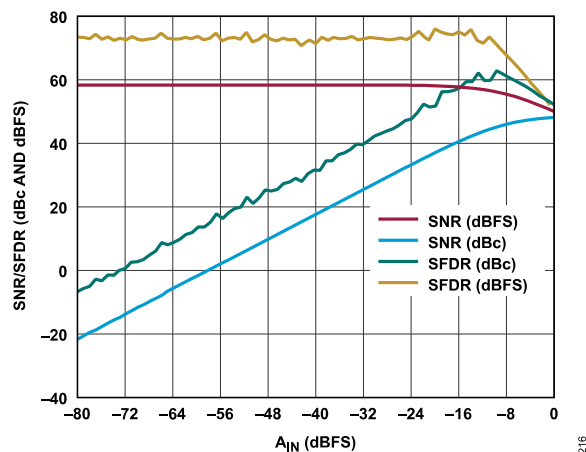
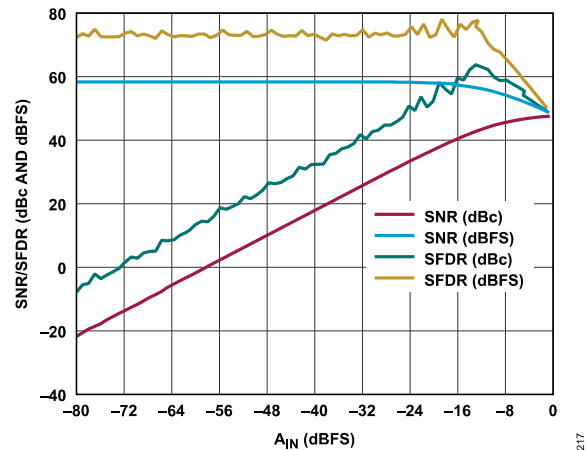
Figure 36. Single-Tone FFT at  $f_{IN} = 450$  MHzFigure 37. Single-Tone FFT at  $f_{IN} = 900$  MHzFigure 38. Single-Tone FFT at  $f_{IN} = 1800$  MHzFigure 39. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 450$  MHz,  $f_S = 4$  GSPSFigure 40. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 900$  MHz,  $f_S = 4$  GSPSFigure 41. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 1800$  MHz,  $f_S = 4$  GSPS

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 42. Single-Tone FFT at  $f_{IN} = 2700$  MHzFigure 43. Single-Tone FFT at  $f_{IN} = 3600$  MHzFigure 44. Single-Tone FFT at  $f_{IN} = 4700$  MHzFigure 45. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 2700$  MHz,  $f_S = 4$  GSPSFigure 46. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 3600$  MHz,  $f_S = 4$  GSPSFigure 47. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 4500$  MHz,  $f_S = 4$  GSPS



## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 48. Single-Tone FFT at  $f_{IN} = 5400$  MHzFigure 49. Single-Tone FFT at  $f_{IN} = 6300$  MHzFigure 50. Single-Tone FFT at  $f_{IN} = 7200$  MHzFigure 51. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 5400$  MHz,  $f_S = 4$  GSFSFigure 52. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 6300$  MHz,  $f_S = 4$  GSFSFigure 53. Single-Tone SFDR and SNR vs.  $A_{IN}$  at  $f_{IN} = 7200$  MHz,  $f_S = 4$  GSFS

## TYPICAL PERFORMANCE CHARACTERISTICS

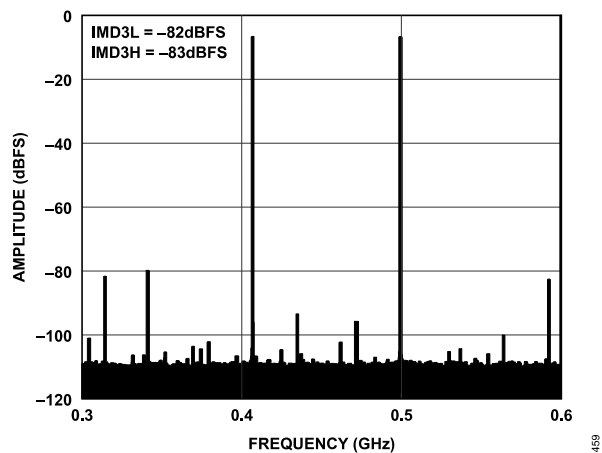


Figure 54. Two-Tone FFT,  $f_{IN1} = 1.775$  GHz,  $f_{IN2} = 1.825$  GHz,  $A_{IN1}$  and  $A_{IN2} = -7$  dBFS (IMD3L =  $2f_{IN1} - f_{IN2}$ , and IMD3H =  $2f_{IN2} - f_{IN1}$ ; IMD3L and IMD3H Are the Lower and Higher IMD3 Product Components, Respectively)

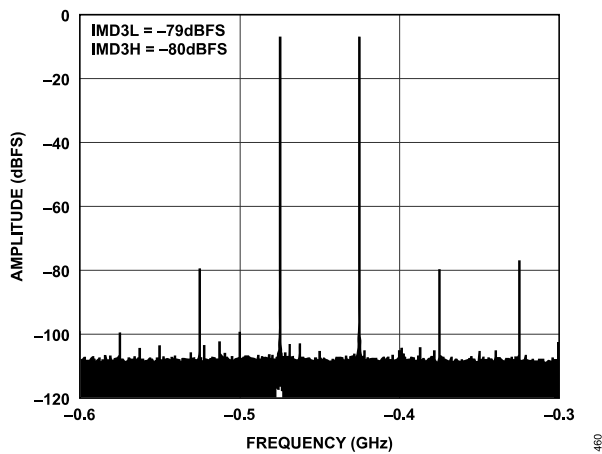


Figure 55. Two-Tone FFT,  $f_{IN1} = 2.675$  GHz,  $f_{IN2} = 2.725$  GHz,  $A_{IN1}$  and  $A_{IN2} = -7$  dBFS

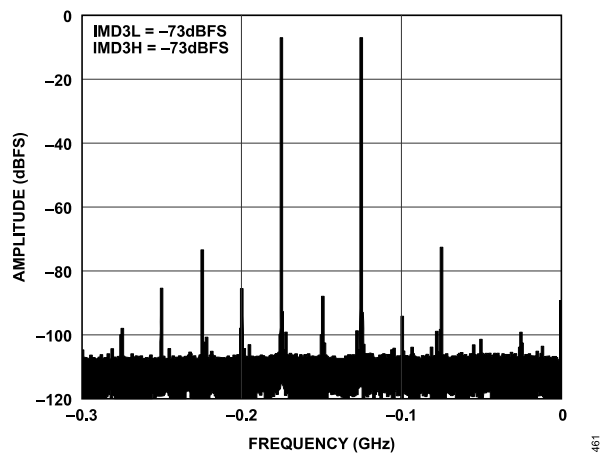


Figure 56. Two-Tone FFT,  $f_{IN1} = 3.575$  GHz,  $f_{IN2} = 3.625$  GHz,  $A_{IN1}$  and  $A_{IN2} = -7$  dBFS

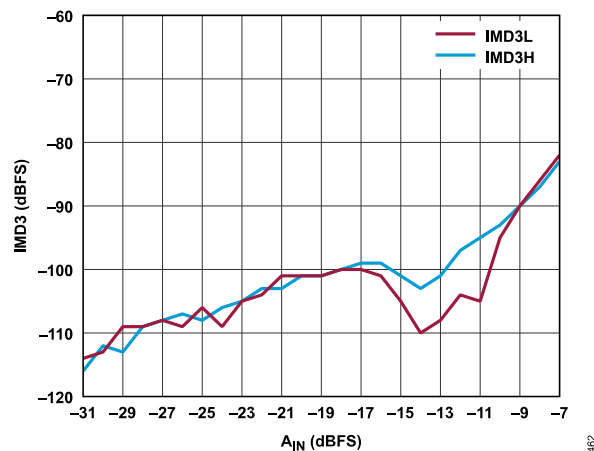


Figure 57. Two-Tone IMD vs.  $A_{IN}$  with  $f_{IN1} = 1.775$  GHz,  $f_{IN2} = 1.825$  GHz

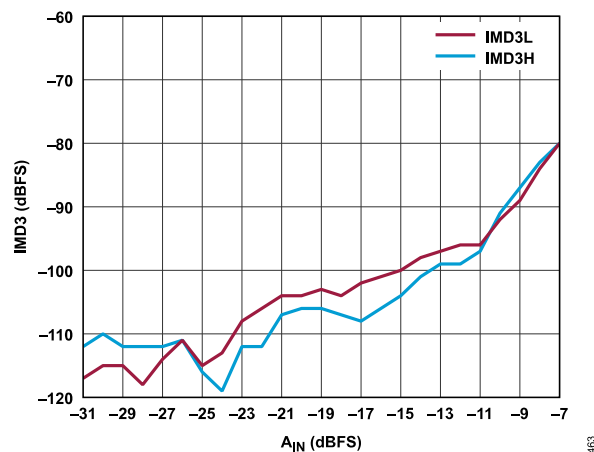


Figure 58. Two-Tone IMD vs.  $A_{IN}$  with  $f_{IN1} = 2.675$  GHz,  $f_{IN2} = 2.725$  GHz

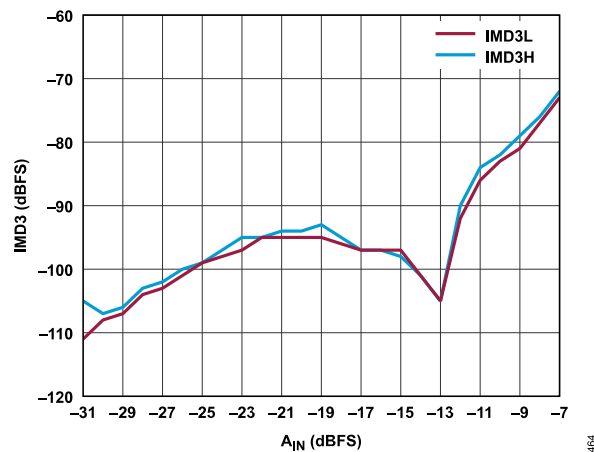


Figure 59. Two-Tone IMD vs.  $A_{IN}$  with  $f_{IN1} = 3.575$  GHz,  $f_{IN2} = 3.625$  GHz

## TYPICAL PERFORMANCE CHARACTERISTICS

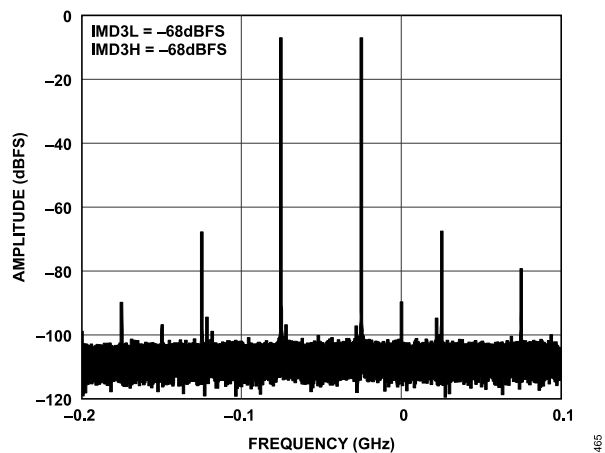


Figure 60. Two-Tone FFT,  $f_{IN1} = 5.375$  GHz,  $f_{IN2} = 5.425$  GHz,  $A_{IN1}$  and  $A_{IN2} = -7$  dBFS

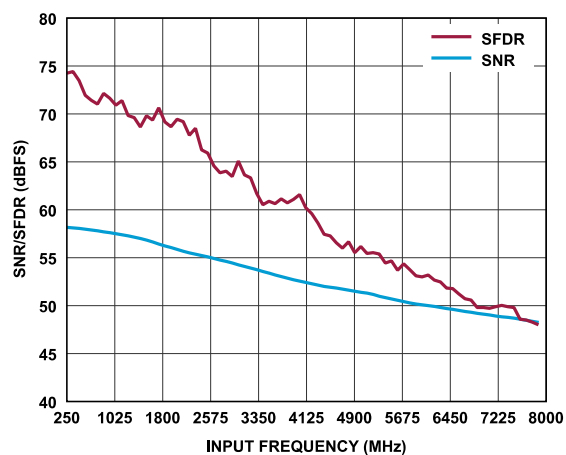


Figure 61. SNR and SFDR vs. Input Frequency with  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

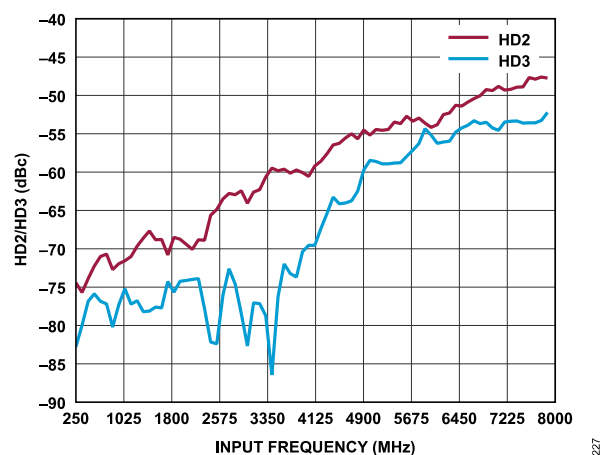


Figure 62. Harmonics (HD2 and HD3) vs. Input Frequency with  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

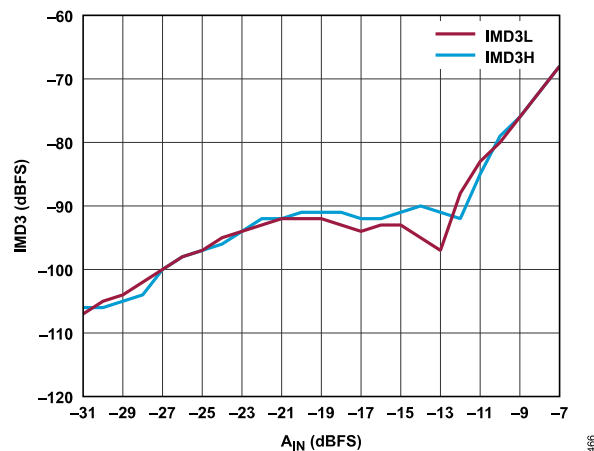


Figure 63. Two-Tone IMD3 vs.  $A_{IN}$  with  $f_{IN1} = 5.375$  GHz,  $f_{IN2} = 5.425$  GHz

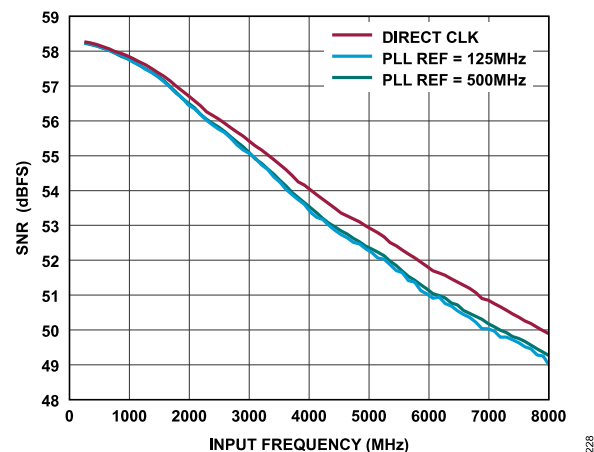


Figure 64. SNR vs. Input Frequency, Direct Clock vs. On-Chip PLL Clock,  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

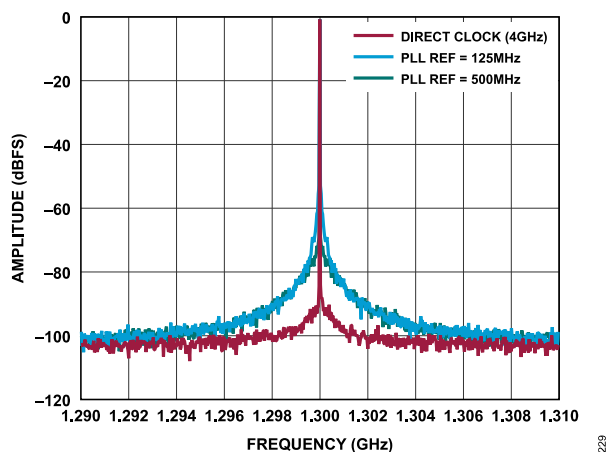


Figure 65. FFT Close-In Comparison, Direct Clock vs. On-Chip PLL Clock,  $f_{IN} = 2.7$  GHz,  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

## TYPICAL PERFORMANCE CHARACTERISTICS

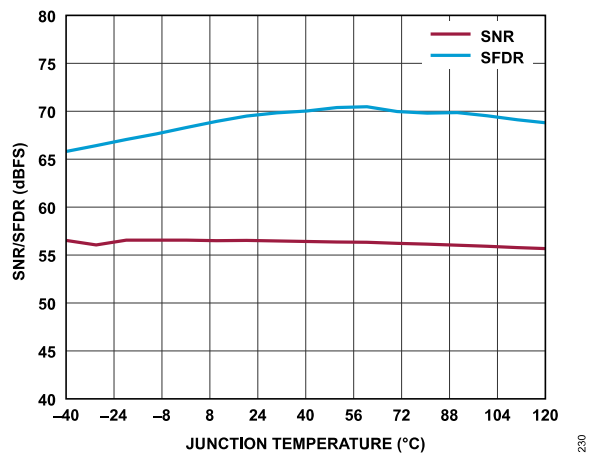


Figure 66. SNR and SFDR vs. Die Temperature,  $f_{IN} = 1.85$  GHz,  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

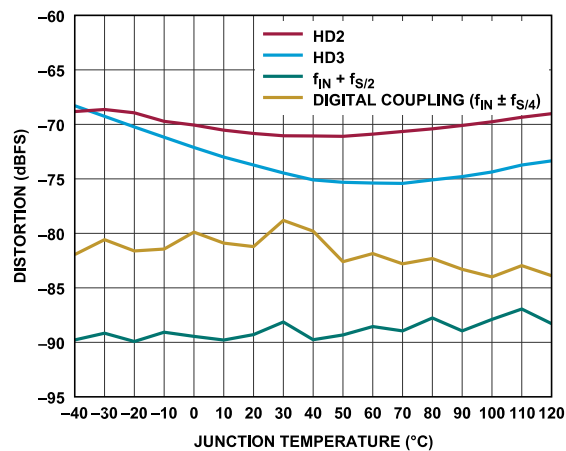


Figure 69. Harmonics (HD2, HD3, and Interleaving) vs. Junction Temperature,  $f_{IN} = 1.85$  GHz,  $f_S = 4$  GSPS

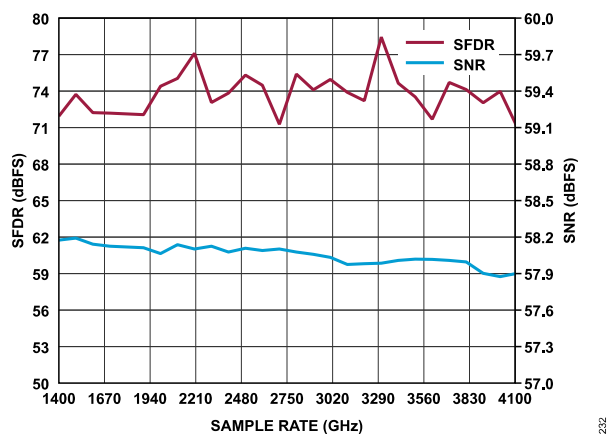


Figure 67. SNR and SFDR vs. Sample Frequency ( $f_S$ ),  $f_{IN} = 450$  MHz,  $f_S = 4$  GSPS

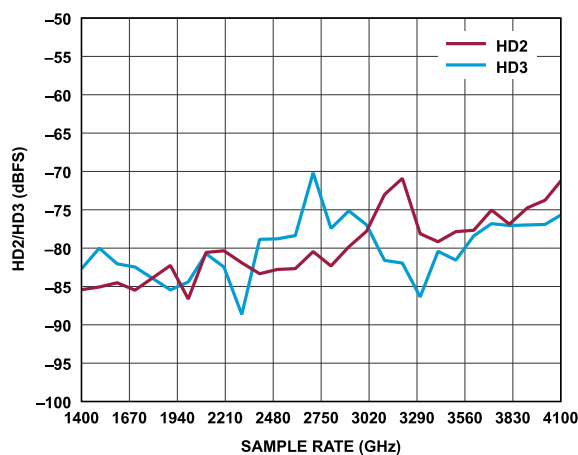


Figure 70. Harmonics (HD2 and HD3) vs. Sample Rate,  $f_{IN} = 450$  MHz

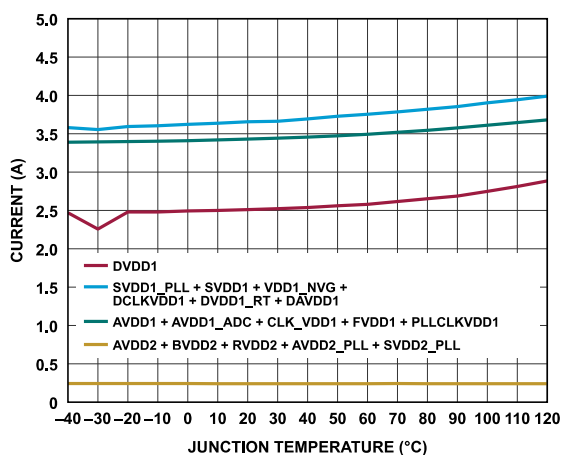


Figure 68. Power vs. Junction Temperature,  $f_{IN} = 1.85$  GHz,  $A_{IN} = -1$  dBFS,  $f_S = 4$  GSPS

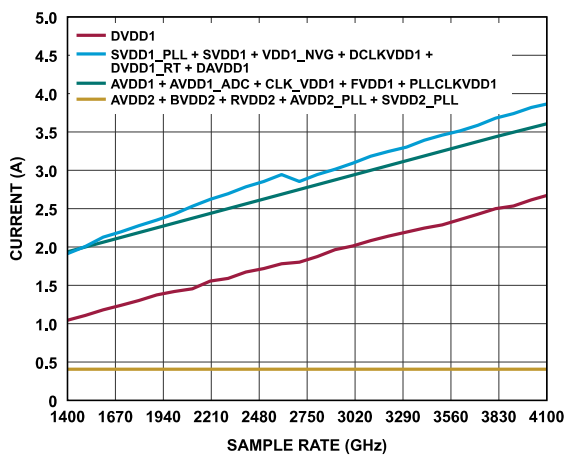


Figure 71. Power vs. Sample Rate,  $f_{IN} = 450$  MHz

## TYPICAL PERFORMANCE CHARACTERISTICS

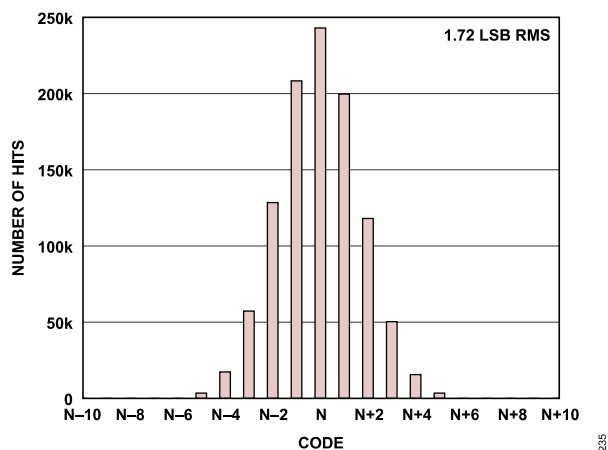
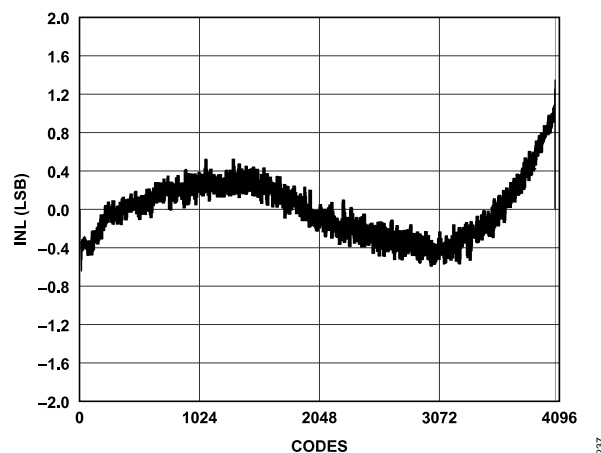
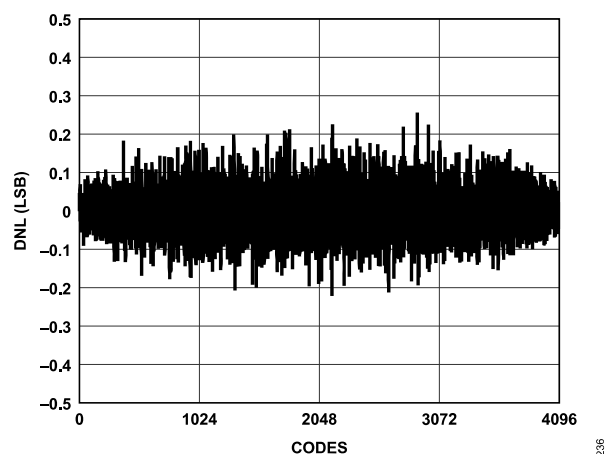
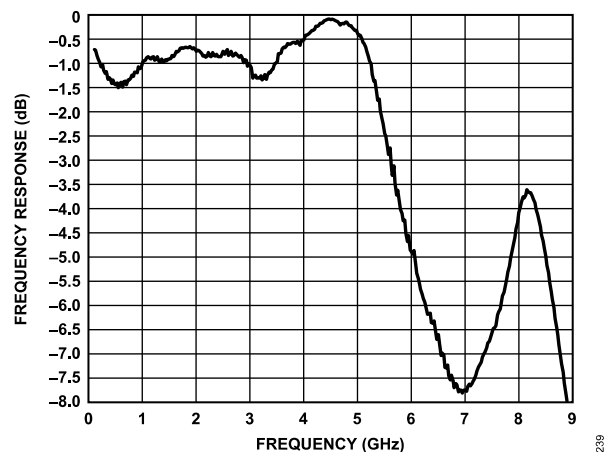


Figure 72. Input Referred Noise Histogram

Figure 75. INL,  $f_{IN} = 255$  MHzFigure 73. DNL,  $f_{IN} = 255$  MHzFigure 74. Measured Input Bandwidth ADC Input on AD9081-FMCA-EBZ  
(No Matching Network)

## THEORY OF OPERATION

The AD9988 is a highly integrated, mixed-signal, direct radio frequency (RF) sampling transceiver offering four transmitters and four receivers (4T4R) and digital signal processing (DSP) functions (see [Figure 1](#)). The device delivers a versatile combination of high performance, configurability, and low power consumption demanded by wireless infrastructure applications such as multiband macro 5G and mmWave 5G base station radios. The AD9988 also offers features to support the time division duplex (TDD) and the frequency division duplex (FDD) techniques.

The receive path consists of four pipelined, 12-bit, 4 GSPS rate, RF analog-to-digital converter (ADC) cores. The transmit path consists of four 16-bit, 12 GSPS maximum sample rate, RF digital-to-analog converter (DAC) cores. Both receive and transmit paths are designed and optimized to sample and synthesize signals up to 7.5 GHz, with maximum instantaneous bandwidths of up to 1.2 GHz with a sample resolution of 16 bits. The device also supports lower resolutions such as 12 bits and 8 bits to reduce the bit rate of the JESD204B/C link for applications that do not require the higher dynamic range a 16-bit resolution offers. The wide instantaneous bandwidth allows the chip to support multiple carrier bands or a single wide band within a single device. The combination of the direct RF conversion architecture relaxes the requirements of the RF filters when compared to traditional intermediate frequency (IF) receivers. Several auxiliary functions, such as fast detect and signal monitor, a programmable finite impulse response (FIR) filter, trans-

mit downstream power amplifier protection, and general-purpose inputs/output (GPIO) control are also integrated.

The DAC and ADC cores use sampling clocks that originate from either an external clock source or an on-chip clock multiplier that consists of an integer PLL circuit and voltage-controlled oscillator (VCO).

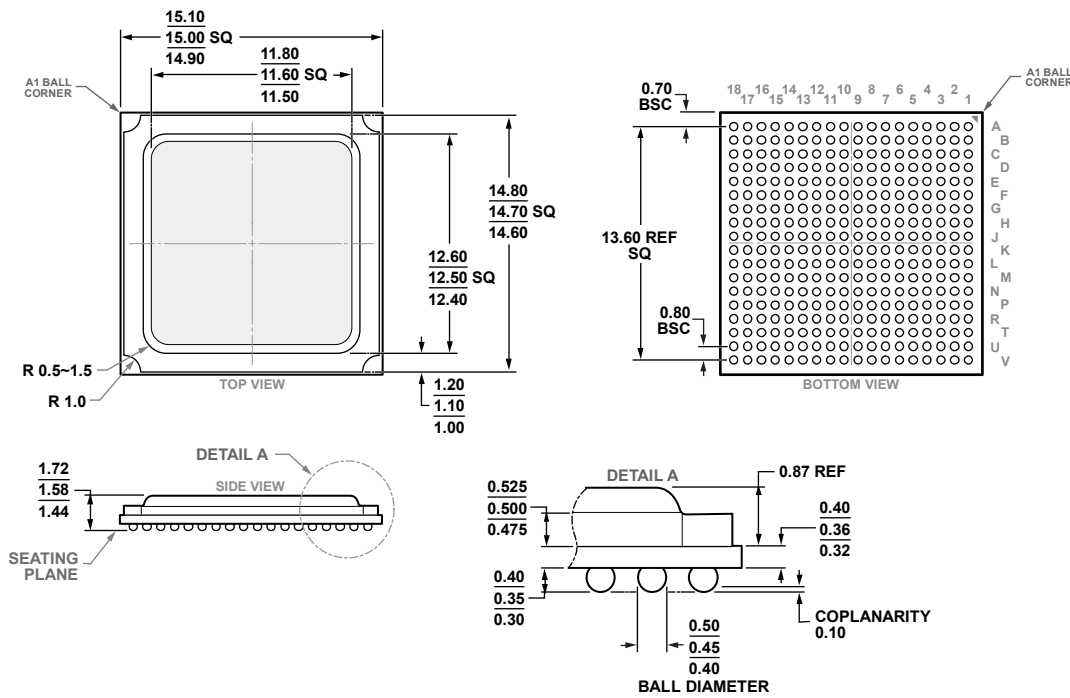
The device features eight transmit and eight receive lanes, where each lane supports up to 24.75 Gbps JESD204C or up to 15.5 Gbps JESD204B as a single or a dual link. Multichip synchronization and deterministic latency are supported according to JESD204B/C Subclass 1. The JESD204B/C interface supports a wide range of setups depending on the interface bandwidth requirements of the custom application specific IC (ASIC) or field-programmable gate array (FPGA). Refer to [UG-1578](#), the device user guide, for more information on device features and operation.

The AD9988 has an on-chip thermal management unit (TMU) that can be used to measure die junction temperature as part of a thermal management solution to guarantee thermal stability during system operation. The device is controlled via a standard 4-wire serial port interface (SPI) with support for 3-wire SPI communications. A comprehensive set of power-down modes are included to minimize power consumption during system downtime. The AD9988 is packaged in a 15 mm × 15 mm, 324-ball, thermally enhanced, ball grid array (BGA\_ED).

## APPLICATIONS INFORMATION

Refer to [UG-1578](#), the device user guide, for more information on device initialization and other Applications Information.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1

Figure 76. 324-Ball Ball Grid Array, Thermally Enhanced [BGA\_ED]  
(BP-324-3)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range <sup>2</sup> | Package Description | Ordering Quantity | Package Option |
|--------------------|--------------------------------|---------------------|-------------------|----------------|
| AD99988BBPZ-4D4AC  | -40°C to +120°C                | 324-Ball BGA_ED     | Tray, 126         | BP-324-3       |
| AD9988BBPZRL-4D4AC | -40°C to +120°C                | 324-Ball BGA_ED     | Reel, 1000        | BP-324-3       |

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> Specified operating junction temperature (T<sub>J</sub>).

## EVALUATION BOARDS

| Model           | Description             |
|-----------------|-------------------------|
| AD9988-FMCB-EBZ | AD9988 Evaluation Board |