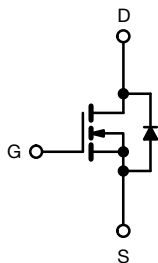


# Power MOSFET

**TO-220 FULLPAK**


N-Channel MOSFET

## FEATURES

- Isolated package
- High voltage isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Logic-level gate drive
- R<sub>DS(on)</sub> specified at V<sub>GS</sub> = 4 V and 5 V
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

## PRODUCT SUMMARY

V <sub>DS</sub> (V)	100	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 5 V	0.077
Q <sub>g</sub> (Max.) (nC)	64	
Q <sub>gs</sub> (nC)	9.4	
Q <sub>gd</sub> (nC)	27	
Configuration	Single	

## DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

## ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRLI540GPbF

## ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V <sub>DS</sub>	100	V
Gate-source voltage			V <sub>GS</sub>	± 10	
Continuous drain current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	17	A
		T <sub>C</sub> = 100 °C		12	
Pulsed drain current <sup>a</sup>			I <sub>DM</sub>	68	
Linear derating factor				0.32	W/°C
Single pulse avalanche energy <sup>b</sup>			E <sub>AS</sub>	400	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	48	W
Peak diode recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns
Operating junction and storage temperature range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s			300 <sup>d</sup>	
Mounting torque	M3 screw			0.6	

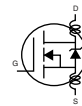

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V<sub>DD</sub> = 25 V, starting T<sub>J</sub> = 25 °C, L = 2.1 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 17 A (see fig. 12)
- I<sub>SD</sub> ≤ 28 A, dI/dt ≤ 170 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 175 °C
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	3.1	

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-ssource breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		100	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.12	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.0	-	2.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 5 V	I <sub>D</sub> = 10 A <sup>b</sup>	-	-	0.077	Ω
		V <sub>GS</sub> = 4 V	I <sub>D</sub> = 8.5 A <sup>b</sup>	-	-	0.11	
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 10 A <sup>b</sup>		12	-	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	2200	-	pF
Output capacitance	C <sub>OSS</sub>			-	560	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	140	-	
Drain to sink capacitance	C	f = 1.0 MHz		-	12	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 5 V	I <sub>D</sub> = 28 A, V <sub>DS</sub> = 80 V, see fig. 6 and 13 <sup>b</sup>	-	-	64	nC
Gate-source charge	Q <sub>gs</sub>			-	-	9.4	
Gate-drain charge	Q <sub>gd</sub>			-	-	27	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 28 A, R <sub>g</sub> = 4.5 Ω, R <sub>D</sub> = 1.7 Ω, see fig. 10 <sup>b</sup>		-	8.5	-	ns
Rise time	t <sub>r</sub>			-	170	-	
Turn-off delay time	t <sub>d(off)</sub>			-	35	-	
Fall time	t <sub>f</sub>			-	80	-	
Internal drain inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	17	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>			-	-	68	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 17 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.5	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 28 A, dI/dt = 100 A/μs <sup>b</sup>		-	130	260	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	1.5	2.9	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

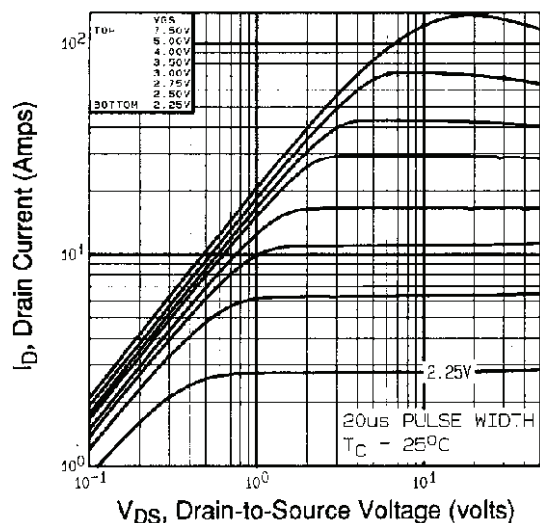


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

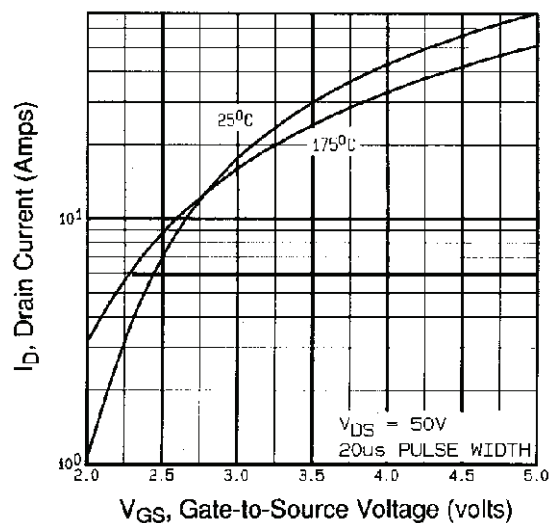


Fig. 2 - Typical Transfer Characteristics

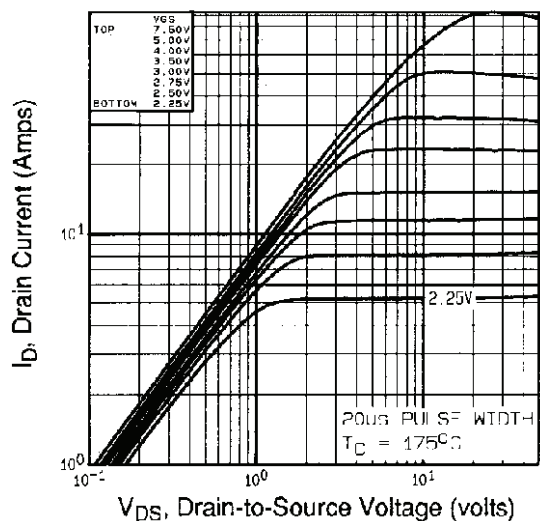


Fig. 1 - Typical Output Characteristics,  $T_C = 175\text{ }^{\circ}\text{C}$

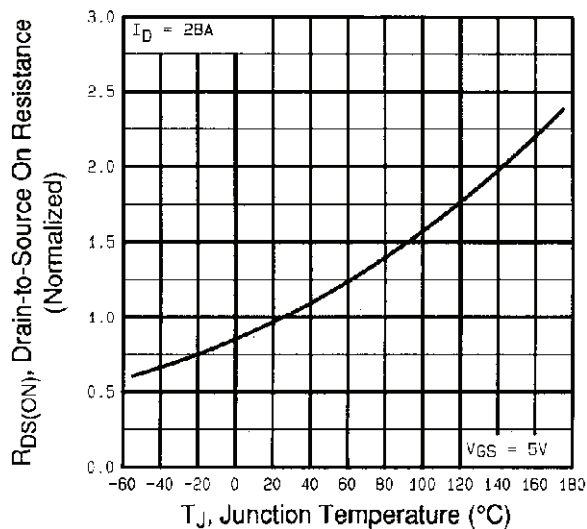
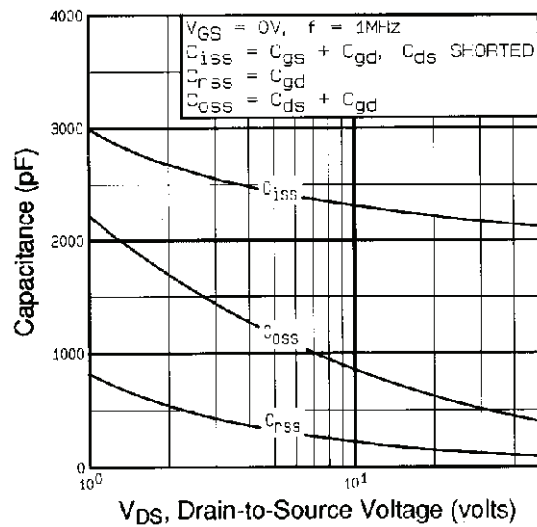
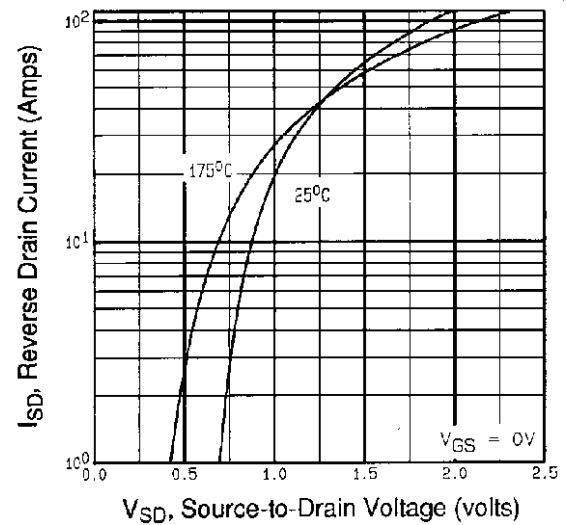
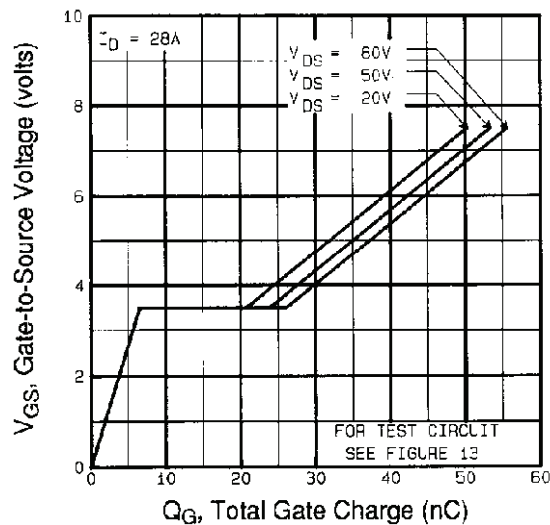
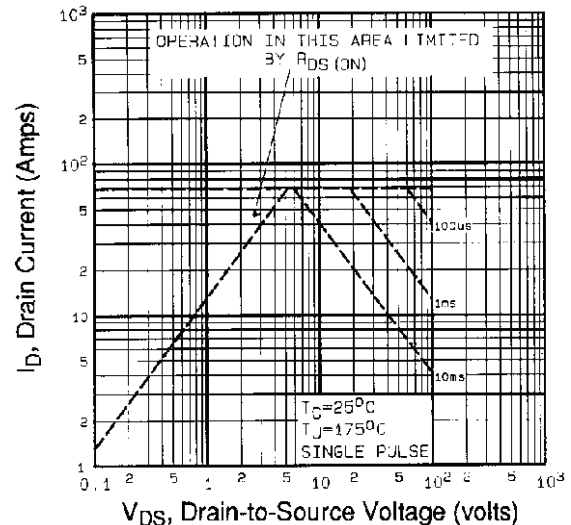
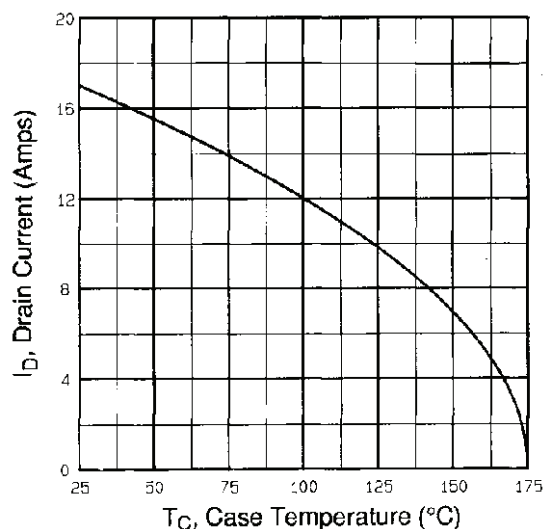
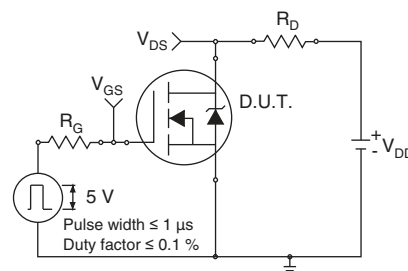
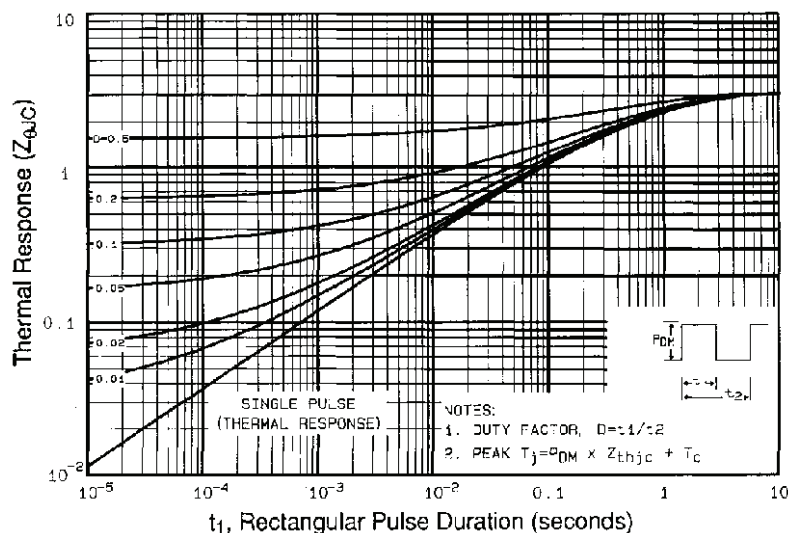
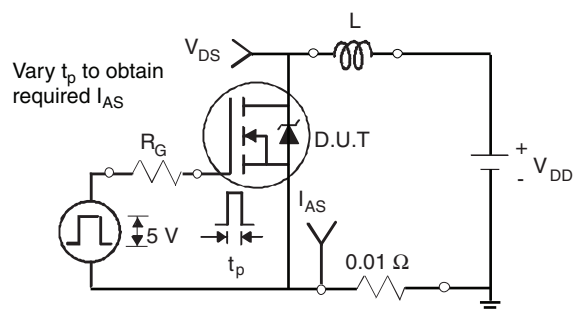
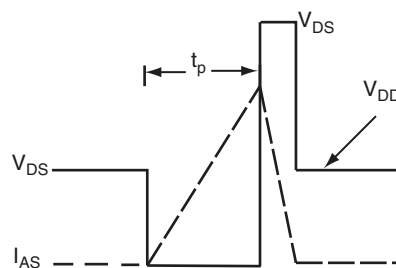
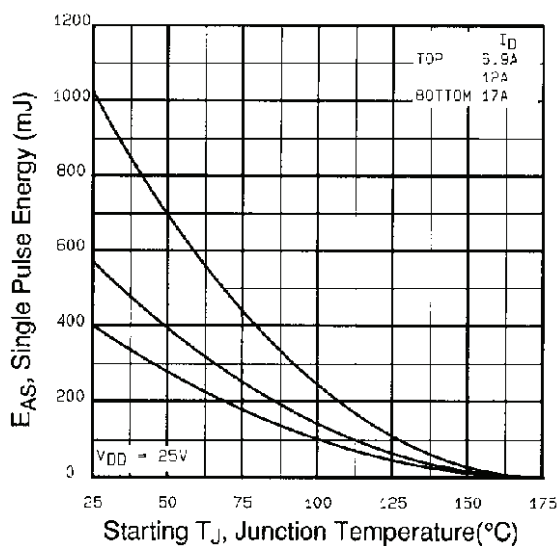


Fig. 3 - Normalized On-Resistance vs. Temperature

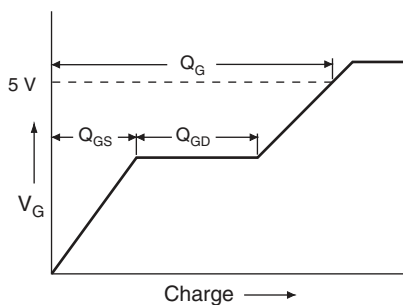

**Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6 - Typical Source-Drain Diode Forward Voltage**

**Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 7 - Maximum Safe Operating Area**


**Fig. 8 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

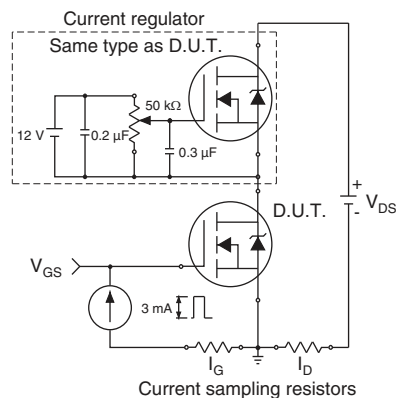
**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

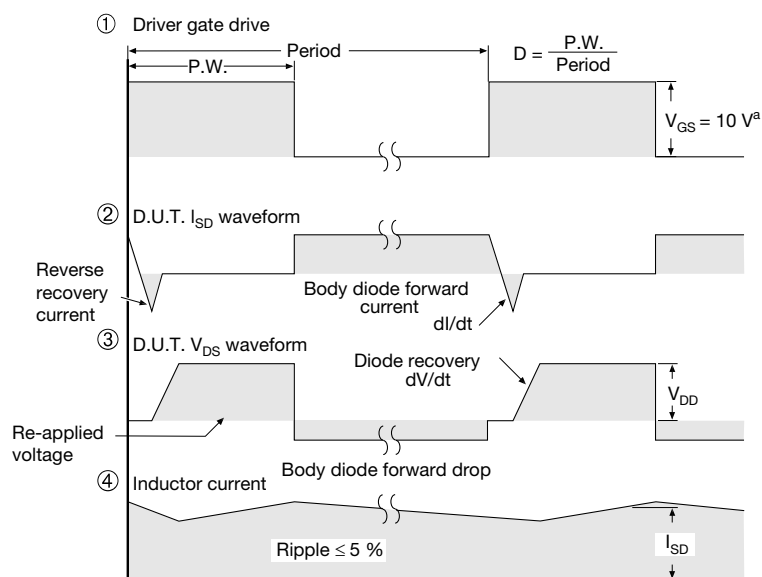
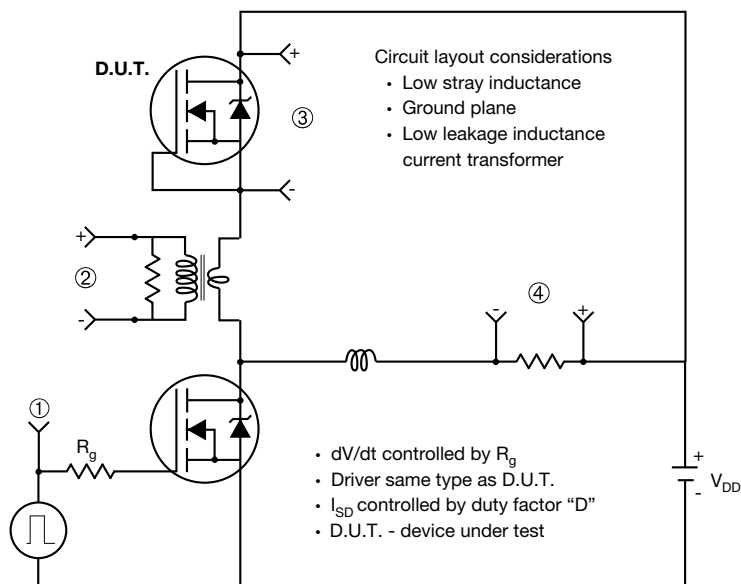


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

### Peak Diode Recovery dV/dt Test Circuit



#### Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

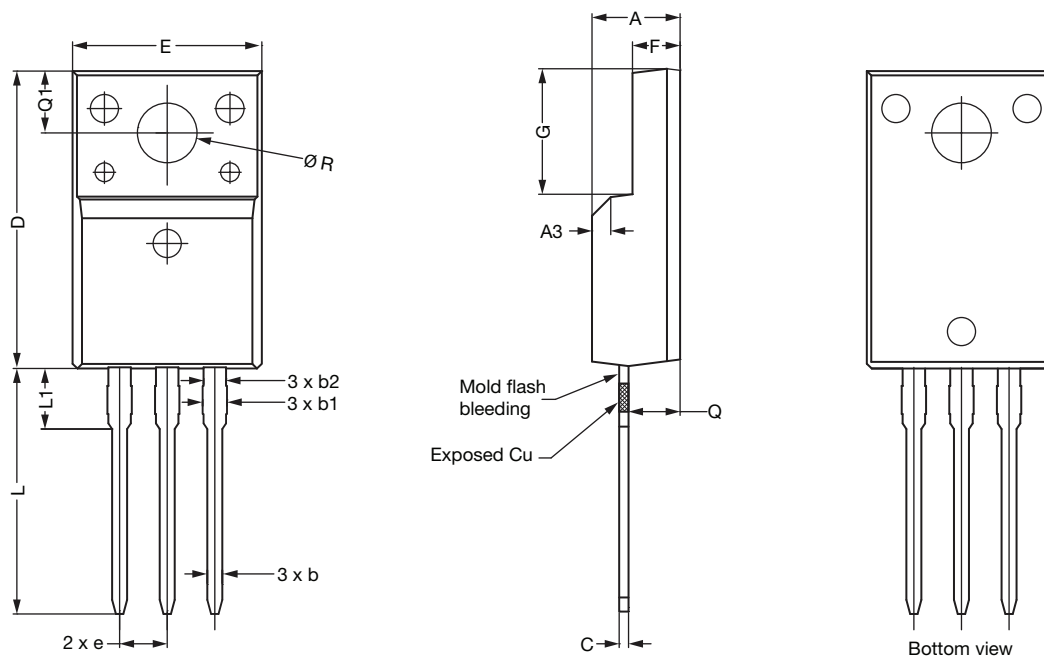
**Fig. 9 - For N-Channel**

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## TO-220 FULLPAK (High Voltage)

### OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

#### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





## OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

### Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
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