

# LC898113

CMOS LSI

## Optical Image Stabilization (OIS) Controller & Driver



ON Semiconductor®

www.onsemi.com

### Overview

The LC898113 is a device integrating digital gyro interface, gyro filter, stepping motor control circuit, and motor driver functions needed to implement an Optical Image Stabilization (OIS) system using stepping motors. These functions make it possible to build a system using a minimal software program that enables the host microcontroller to turn Optical Image Stabilization (OIS) on and off, for example.

The gyro filter coefficients may be set to any values by the host microcontroller, making it possible to build filter circuits optimized for the system. The LC898113 integrates a signal determination circuit for pan/tilt processing and a filter circuit, enabling implementation of a variety of processing in response to camera movements.

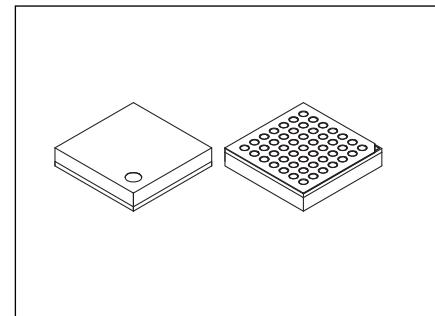
The LC898113 integrates four saturation-drive H-bridge channels for stepping motor drive, and PWM drive with 1-2-phase control to 8W1-2-phase control is supported.

Also integrated are a photo sensor drive circuit for control object position detection (for example, a CMOS sensor), a position determination circuit, and a circuit for moving to the optical center based on the results from the preceding circuits. Thus, the host microcontroller can specify detection start and the LC898113 will automatically move the control object to the initial position.

Both SPI and I<sup>2</sup>C are supported as serial interfaces for communication with the host microcontroller. This allows the customer to choose based on the specifications of the host microcontroller. The I<sup>2</sup>C interface also supports a 1.8 V interface.

### Features

- Serial interface
  - SPI (mode0, mode3)
  - I<sup>2</sup>C (F/S mode)
  - Selection with MODE0 pin
- Built in Gyro filter
- Digital Gyro Support
  - Built in Digital Gyro I/F for each manufacturer
- Stepping motor drive mode
  - 1-2 phase
  - W1-2 phase
  - 2W1-2 phase
  - 4W1-2 phase
  - 8W1-2 phase



LFLGA49 4x4 / FLGA49

Continued on next page.

\* I<sup>2</sup>C Bus is a trademark of Philips Corporation.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Continued from preceding page.

- Stepping motor driver integrated in an MCP  
Saturation driven H bridge 4ch  
Built in thermal protection circuit  
Built in low voltage malfunction prevention circuit  
Built in transistor for photo sensor drive  
Two driver power supplies (VM : for motor, VCC : for others)
- Operation Clock  
Clock generated from built in oscillation amplifier  
Clock input directly from CLKIN pin  
Selection with MODE1 pin  
Recommended drive frequency 24MHz, Permission drive frequency 15MHz to 36MHz
- Package  
FLGA49 (4mm × 4mm)  
Pb-Free  
Halogen Free
- Power supply voltage (Typical voltage)  
Logic LSI : Pin 3.3V, Inside 1.8V (External supply required)  
Driver LSI : VM 5.0V, VCC 3.3V

## Electrical Characteristics

### Absolute Maximum Ratings at VSS = 0V

Parameter	Symbol	Conditions	Ratings	unit
Power supply voltage	V <sub>DD18</sub> max	T <sub>a</sub> ≤ 25°C	-0.3 to 3.6	V
	V <sub>DD33</sub> max	T <sub>a</sub> ≤ 25°C	-0.3 to 4.6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### D.C. Characteristics: Input/output level/VSS = 0V, VDD = 2.7 to 3.6V, Ta = -30 to 85°C

Parameter	Symbol	Conditions	min	typ	max	unit	Applicable pin
High-level input voltage	V <sub>IH</sub>	CMOS schmidt	1.4			V	(1)
Low-level input voltage	V <sub>IL</sub>				0.36	V	
High-level input voltage	V <sub>IH</sub>	CMOS schmidt	1.4			V	(2)
Low-level input voltage	V <sub>IL</sub>				0.50	V	
High-level input voltage	V <sub>IH</sub>	CMOS schmidt	1.5			V	(3)
Low-level input voltage	V <sub>IL</sub>				0.36	V	

\*Applicable pin

(1)ZRESET

(2)CLKIN

(3)SCLK, MOSI

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

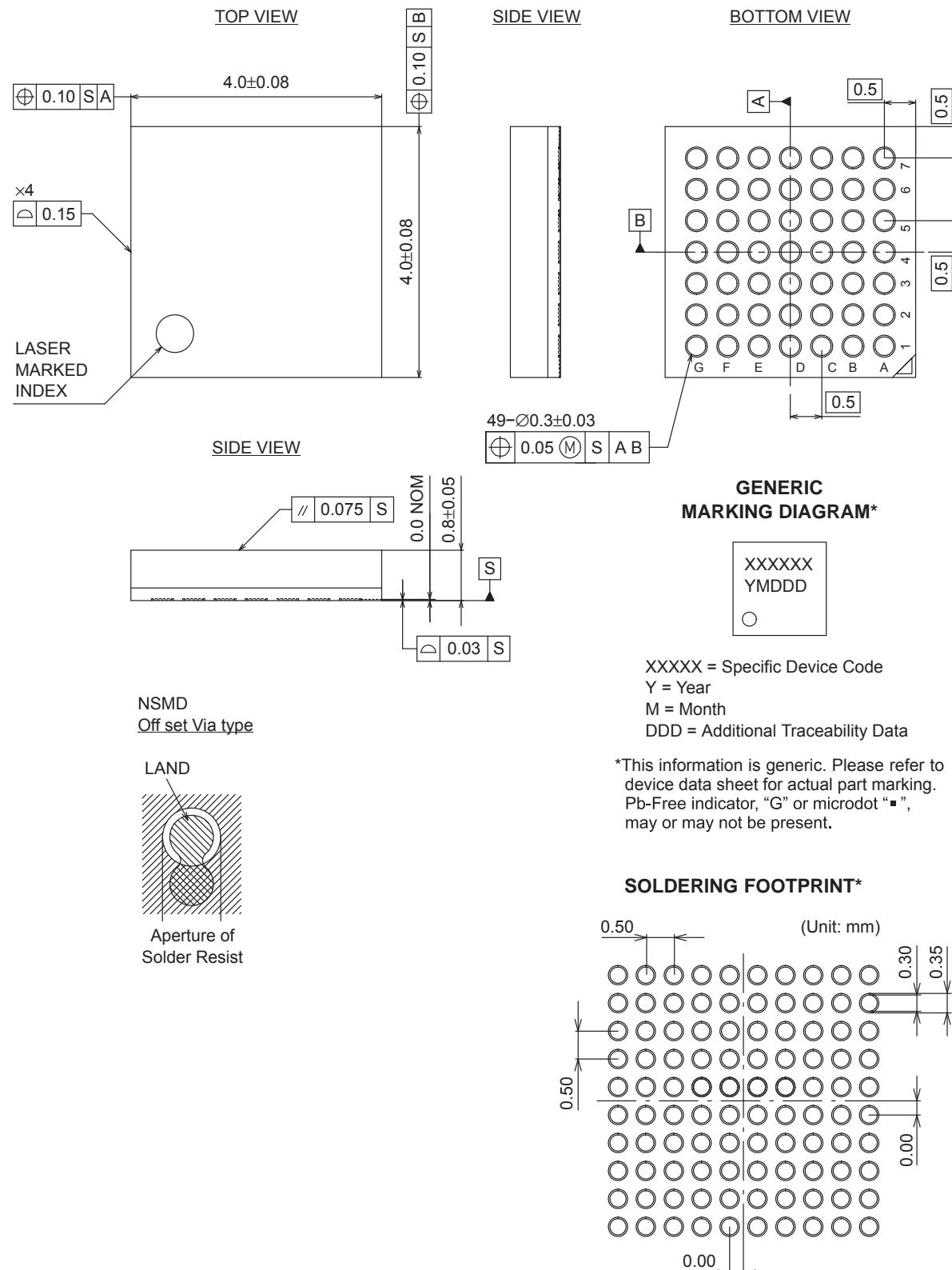
**Package Dimensions**

unit : mm

**LFLGA49 4x4 / FLGA49**

CASE 569AM

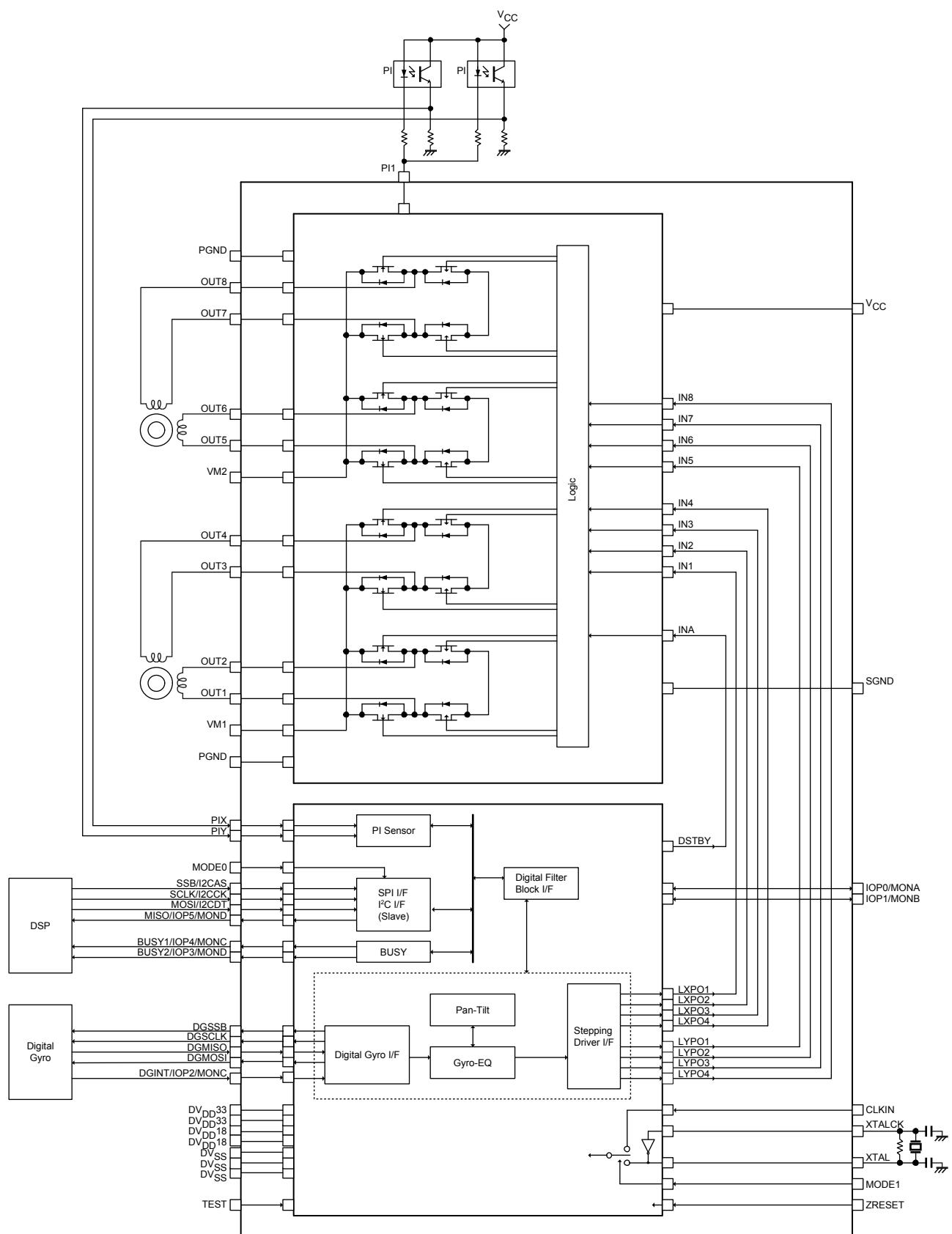
ISSUE A



NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Block Diagram



## Pin Description

TYPE					
I	INPUT	P	Power, GND	NC	NOT CONNECT
O	OUTPUT				
B (I)	BIDIRECTION : INPUT at reset				
B (O)	BIDIRECTION : OUTPUT at reset				

## Logic LSI

### SPI/I<sup>2</sup>C interface (Slave)

SSB/I2CSA	I	SPI chip select/ I <sup>2</sup> C slave address select (L: 0100100, H: 0100101, Please make sure to connect the pin to L level or H level.)
SCLK/I2CCK	B (I)	SPI clock/I <sup>2</sup> C clock
MOSI/I2CDT	B (I)	SPI received data/I <sup>2</sup> C data
MISO/IOP5/MOND	B (O)	SPI transmit data/Monitor pin

### Sensor output signal input for reference point detection

PIX	B(I)
PIY	B(I)

### Digital gyro interface

DGSSB	O	Digital gyro I/F chip select
DGSCLK	O	Digital gyro I/F transfer clock
DGMOSI	O	Digital gyro I/F transmit data
DGMISO	I	Digital gyro I/F received data
DGINT/IOP2/MONC	B (I)	Digital gyro I/F timing signal/General-purpose port/Monitor pin

### PIO interface

IOP0/MONA	B (I)	General-purpose port/Monitor pin
IOP1/MONB	B (I)	General-purpose port/Monitor pin

### BUSY flag

BUSY1/IOP4/MONC	B (O)	BUSY pin (RAM access BUSY signal when SPI I/F is selected)
BUSY2/IOP3/MOND	B (O)	BUSY pin (Stepping motor force movement busy, measurement busy etc.)

### Clock, Reset pin

XTALCK	I	Oscillation amplifier input (recommended drive frequency : 24MHz, permission drive frequency : 15MHz to 36MHz)
XTAL	O	Oscillation amplifier output
CLKIN	I	Clock input (Refer to XTALCK description about both recommended and permission drive frequency)
ZRESET	I	Power-on reset

### Mode select pin

MODE0	I	Interface select : L→SPI, H→I <sup>2</sup> C
MODE1	I	Clock select : L→XTALCK/XTAL use, H→CLKIN use

### Test pin

TEST	I	For test mode setting (fixed to L for normal operation)
------	---	---

### Power supply pin

DVDD33	P	3.3V digital power supply
DVDD18	P	1.8V digital power supply
DVSS	P	Digital ground

## \*Process when pins are not used

PIN TYPE "O" —— The pin must be left open.

PIN TYPE "I" —— The pin must not be left open. Please make sure to connect the pin to VDD or VSS even when it is not used. (Please check with us whether to connect to VDD or VSS.)

PIN TYPE "B" —— Please contact us if you are uncertain about a processing method in the pin description in the PIN layout table.

A problem may occur if the processing method is used wrongly for any unused pin.

Please make sure to contact us.

## Driver LSI

Saturation-driven H bridge output

OUT1 to OUT8      O      Motor control pulse output

Power supply pin

VM1,VM2	P	Motor power supply
VCC	P	Other power supply
SGND	P	Signal ground
PGND	P	Power ground

Photo sensor pin

PI1      I      Photo sensor connectiong pin

## Pin Assignment

Top View

7	OUT7	OUT8	PGND2	VM2	DV <sub>SS</sub>	IOP1	CLKIN
6	OUT6	NC	NC	DV <sub>DD33</sub>	DV <sub>DD18</sub>	PIX	XTAL
5	OUT5	NC	DGMISO	ZRESET	DV <sub>SS</sub>	PIY	XTALCK
4	OUT4	DGINT	DGSSB	DGMOSI	BUSY2	BUSY1	MODE1
3	OUT3	NC	DGSCLK	MODE0	SSB	MOSI	SCLK
2	OUT2	IOP0	NC	TEST	DV <sub>DD18</sub>	MISO	DV <sub>DD33</sub>
1	PGND1	OUT1	VM1	VCC	SGND	PI1	DV <sub>SS</sub>

## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898113-TBM-H	LFLGA49 4x4 / FLGA49 (Pb-Free / Halogen Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.