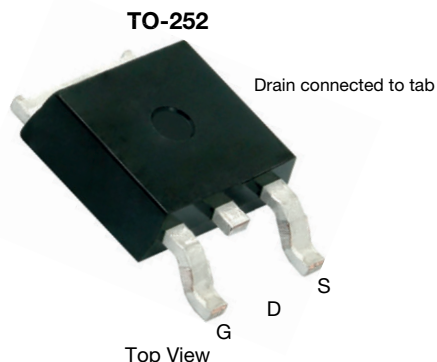


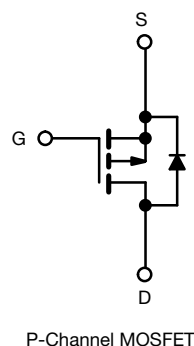
# Automotive P-Channel 30 V (D-S) 175 °C MOSFET



## FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 %  $R_g$  and UIS tested
- AEC-Q101 qualified
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


## PRODUCT SUMMARY

$V_{DS}$ (V)	-30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -10$ V	0.00320
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.00520
$I_D$ (A)	-100
Configuration	Single
Package	TO-252

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	-30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C <sup>a</sup>	A
		$T_C = 125$ °C	
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	-100	
Pulsed drain current <sup>b</sup>	$I_{DM}$	-300	
Single pulse avalanche current	$I_{AS}$	-41	
Single pulse avalanche energy	$E_{AS}$	84	mJ
Maximum power dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	W
		$T_C = 125$ °C	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	50	°C/W
Junction-to-case (drain)	$R_{thJC}$	1.1	

### Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)

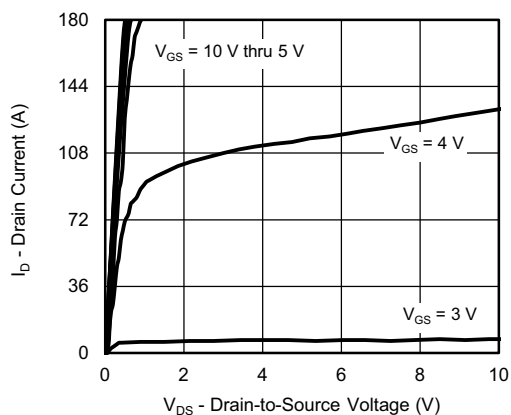
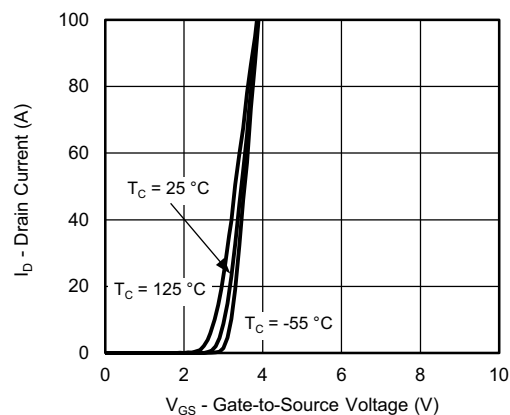
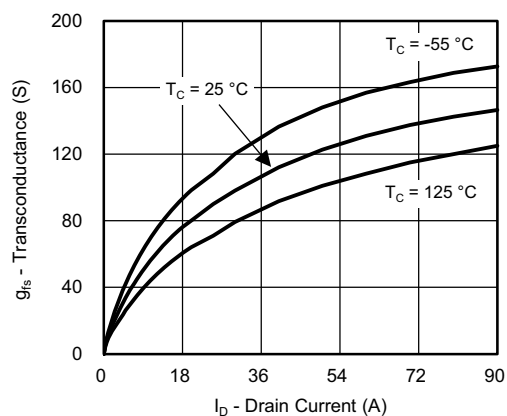
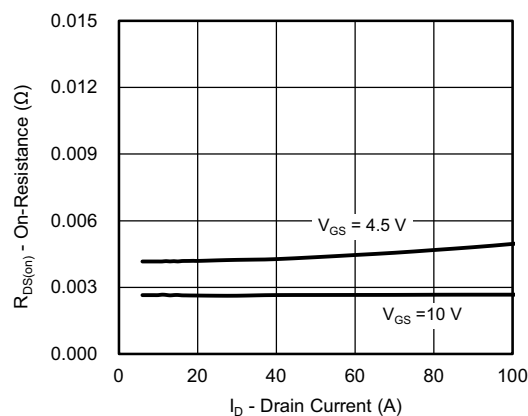
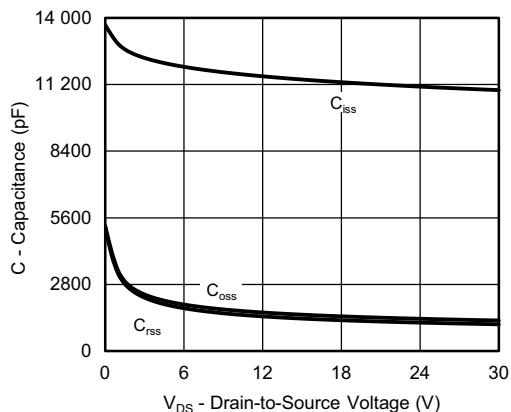
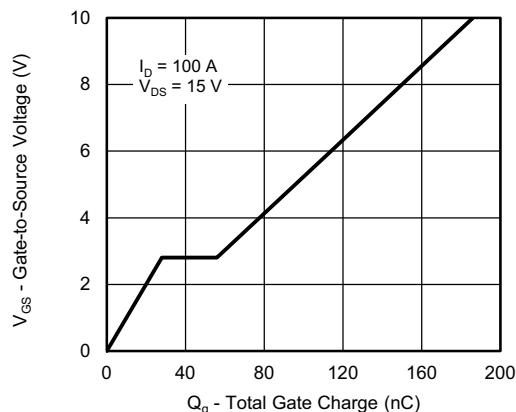


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA		-30	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-1.5	-2.0	-2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V	-	-	-1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≥ -5 V	-50	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -30 A	-	0.00263	0.00320	Ω
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -30 A, T <sub>J</sub> = 125 °C	-	-	0.00438	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -30 A, T <sub>J</sub> = 175 °C	-	-	0.00502	
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -25 A	-	0.00425	0.00520	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = 30 A		-	98	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -25 V, f = 1 MHz	-	11 085	15 000	pF
Output capacitance	C <sub>oss</sub>			-	1342	1900	
Reverse transfer capacitance	C <sub>rss</sub>			-	1181	1600	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -100 A	-	186	280	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	28	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	28	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		1.7	3.5	5.3	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 0.2 Ω I <sub>D</sub> ≅ -100 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω		-	16	25	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	204	310	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	126	190	
Fall time <sup>c</sup>	t <sub>f</sub>			-	72	110	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	-300	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = -30 A, V <sub>GS</sub> = 0 V		-	-0.8	-1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -40 A, di/dt = 100 A/μs		-	66	135	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	100	200	nC
Reverse recovery fall time	t <sub>a</sub>			-	31	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	35	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-3.4	-	A

**Notes**

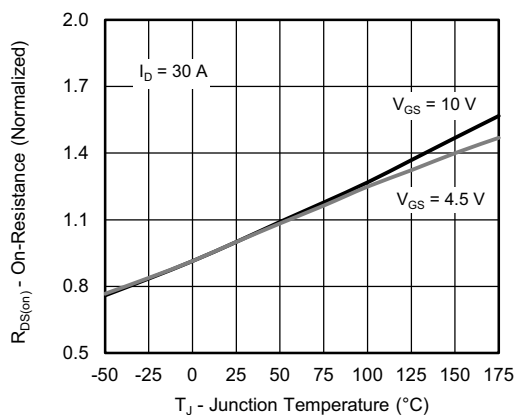
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %  
b. Guaranteed by design, not subject to production testing  
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

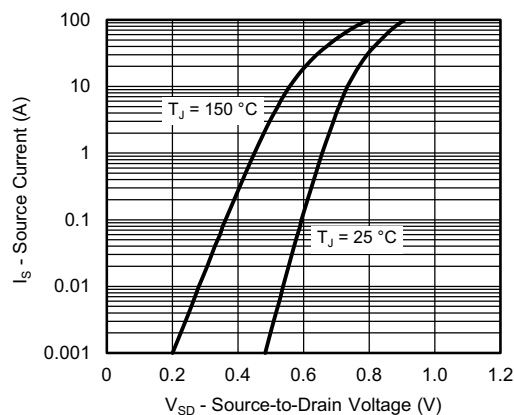
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**



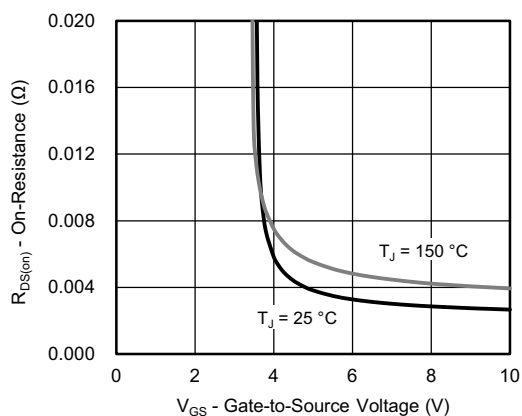
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



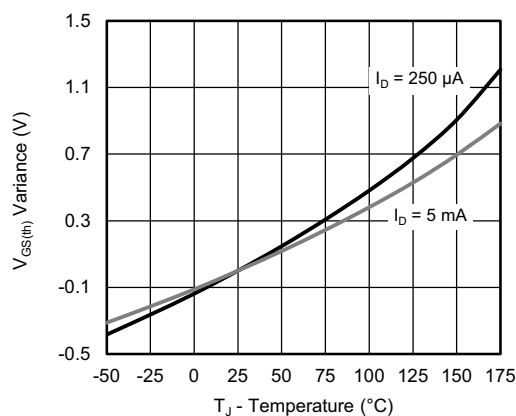
**On-Resistance vs. Junction Temperature**



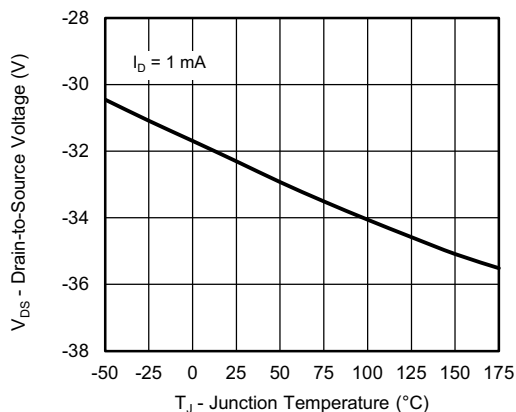
**Source Drain Diode Forward Voltage**



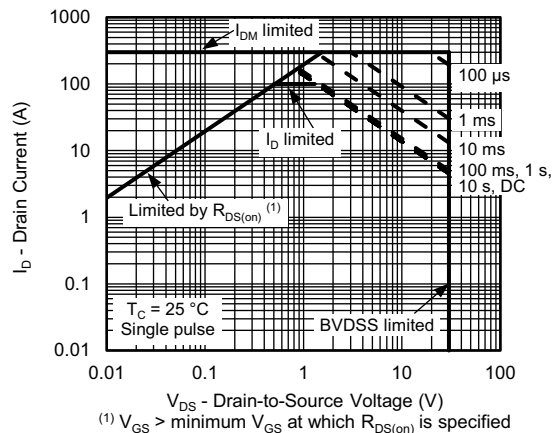
**On-Resistance vs. Gate-to-Source Voltage**



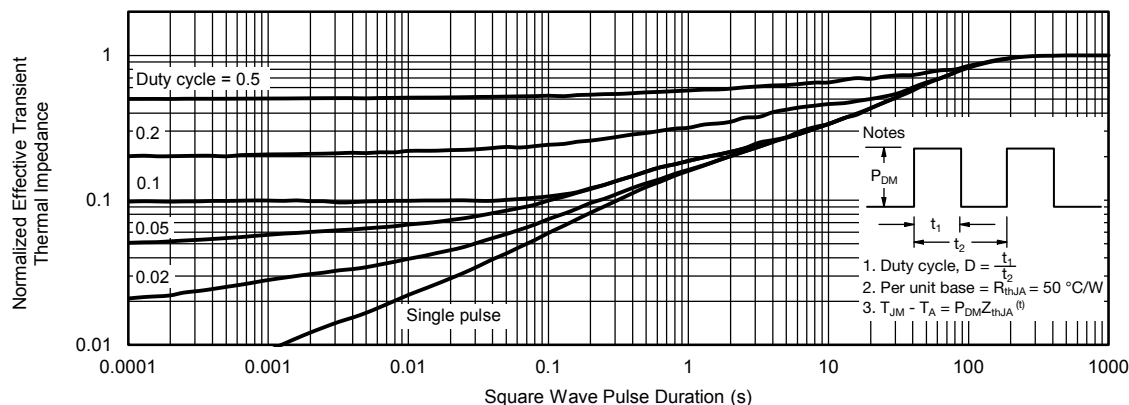
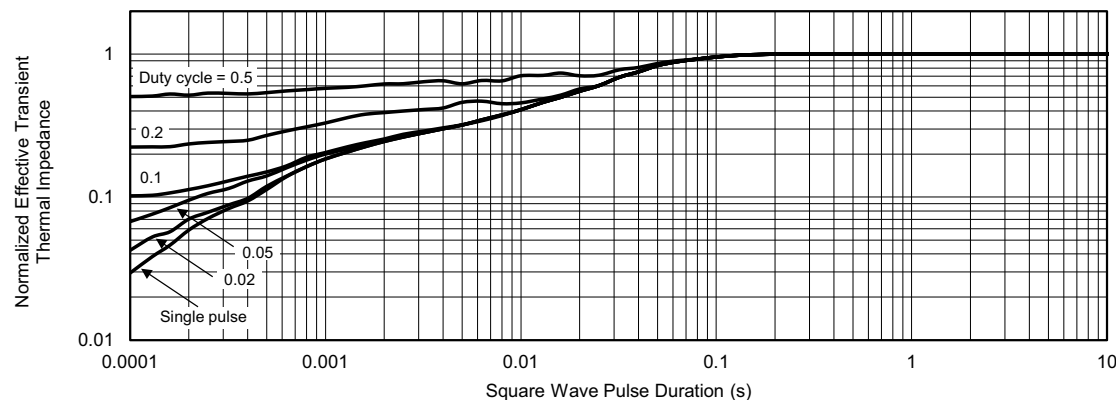
**Threshold Voltage**



**Drain Source Breakdown vs. Junction Temperature**



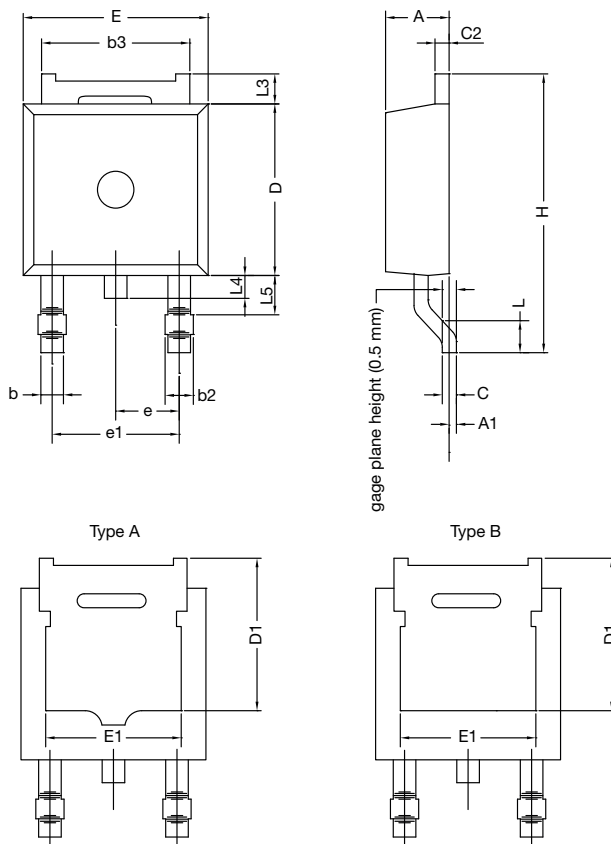
**Safe Operating Area**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to- Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?76011](http://www.vishay.com/ppg?76011).

## TO-252AA Case Outline



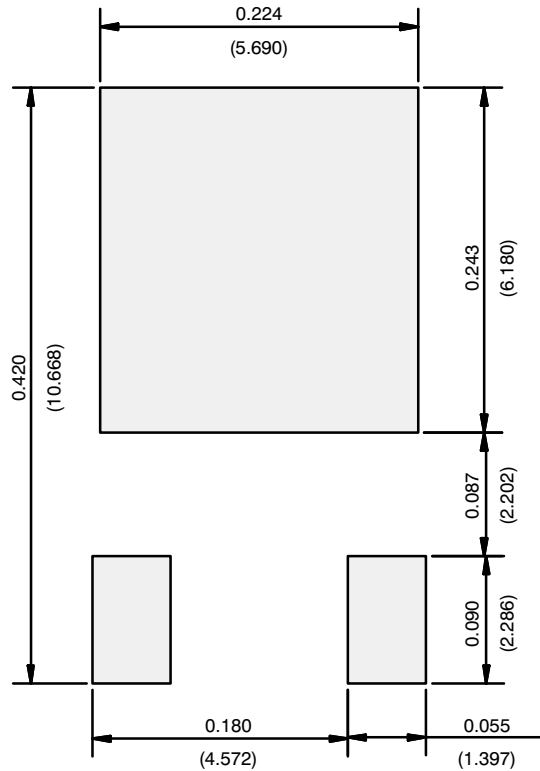
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T25-0122-Rev. C, 12-May-2025  
DWG: 6019

### Notes

- Dimension L3 is for reference only
- Dimension D1 and E1 on type A and B is the same

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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