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2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** 





MSL Level = N/A

#### **Features**

- Based on 3rd Overtone, Quartz Crystal Technology
- Ultra-low rms jitter; < 120fs typical @ 156.25MHz
- Lowest in-class power consumption (15mA max with LVDS)
- $\pm 25$ ppm max &  $\pm 30$ ppm max stability over -20°C to +70°C and -40°C to +85°C respectively
- 3.3V, 2.5V & 1.8V supply voltage options
- LVPECL, LVDS and HCSL differential output options
- Output enabled (Active High standard default)

#### **Key Electrical Specifications**

### **Applications**

- **Optical Transceivers**
- Optical Modules
- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range		100		200	MHz	
Standard Available Frequencies		100.00, 125.00, 148.50, 156.25 & 200.00		MHz	Contact Abracon for availability of frequencies not listed	
		2.97	3.3	3.63		Option "A"
Supply Voltage (Vdd) [Note 1]		2.37	2.5	2.62	V	Option "B"
		1.71	1.8	1.89		Option "C"
	LVPECL		30	50		@ 200MHz; @ Vdd=3.3V
Supply Current (Idd)	LVDS		10	15	mA	@ 200MHz; @ Vdd=3.3V
	HCSL		22	30		@ 200MHz; @ Vdd=3.3V
O 1 T 1 P		-20		70	°C	Option "D"
Operating Temperature Range		-40		85		Option "F"
Storage Temperature		-55		150	°C	
Frequency Accuracy (Initial Set-Tolerance, as received stand-alone measured frequency) at time of shipment (Pre-Reflow) @ +25°C		-10	<±5	+10	ppm	Relative to carrier frequency
Frequency Shift through Reflow		-2.00		+2.00	ppm	Relative to as received frequency
Frequency Stability over		-25		25		Option "D" (-20°C to +70°C)
Operating Temperature Range[Note 2]		-30		30	ppm	Option "F" (-40°C to +85°C)
First Year Aging		-3.00		+3.00	ppm	Maximum first year aging, ±2.00 ppm max. per year thereafter
Aging over 20 Year Product Life Note 3	3]	-15		+15	ppm	
All-Inclusive Frequency Accuracy (To	otal Stability)	-52		52		Option "D" (-20°C to +70°C)
over 20 Year Product Life [Notes 4]		-57		57	ppm	Option "F" (-40°C to +85°C)
	LVPECL		0.3	0.6		@ Vdd=3.3V, RL=50Ω
Rise (Tr) / Fall (Tf) Time 20% to 80% Vpeak to peak	LVDS		0.3	0.5	ns	@ Vdd=3.3V, RL=100Ω
2070 to 0070 v peak to peak	HCSL		0.3	0.6		@ Vdd=3.3V, RL=50Ω to GND
Duty Cycle		45		55	%	
Start-up Time			< 2	5	ms	



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ESD Sensitive (Pb)



2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

Parameters			Min.	Typ.	Max.	Unit	Notes	
	LVDECL	$V_{\mathrm{OH}}$	V <sub>dd</sub> -1.03		$V_{dd}$ -0.88		D 500 / W 20W	
	LVPECL	Vol	V <sub>dd</sub> -1.85		V <sub>dd</sub> -1.60		$R_L$ =50 $\Omega$ to $V_{dd}$ -2.0 $V$	
Differential	LVDC	V <sub>OH</sub>		1.40	1.60	V	D =1000 hotrroom both outputs	
Output High Voltage (VOH) Output Low Voltage (VOL)	LVDS	$V_{OL}$	0.90	1.10		V	$R_L=100\Omega$ between both outputs	
	HCSL	V <sub>OH</sub>	0.40	0.74	0.85		D =500 to around on each output	
	HCSL	Vol	-0.15	0.00	0.15		$R_L$ =50 $\Omega$ to ground on each output	
			0.50				LVPECL	
Output Voltage Swing			0.250	0.350	0.450	V	LVDS	
		0.50				HCSL		
Outrast Englis & Digital Control	1		0.7*(V <sub>dd</sub> )			V	Output Enable or No Connect	
Output Enable & Disable Contro	L				0.3*(V <sub>dd</sub> )	V	Output Disable (High Impedance)	
Output Enable Time				< 2.00	5.00	ms		
Output Disable Time					0.2	μs		
Output Disable Current Consumption				< 10	μΑ	$OE \le 0.3V$		
rms phase jitter (12kHz to 20MHz from Carrier)				< 200	500	fs	Vdd, RF output type and Carrier frequency dependent	
				<150	200	fs	@ 156.25MHz	

Note 1: Supply voltage (Vdd) = 1.8V option not available with LVPECL output.

Note 2: Relative to initial measured frequency @ +25°C, pre-reflow.

Note 3: Relative to post-reflow frequency.

Note 4: Includes post reflow frequency accuracy, temperature stability, load pulling, power supply variation, and 20-year aging.



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2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A





#### **Phase Noise Test Setup**

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Not omitted (Normalized in dBc/Hz)
- Specifed Spur Omission Function = Not enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

#### Typical Values measured at $25^{\circ}C \pm 3^{\circ}$

Frequency	y (MHz)	100.00MHz						156.2	5MHz		
$V_{\mathrm{DI}}$	)	1.8	BV		2.5V			3.3V		1.8V	2.5V
RF Ou	tput	LVDS	HCSL	LVDS	HCSL	LVPECL	LVDS	HCSL	LVPECL	LV	DS
rms Ph Jitter (1 12kHz-:		385.27	147.12	207.96	117.86	131.63	255.13	195.68	123.73	139.49	107.18
Phase	100Hz	-104.49	-86.91	-80.88	-75.50	-99.17	-87.89	-105.15	-102.40	-93.43	-93.21
Noise (dB <sub>C</sub> /H <sub>Z</sub> )	1KHz	-125.64	-120.54	-115.99	-115.89	-129.38	-120.80	-132.38	-132.55	-123.45	-125.31
	10KHz	-134.97	-144.63	-140.15	-147.34	-145.94	-143.61	-144.58	-146.61	-136.98	-139.61
	100KHz	-140.45	-152.42	-149.52	-457.05	-153.02	-146.87	-150.96	-152.79	-140.93	-149.12
	1MHz	-147.69	-155.94	-153.49	-153.53	-156.87	-148.30	-150.70	-156.98	-150.53	-154.70
	10MHz	-149.67	-157.06	-153.53	-159.42	-157.87	-153.04	-154.78	-158.59	-155.31	-156.40

Note 5: Guaranteed by characterization; rms Phase Jitter specifications are inclusive of any spurs

Note 6: Phase jitter measured with Keysight E5052B Signal Source Analyzer at 25°C±3°C



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2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** 

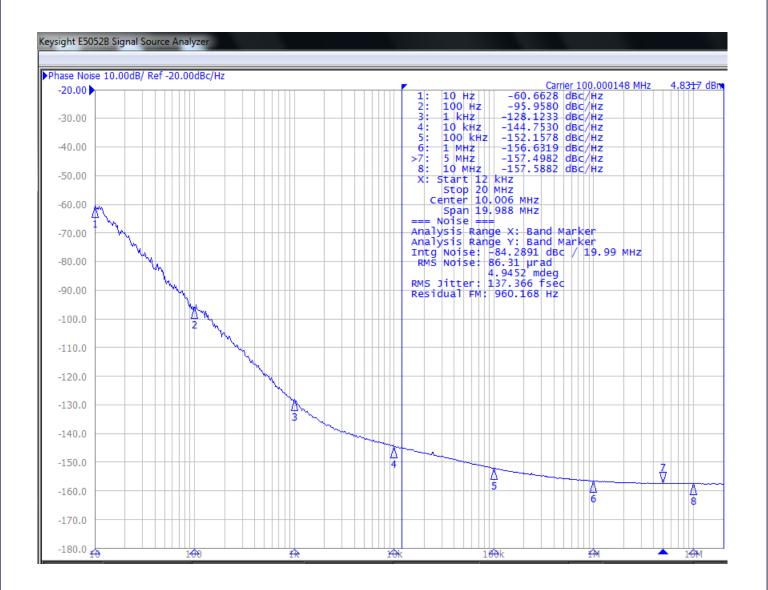
MSL Level = N/A





Representative Phase Noise Plots @ +25°C [Note 7]

**Frequency** = 100.00 MHzVdd = 2.50V**RF** Output = LVPECL rms Phase Jitter = 137 fs





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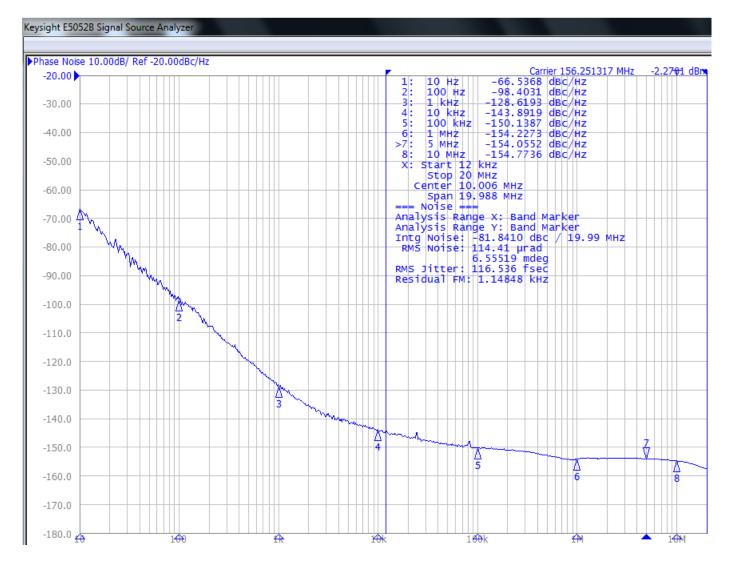
2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** 

ESD Sensitive (Pb)

MSL Level = N/A

**Frequency** = 156.2500 MHz

Vdd = 2.50V**RF** Output =LVDSrms Phase Jitter = 117 fs



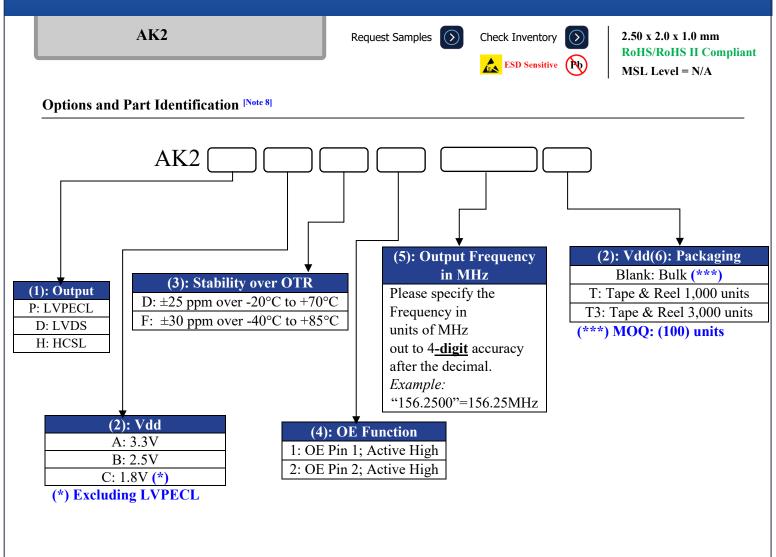
Note 7: Contact Abracon for phase noise plots at alternative supply voltage (V<sub>dd</sub>) & differential output formats



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# ClearClock<sup>TM</sup> Oscillator Family | Low Jitter | 2.5x2.0mm XO



#### Part Number Example

AK2PAF1-156.2500 [(100) units in Bulk]

AK2PAF1-156.2500T [(1k) units on Tape & Reel]

AK2PAF1-156.2500T3 [(3k) units on Tape & Reel]

Note 8: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal



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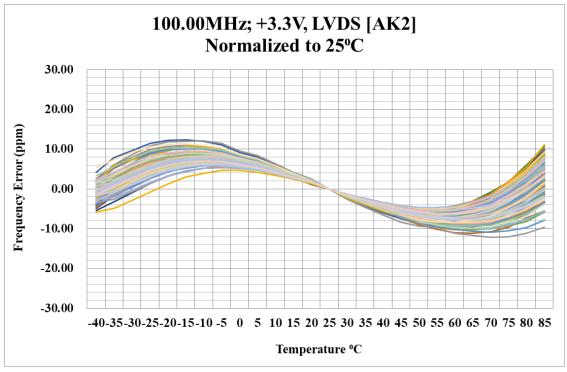
Check Inventory

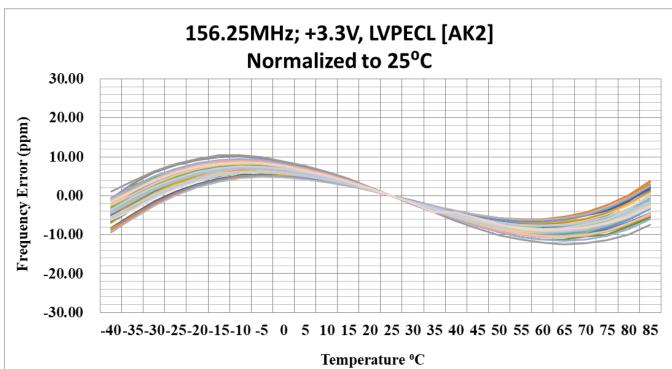
ESD Sensitive (Pb)



2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

#### **Typical Frequency vs. Temperature Characteristics**







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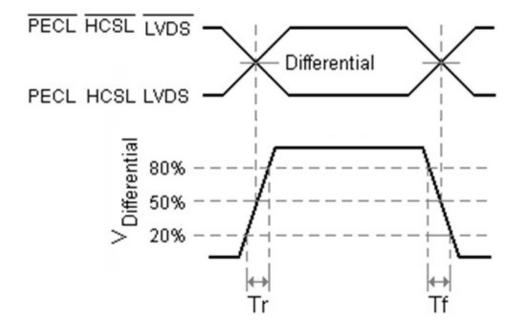
2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

ESD Sensitive (Pb)



#### **Differential Output Waveform**

#### LVPECL, LVDS and HCSL Output Waveforms





AK2

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Check Inventory



2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

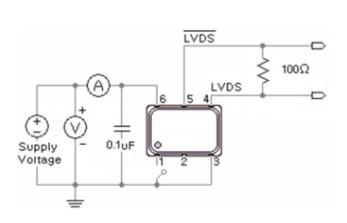
ESD Sensitive Pb

Recommended Test Circuit [Note 9]

### LVPECL

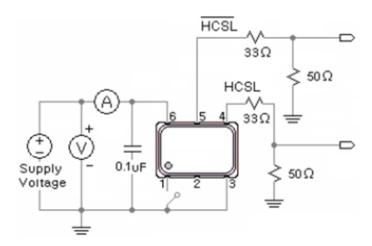
# $V_{\alpha i}$ R1 PECL $V_{dd}$ PECL R3 Supply Voltage R4

### LVDS



Vdd= 3.3V: R1=R3=127 $\Omega$ ; R2=R4=82.5 $\Omega$ Vdd= 2.5V: R1=R3=250 $\Omega$ ; R2=R4=62.5 $\Omega$ 

### HCSL



Note 9: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.



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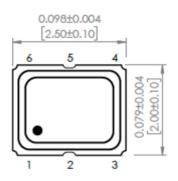


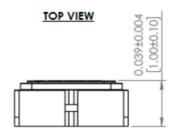
2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** 

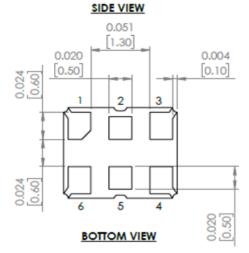
MSL Level = N/A

ESD Sensitive (Pb)

#### **Mechanical Dimensions**

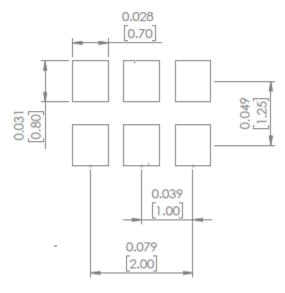






Dimensions: inches [mm]

#### Recommended Land Pattern



<u>Case 1</u> Pin #1=Output Enable/Disable Function where OE is Active HIGH			<u>Case 2</u> Pin #2=Output Enable/Disable Function <i>where</i> OE is Active HIGH		
Pin	Description	Pin	Description		
# 1	Output Enable = Logic High, "1", Vdd	# 1	No Connect		
# 1	Output Disable =		Output Enable =		
	Logic Low, "0", GND	# 2	Logic High, "1", Vdd		
# 2	#2 No Connect		Output Enable =		
# 2	No Connect		Logic Low, "0", GND		
# 3	GND	# 3	GND		
# 4	Output	# 4	Output		
# 5	Complementary output	# 5	Complementary output		
# 6	Supply Voltage (Vdd)	# 6	Supply Voltage (Vdd)		



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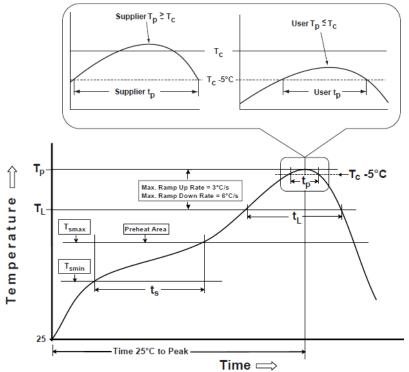
ESD Sensitive Pb



2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** 

MSL Level = N/A

#### **Reflow Profile [JEDEC J-STD-020]**



#### Table 1 **SnPb Eutectic Process** Classification Temperatures (Tc) Package Volume mm<sup>3</sup> Volume mm<sup>3</sup> Thickness <350 <u>></u>350 235 °C 220 °C 220 °C 220 °C ≥2.5 mm

Tab	le 2	
DI-		B

Pb-Free Process Classification Temperatures (Tc)					
Package Thickness	Volume mm³ <350	Volume mm <sup>3</sup> 350-2000	Volume mm³ >2000		
<1.6 mm	260 °C	260 °C	260 °C		
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C		
>2.5 mm	250 °C	245 °C	245 °C		

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T <sub>smin</sub> )	100°C	150°C
Temperature maximum (T <sub>smax</sub> )	150°C	200°C
Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T <sub>smax</sub> to T <sub>P</sub> )	3°C/sec. max	3°C/sec. max
Liquidous temperature (T <sub>L</sub> )	183°C	217°C
Time at liquidous (t <sub>L</sub> )	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T <sub>P</sub> )*	see Table 1	see Table 2
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>C</sub> )	20 sec.	30 sec.
Ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

<sup>\*</sup>Tolerance for peak profile temperature (T<sub>P</sub>) is defined as a supplier minimum and a user maximum.



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<sup>\*\*</sup>Tolerance for time at peak profile temperature  $(t_p)$  is defined as supplier minimum and a user maximum.

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ESD Sensitive (Pb)

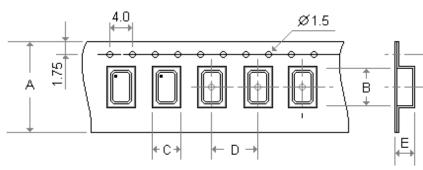


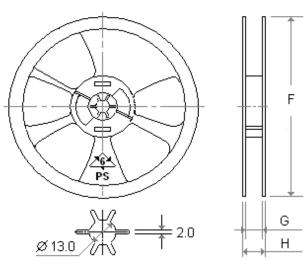
2.50 x 2.0 x 1.0 mm **RoHS/RoHS II Compliant** MSL Level = N/A

#### **Packaging**

Blank = Bulk (MOQ=100 units) T = Tape & Reel 1,000 units/reel T3= Tape & Reel 3,000 units/reel

#### Feeding (PULL) Direction →





Dimensions: (Unit:mm)

Α	В	С	D	Е
8.0	2.7	2.2	4.0	1.2
F	G	Н		

F	G	Н
180.0	9.0	12.0

- (10) sprocket hold pitch cumulative tolerance is  $\pm 0.10$  mm
- "E" measured from a place on the inside bottom of the pocket to the top surface of the carrier

Dimensions: mm

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