TPS780xx 150-mA Low-Dropout Regulator, Ultralow-Power, I_Q 500 nA With Pin-Selectable, Dual-Level Output Voltage

1 Features

- Low I_Q: 500 nA
- 150-mA, Low-Dropout Regulator With Pin-Selectable Dual Voltage Level Output
- Low Dropout: 200 mV at 150 mA
- 3% Accuracy Over Load, Line, and Temperature
- Available in Dual-Level, Fixed-Output Voltages From 1.5 V to 4.2 V
- Available in an Adjustable Version from 1.22 V to 5.25 V or a Dual-Level Output Version
- V_{SET} Pin Toggles Output Voltage Between Two Factory-Programmed Voltage Levels
- Stable with a 1.0-µF Ceramic Capacitor
- Thermal Shutdown and Overcurrent Protection
- CMOS Logic Level-Compatible Enable Pin
- Available in DDC (TSOT23-5) or DRV (2-mm × 2-mm SON-6) Package Options

2 Applications

- TI MSP430™ Attach Applications
- Power Rails With Programming Mode
- Dual Voltage Levels for Power-Saving Mode
- Wireless Handsets, Smart Phones, PDAs, MP3 Players, and Other Battery-Operated Handheld Products

3 Description

The TPS780 family of low-dropout (LDO) regulators offer the benefits of ultralow power, miniaturized packaging, and selectable dual-level output voltage levels with the V_{SET} pin.

The ultralow-power and dynamic voltage scaling (DVS) capability which provides dual-level output voltages let designers customize power consumption for specific applications. Designers can now shift to a lower voltage level in a battery-powered design when the microprocessor is in sleep mode, further reducing overall system power consumption. The two voltage levels are preset at the factory and are stored using EPROM and are available on fixed output voltage devices.

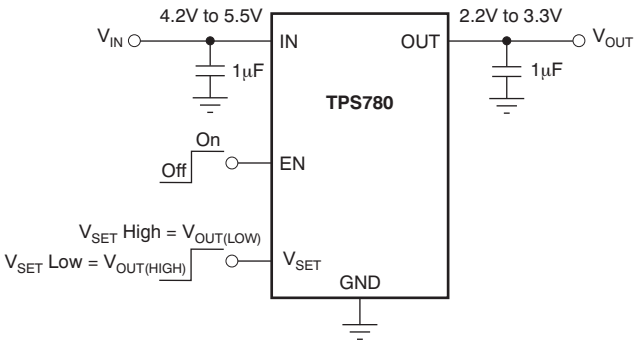
The TPS780 series of LDOs are designed to be compatible with the TI MSP430 and other similar products. The enable pin is compatible with standard CMOS logic. The TPS780 series also come with thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to 125°C. For more cost-sensitive applications requiring a dual-level voltage option and only *on par* I_Q, consider the TPS781 series, with an I_Q of 1.0 µA and dynamic voltage scaling.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS780xx	SOT (5)	2.90 mm x 1.60 mm
	SON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2012) to Revision E — **Page**

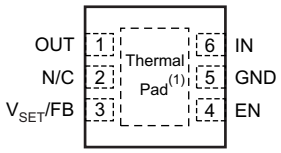
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Dissipation Ratings* table; see *Thermal Information* ... 4
- Changed parametric symbol for line and load regulation ... 5

Changes from Revision C (May 2008) to Revision D — **Page**

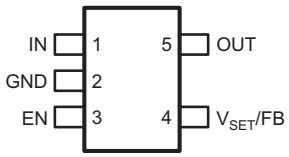
- Updated Figure 47 and Figure 48 ... 12

5 Pin Configuration and Functions

SON
6 Pins
Top View



SOT
5 Pins
Top View



(1) It is recommended that the SON package thermal pad be connected to ground.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SON	SOT		
OUT	1	5	O	Regulated output voltage pin. A small (1-µF) ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* for more details.
N/C	2	—	—	Not connected.
V_{SET}/FB	3	4	I	Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions. Drive the select pin (V_{SET}) below 0.4 V to select preset output voltage high. Drive the V_{SET} pin over 1.2 V to select preset output voltage low.
EN	4	3	I	Enable pin. Drive this pin over 1.2 V to turn on the regulator. Drive this pin below 0.4 V to put the regulator into shutdown mode, reducing operating current to 18 nA typical.
GND	5	2	—	Ground pin. Tie all ground pins to ground for proper operation.
IN	6	1	I	Input pin. A small capacitor is needed from this pin to ground to assure stability. A typical input capacitor is 1.0 µF. Tie back both input and output capacitor ground to the IC ground, with no significant impedance between them.
Thermal pad	—	—	—	(SON package only) Connect the thermal pad to ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	+6.0	V
	V_{EN} and V_{VSET}	–0.3	V_{IN} + 0.3 (2)	
	V_{OUT}	–0.3	V_{IN} + 0.3	
Current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Total continuous power dissipation, P_{DISS}		See *Thermal Information*		
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{EN} and V_{VSET} absolute maximum rating are V_{IN} + 0.3V or +6.0V, whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.2		5.5	V
V_{OUT}	Output voltage	1.8		4.2	V
V_{EN}	Enable voltage	0		V_{IN}	V
I_{OUT}	Output current	0		150	mA
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS780xx		UNIT
		DDC	DRV	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.0	65.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.1	87.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	35.4	
ψ_{JT}	Junction-to-top characterization parameter	0.9	1.7	
ψ_{JB}	Junction-to-board characterization parameter	34.1	35.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

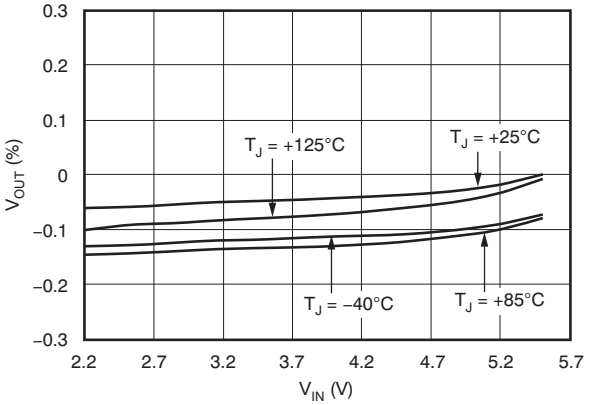
Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{VSET} = V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, fixed or adjustable, unless otherwise noted. Typical values at T_J = 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT} (1)	DC output accuracy	Nominal	T_J = 25°C, V_{SET} = high/low		–2%	±1%	+2%	
		Over V_{IN}, I_{OUT}, temperature	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 150 mA, V_{SET} = high/low		–3.0%	±2.0%	+3.0%	
V_{FB}	Internal reference (2) (adjustable version only)		T_J = 25°C, V_{IN} = 4.0 V, I_{OUT} = 75 mA			1.216		V
V_{OUT_RANGE}	Output voltage range (3) (4) (adjustable version only)		V_{IN} = 5.5 V, I_{OUT} = 100 µA (2)		V_{FB}	5.25		V
$\Delta V_{OUT(\Delta VIN)}$	Line regulation		$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 5 mA		–1%		+1%	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		0 mA ≤ I_{OUT} ≤ 150 mA		–2%		+2%	
V_{DO}	Dropout voltage (5)		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 150 mA				250	mV
V_n	Output noise voltage		BW = 100 Hz to 100 kHz, V_{IN} = 2.2 V, V_{OUT} = 1.2 V, I_{OUT} = 1 mA			86		μV_{RMS}
V_{HI}	V_{SET} high (output $V_{OUT(LO)}$ selected), or EN high (enabled)				1.2		V_{IN}	V
V_{LO}	V_{SET} low (output $V_{OUT(HI)}$ selected), or EN low (disabled)				0		0.4	V
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(nom)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0 mA (6)			420	800	nA
			I_{OUT} = 150 mA			5		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4 V, 2.2 V ≤ V_{IN} < 5.5 V, T_J = –40°C to 100°C			18	130	nA
I_{VSET}	V_{SET} pin current		V_{EN} = V_{VSET} = 5.5 V				70	nA
I_{EN}	EN pin current		V_{EN} = V_{VSET} = 5.5 V				40	nA
I_{FB}	FB pin current (7) (Adjustable version only)		V_{IN} = 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 100 µA				10	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 150 mA	f = 10 Hz		40		dB
				f = 100 Hz		20		
				f = 1kHz		15		
$t_{TR(H\rightarrow L)}$	V_{OUT} transition time (high-to-low) V_{OUT} = 97% × $V_{OUT(HI)}$		V_{OUT_LOW} = 2.2 V, $V_{OUT(HI)}$ = 3.3 V, I_{OUT} = 10 mA			800		µs
$t_{TR(L\rightarrow H)}$	V_{OUT} transition time (low-to-high) V_{OUT} = 97% × $V_{OUT(LO)}$		V_{OUT_HIGH} = 3.3 V, $V_{OUT(LO)}$ = 2.2 V, I_{OUT} = 10 mA			800		µs
t_{STR}	Start-up time (8)		C_{OUT} = 1.0 µF, V_{OUT} = 10% $V_{OUT(nom)}$ to V_{OUT} = 90% $V_{OUT(nom)}$			500		µs
t_{SHDN}	Shutdown time (9)		I_{OUT} = 150 mA, C_{OUT} = 1.0 µF, V_{OUT} = 2.8 V, V_{OUT} = 90% $V_{OUT(nom)}$ to V_{OUT} = 10% $V_{OUT(nom)}$			500 (10)		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			160		°C
			Reset, temperature decreasing			140		°C
T_J	Operating junction temperature				–40		125	°C

(1) The output voltage for V_{SET} = low/high is programmed at the factory.
(2) Adjustable version only.
(3) No V_{SET} pin on the adjustable version.
(4) No dynamic voltage scaling on the adjustable version.
(5) V_{DO} is not measured for devices with $V_{OUT(nom)}$ < 2.3 V because minimum V_{IN} = 2.2 V.
(6) I_{GND} = 800 nA (max) up to 100°C.
(7) The TPS78001 FB pin is tied to V_{OUT}. Adjustable version only.
(8) Time from V_{EN} = 1.2 V to V_{OUT} = 90% ($V_{OUT(nom)}$).
(9) Time from V_{EN} = 0.4 V to V_{OUT} = 10% ($V_{OUT(nom)}$).
(10) See *Shutdown* for more details.

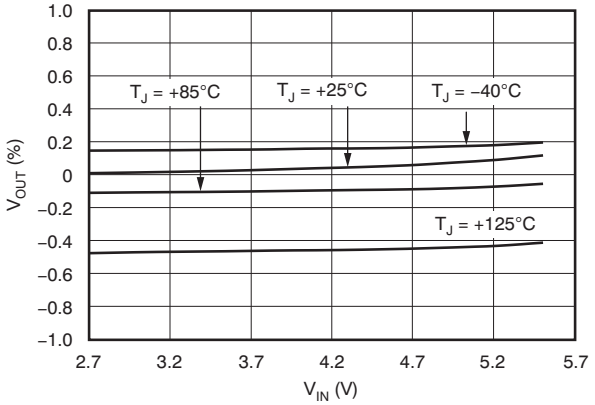
6.6 Typical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



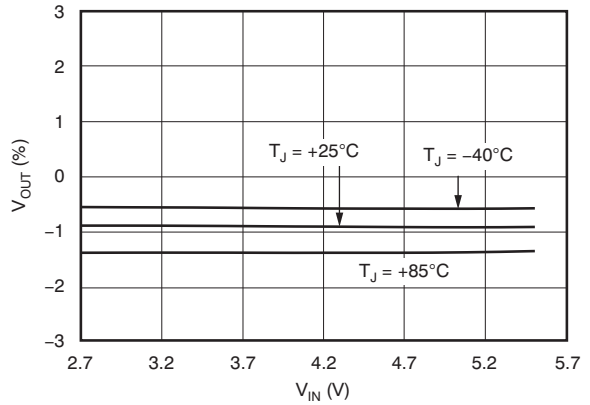
I_{OUT} = 5 mA $V_{OUT(nom)}$ = 1.22 V

Figure 1. TPS78001 Line Regulation



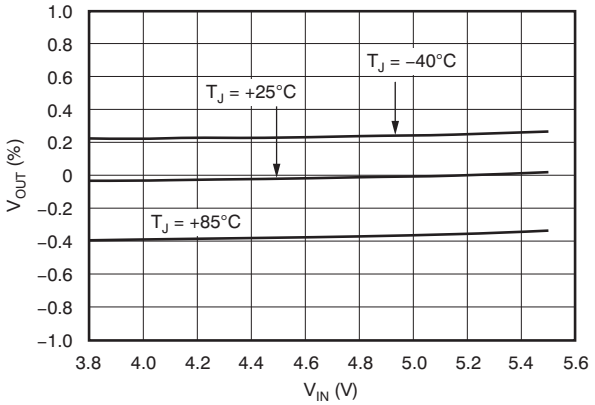
I_{OUT} = 5 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 2. TPS780330220 Line Regulation



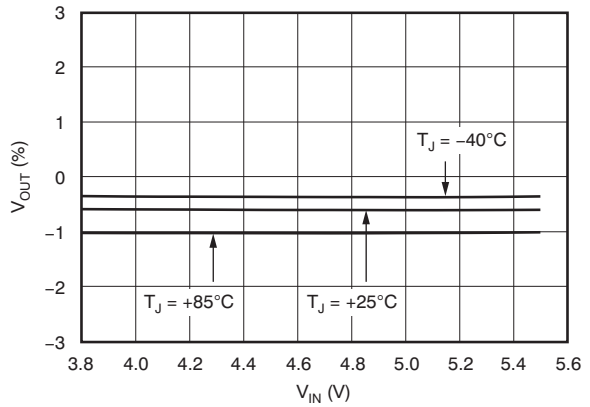
I_{OUT} = 150 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 3. TPS780330220 Line Regulation



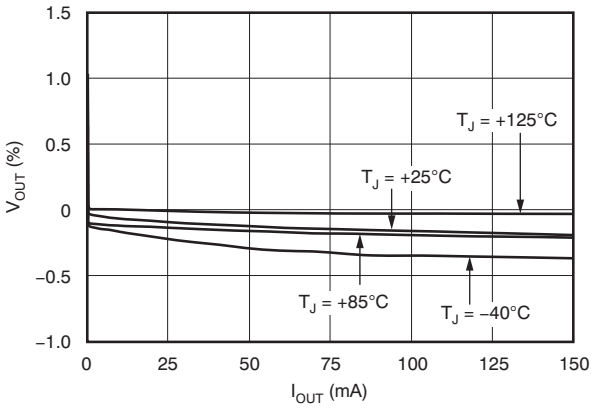
I_{OUT} = 5 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 4. TPS780330220 Line Regulation



I_{OUT} = 150 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 5. TPS780330220 Line Regulation

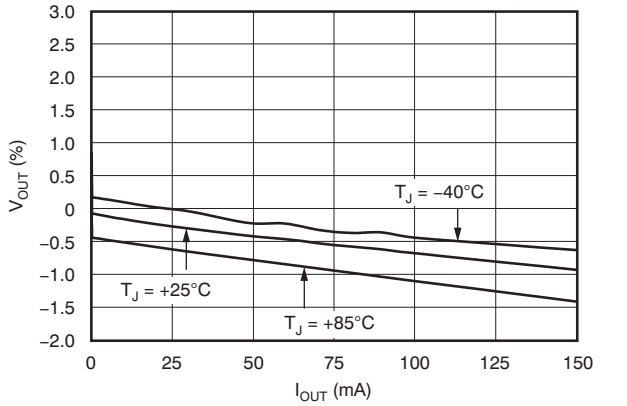


$V_{OUT(nom)}$ = 3.3 V

Figure 6. TPS78001 Load Regulation

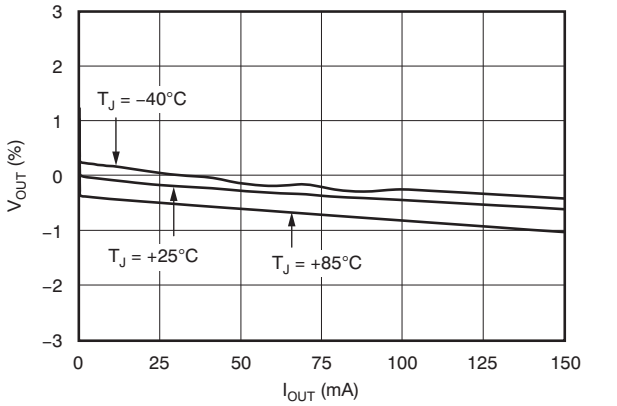
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



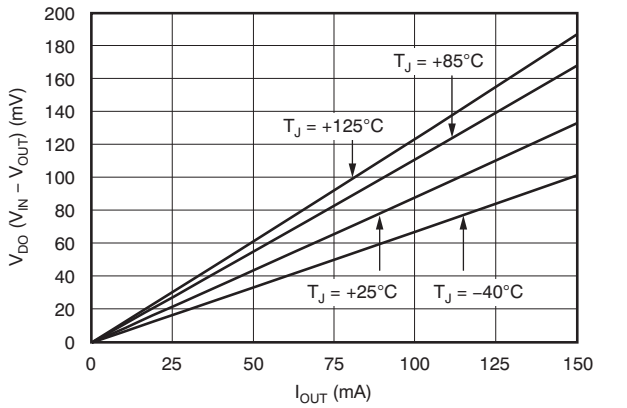
V_{VSET} = 1.2 V V_{IN} = 2.7 V $V_{OUT(nom)}$ = 2.2 V

Figure 7. TPS780330220 Load Regulation



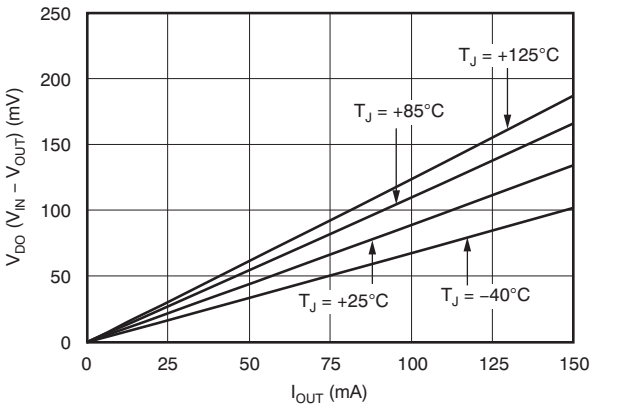
V_{VSET} = 0.4 V V_{IN} = 3.8 V $V_{OUT(nom)}$ = 3.3 V

Figure 8. TPS780330220 Load Regulation



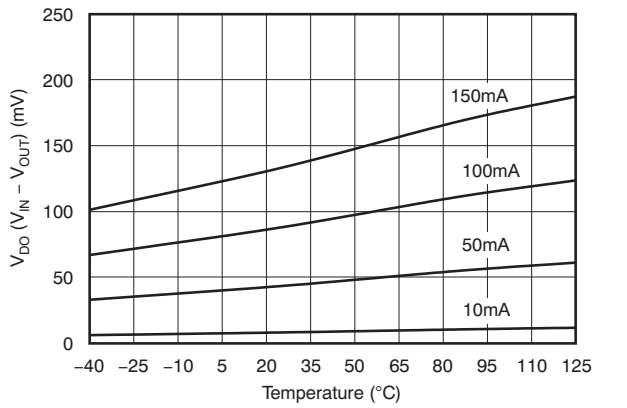
$V_{OUT(nom)}$ = 3.3 V V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 9. TPS78001 Dropout Voltage vs Output Current



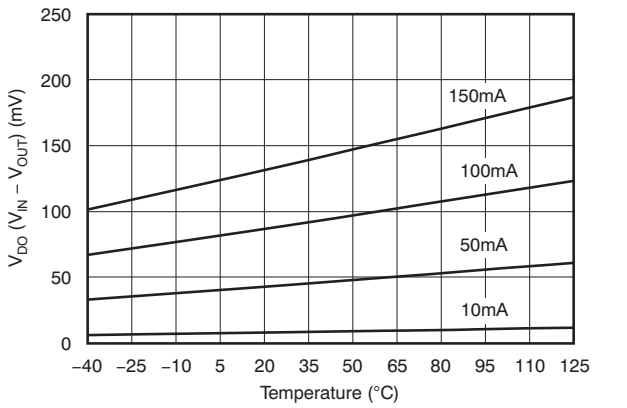
V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 10. TPS780330220 Dropout Voltage vs Output Current



$V_{OUT(nom)}$ = 3.3 V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 11. TPS78001 Dropout Voltage vs Temperature

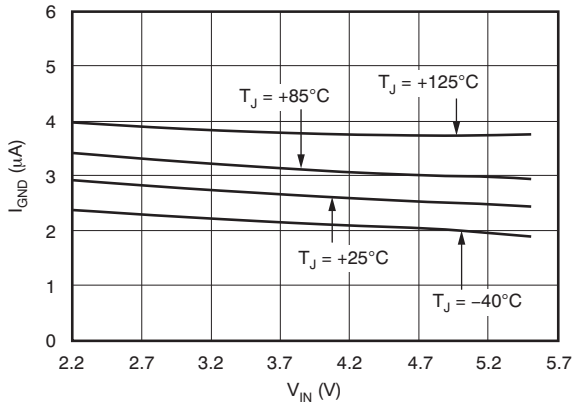


V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V V_{IN} = 0.95 × $V_{OUT(nom)}$

Figure 12. TPS780330220 Dropout Voltage vs Temperature

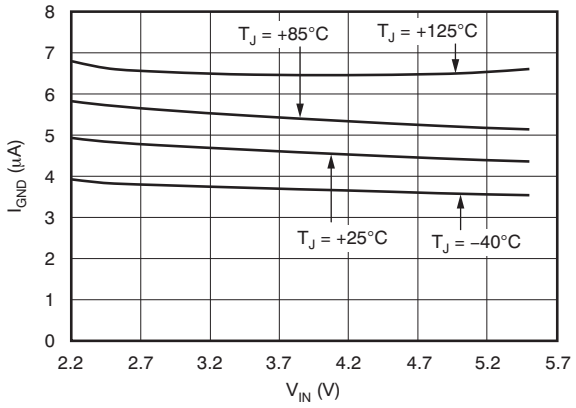
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



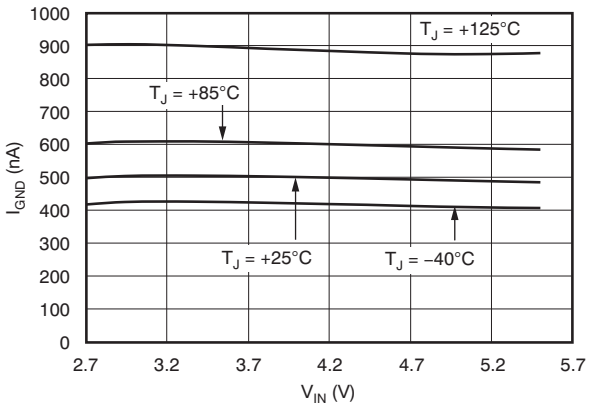
I_{OUT} = 50 mA $V_{OUT(nom)}$ = 1.22 V

Figure 13. TPS78001 Ground Pin Current vs Input Voltage



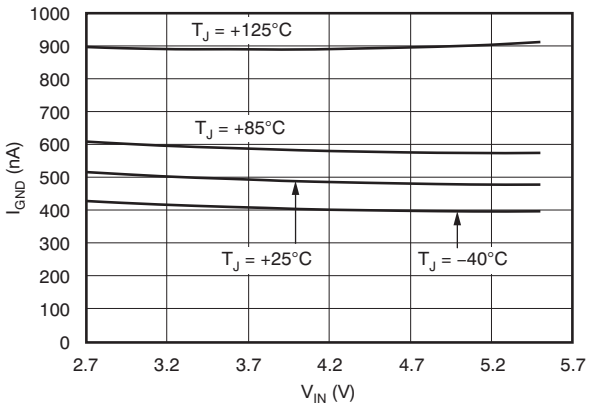
I_{OUT} = 150 mA $V_{OUT(nom)}$ = 1.22 V

Figure 14. TPS78001 Ground Pin Current vs Input Voltage



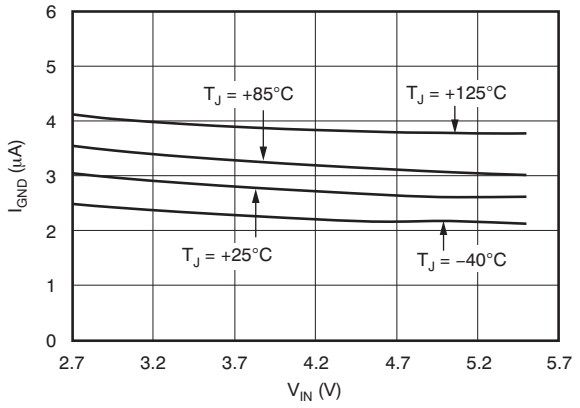
I_{OUT} = 0 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 15. TPS780330220 Ground Pin Current vs Input Voltage



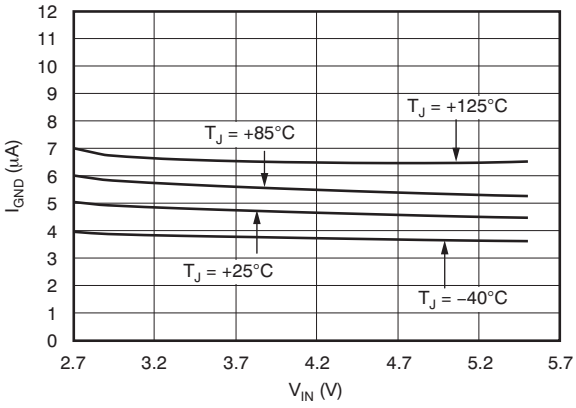
I_{OUT} = 1 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 16. TPS780330220 Ground Pin Current vs Input Voltage



I_{OUT} = 50 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 17. TPS780330220 Ground Pin Current vs Input Voltage

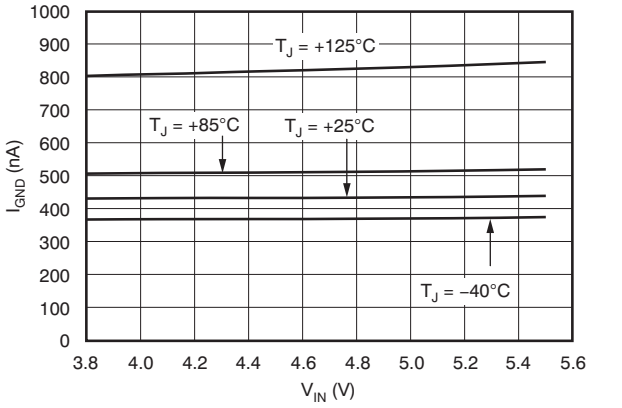


I_{OUT} = 150 mA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 18. TPS780330220 Ground Pin Current vs Input Voltage

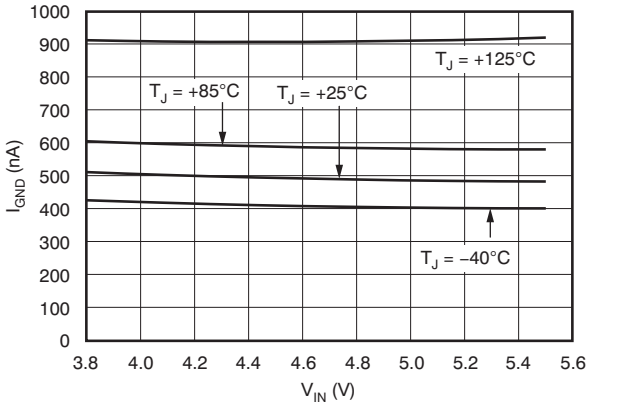
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



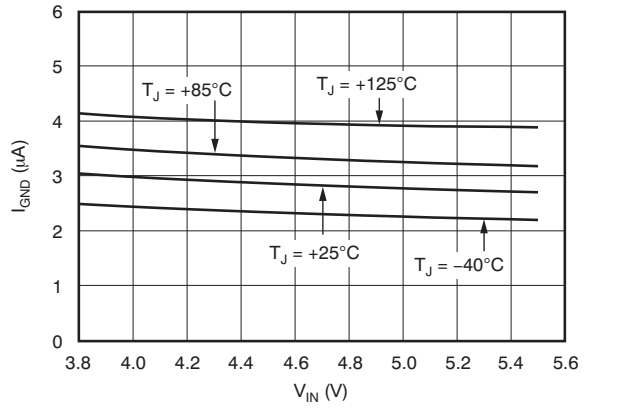
I_{OUT} = 0 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 19. TPS780330220 Ground Pin Current vs Input Voltage



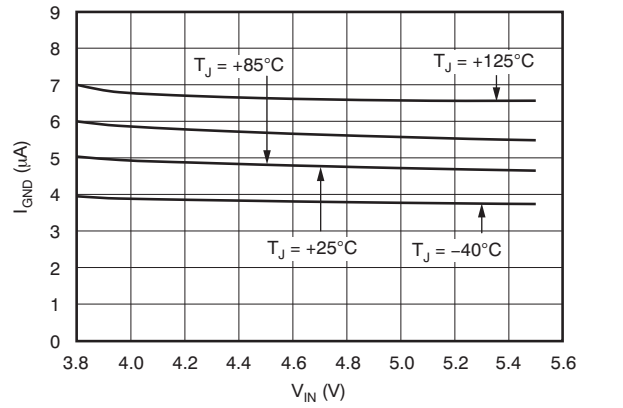
I_{OUT} = 1 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 20. TPS780330220 Ground Pin Current vs Input Voltage



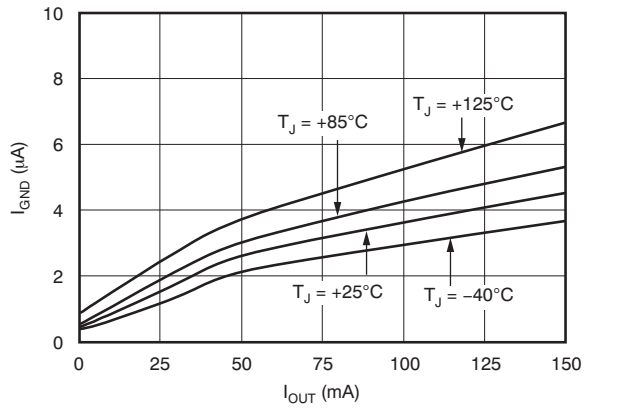
I_{OUT} = 50 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 21. TPS780330220 Ground Pin Current vs Input Voltage



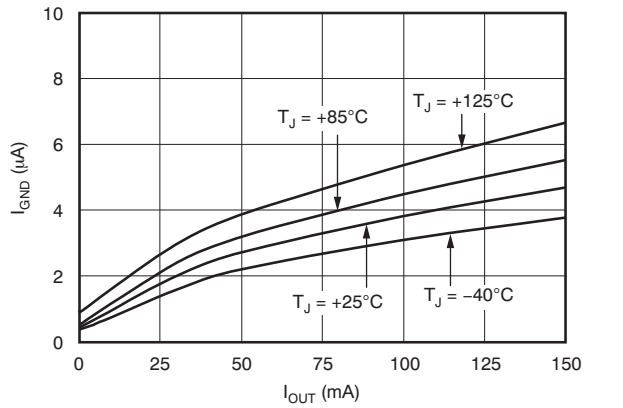
I_{OUT} = 150 mA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 22. TPS780330220 Ground Pin Current vs Input Voltage



V_{VSET} = 1.2 V V_{IN} = 5.5 V $V_{OUT(nom)}$ = 2.2 V

Figure 23. TPS780330220 Ground Pin Current vs Output Current

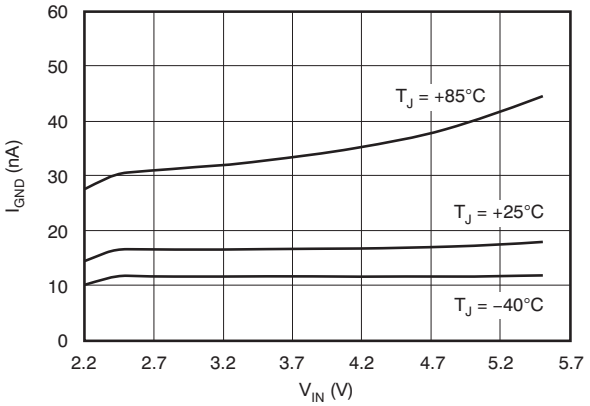


V_{VSET} = 0.4 V V_{IN} = 5.5 V $V_{OUT(nom)}$ = 3.3 V

Figure 24. TPS780330220 Ground Pin Current vs Output Current

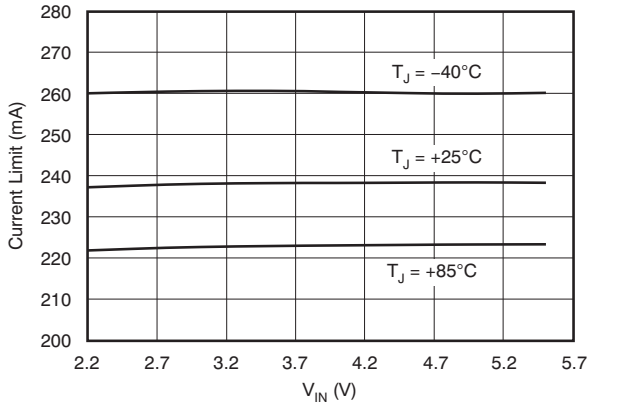
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



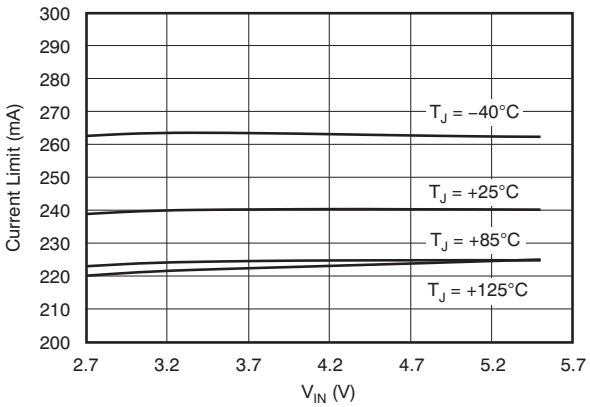
I_{OUT} = 0 mA V_{VSET} = 0.4 V

Figure 25. TPS78001 Shutdown Current vs Input Voltage



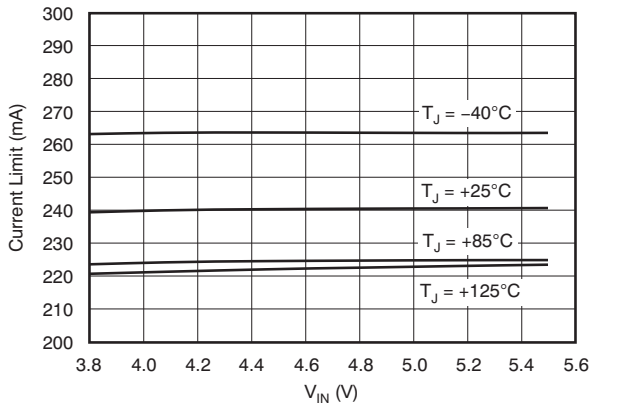
V_{OUT} = 90% $V_{OUT(nom)}$ $V_{OUT(nom)}$ = 1.22 V

Figure 26. TPS78001 Current Limit vs Input Voltage



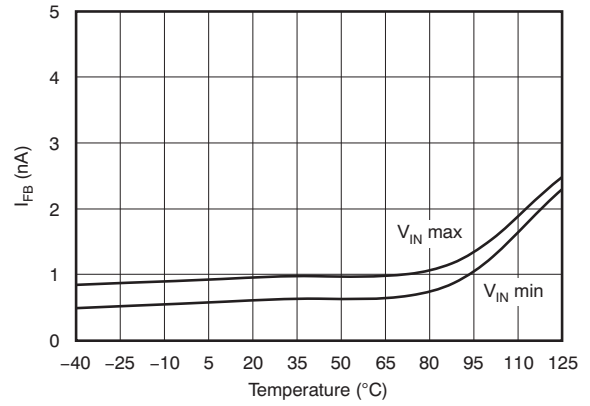
V_{VSET} = 1.2 V V_{OUT} = 95% $V_{OUT(nom)}$ $V_{OUT(nom)}$ = 2.2 V

Figure 27. TPS780330220 Current Limit vs Input Voltage



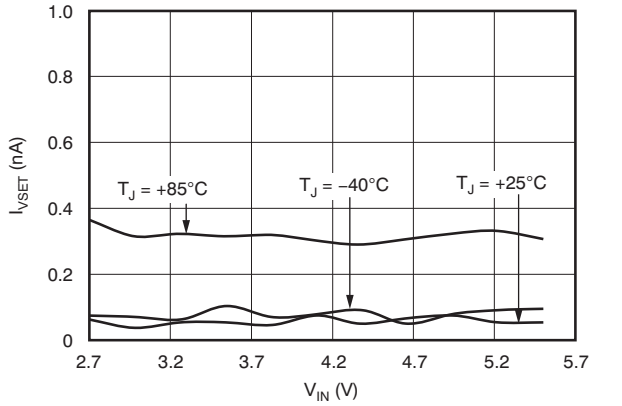
V_{VSET} = 0.4 V V_{OUT} = 95% $V_{OUT(nom)}$ $V_{OUT(nom)}$ = 3.3 V

Figure 28. TPS780330220 Current Limit vs Input Voltage



I_{OUT} = 0 mA $V_{OUT(nom)}$ = 1.22 V

Figure 29. TPS78001 Feedback Pin Current vs Temperature

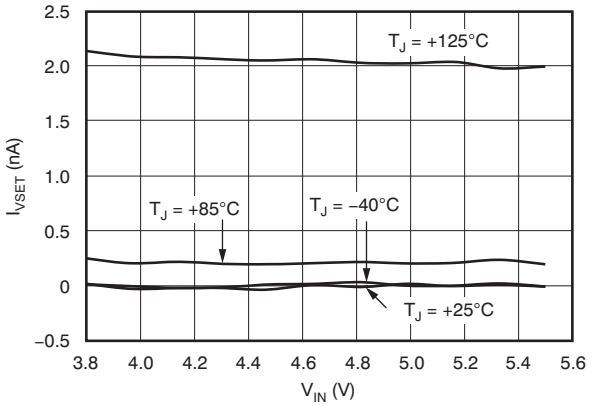


I_{OUT} = 100 µA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 30. TPS780330220 V_{SET} Pin Current vs Input Voltage

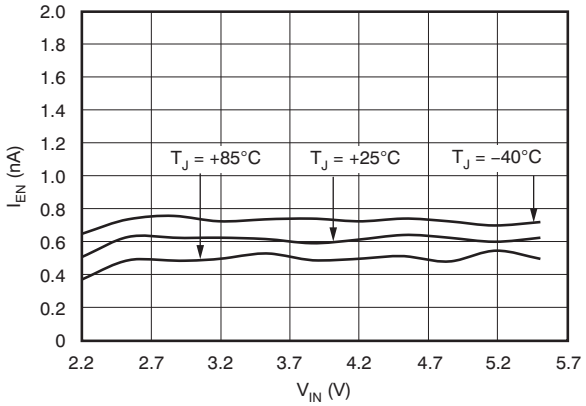
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



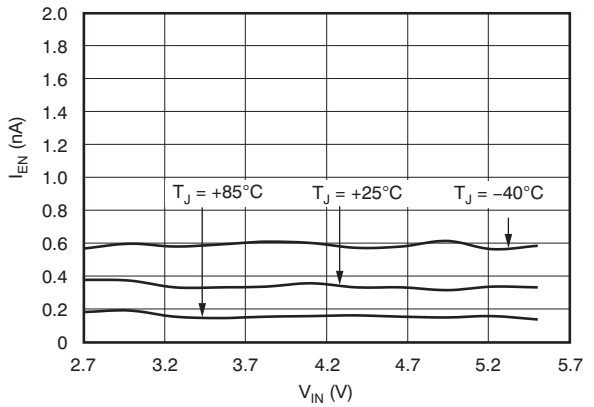
I_{OUT} = 100 µA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 31. TPS780330220 V_{SET} Pin Current vs Input Voltage



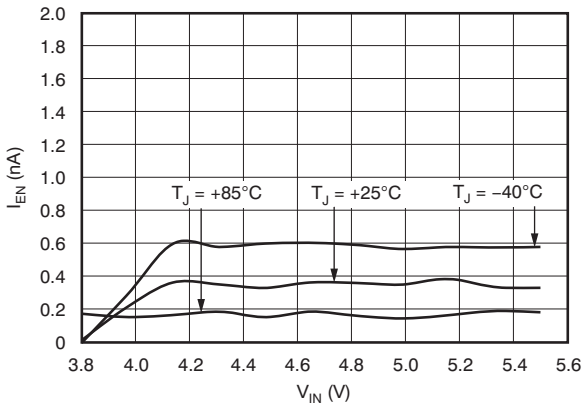
I_{OUT} = 1 mA $V_{OUT(nom)}$ = 1.22 V

Figure 32. TPS78001 Enable Pin Current vs Input Voltage



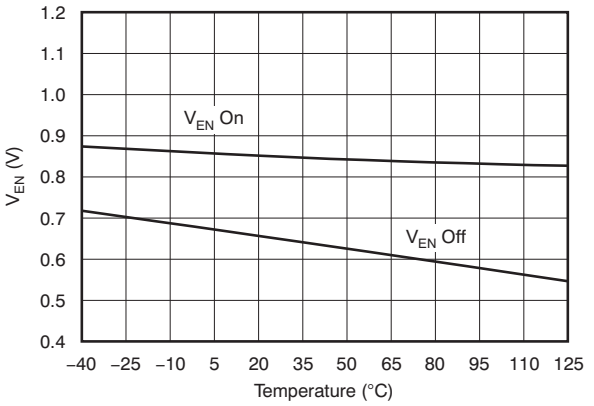
I_{OUT} = 100 µA V_{VSET} = 1.2 V $V_{OUT(nom)}$ = 2.2 V

Figure 33. TPS780330220 Enable Pin Current vs Input Voltage



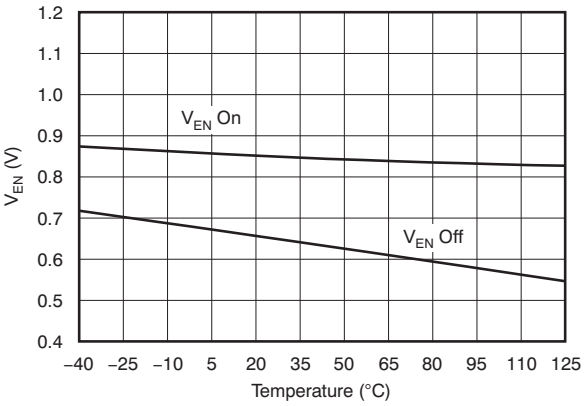
I_{OUT} = 100 µA V_{VSET} = 0.4 V $V_{OUT(nom)}$ = 3.3 V

Figure 34. TPS780330220 Enable Pin Current vs Input Voltage



I_{OUT} = 1 mA

Figure 35. TPS78001 Enable Pin Hysteresis vs Temperature

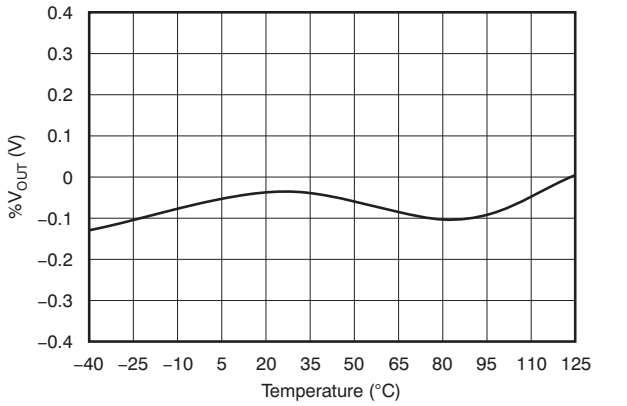


I_{OUT} = 1 mA

Figure 36. TPS780330220 Enable Pin Hysteresis vs Temperature

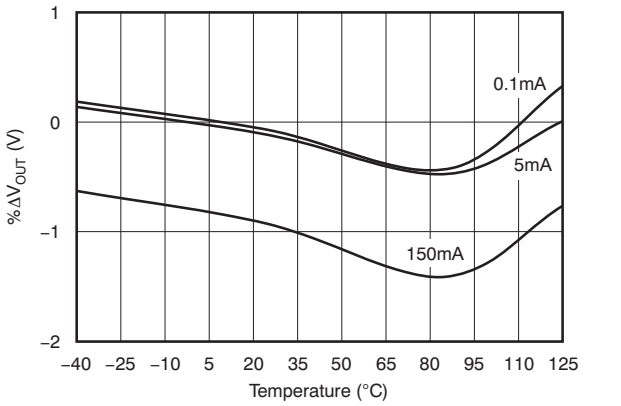
Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.



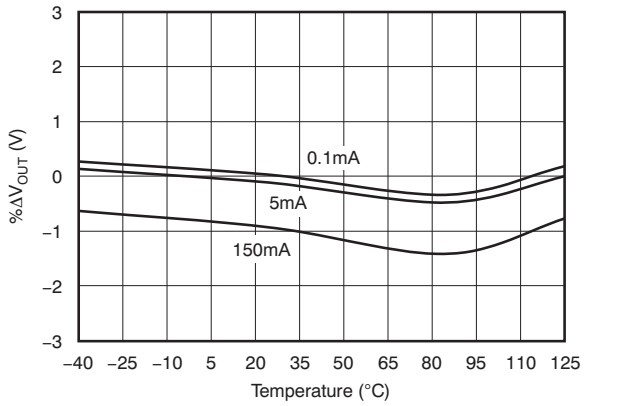
I_{OUT} = 1 mA V_{IN} = 3.8 V $V_{OUT(nom)}$ = 3.3 V

Figure 37. TPS78001 %ΔV$_{OUT}$ vs Temperature



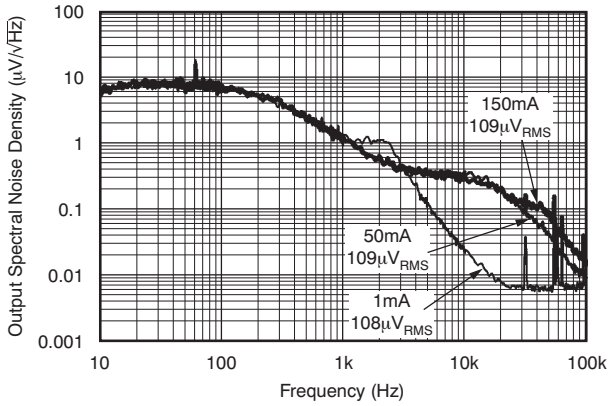
V_{VSET} = 1.2 V V_{IN} = 2.7 V $V_{OUT(nom)}$ = 2.2 V

Figure 38. TPS780330220 %ΔV$_{OUT}$ vs Temperature



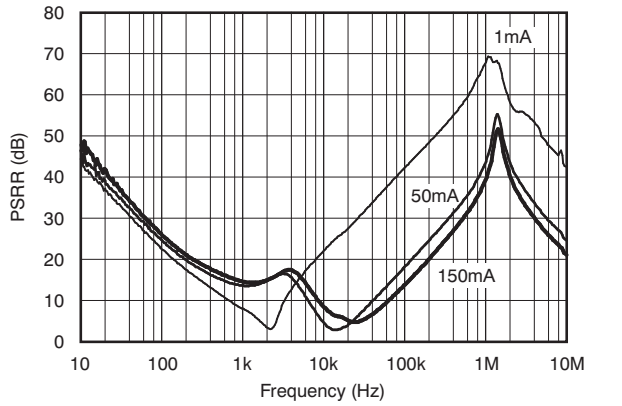
V_{VSET} = 0.4 V V_{IN} = 3.8 V $V_{OUT(nom)}$ = 3.3 V

Figure 39. TPS780330220 %ΔV$_{OUT}$ vs Temperature



C_{IN} = 1 µF C_{OUT} = 2.2 µF V_{VSET} = 1.2 V
V_{IN} = 2.7 V

Figure 40. TPS780330220 Output Spectral Noise Density vs Frequency



V_{IN} = 2.7 V V_{OUT} = 1.2 V C_{OUT} = 2.2 µF

Figure 41. TPS78001 Ripple Rejection vs Frequency

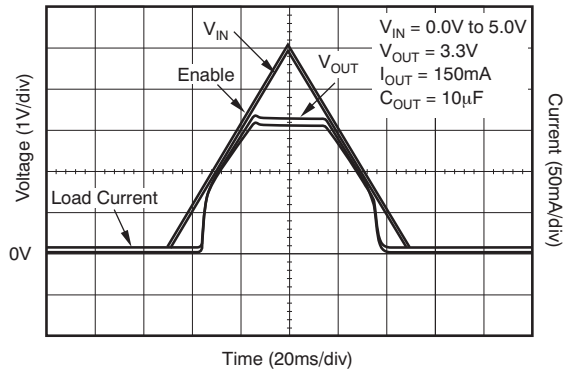


Figure 42. TPS780330220 Input Voltage Ramp vs Output Voltage

Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.

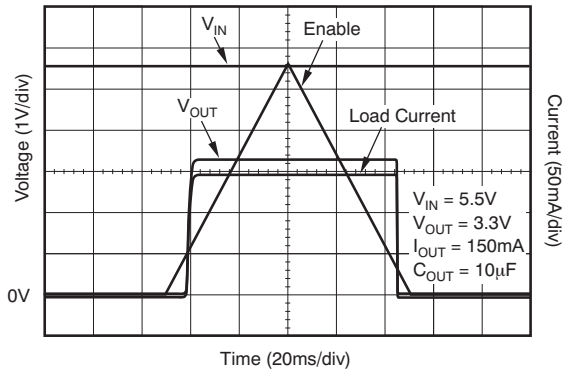


Figure 43. TPS780330220 Output Voltage vs Enable (Slow Ramp)

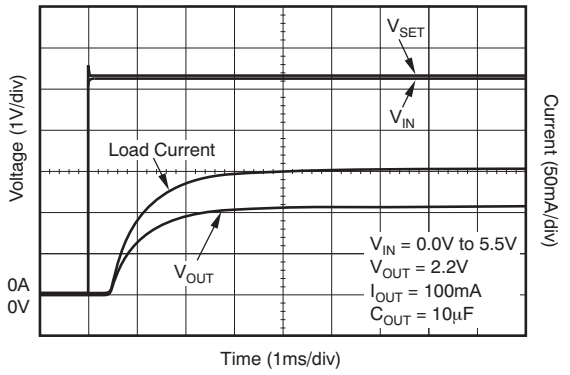


Figure 44. TPS780330220 Input Voltage vs Delay to Output

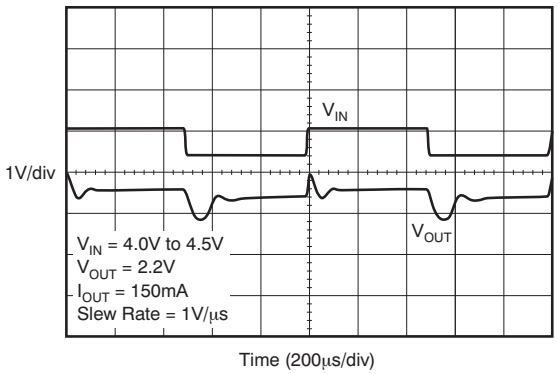


Figure 45. TPS780330220 Line Transient Response

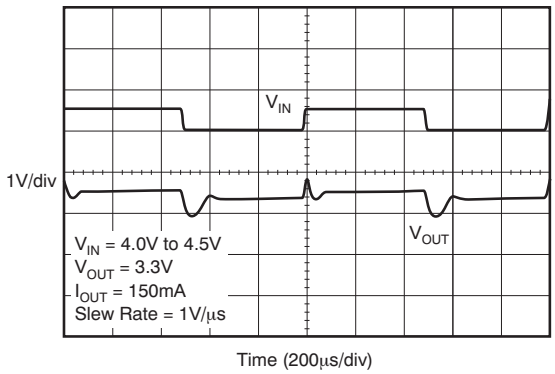


Figure 46. TPS780330220 Line Transient Response

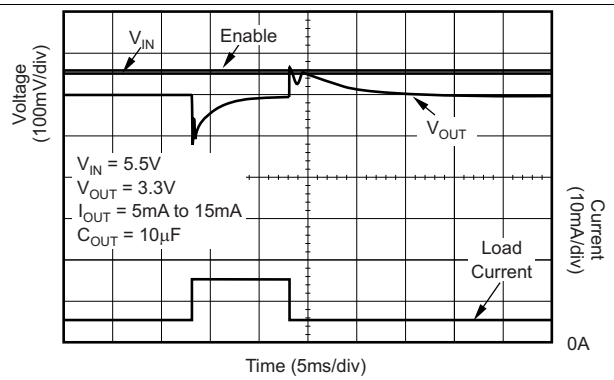


Figure 47. TPS780330220 Load Transient Response

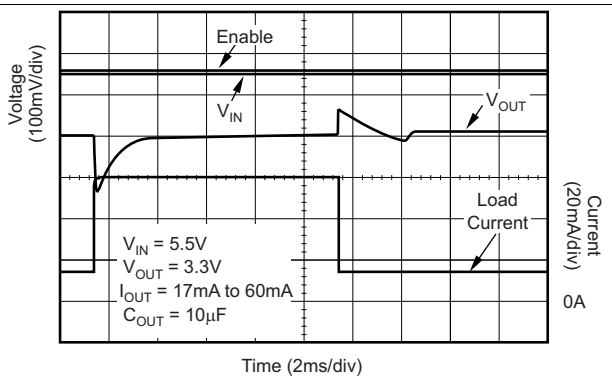


Figure 48. TPS780330220 Load Transient Response

Typical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.2 V, whichever is greater; I_{OUT} = 100 µA, V_{EN} = V_{VSET} = V_{IN}, C_{OUT} = 1 µF, and C_{IN} = 1 µF, unless otherwise noted.

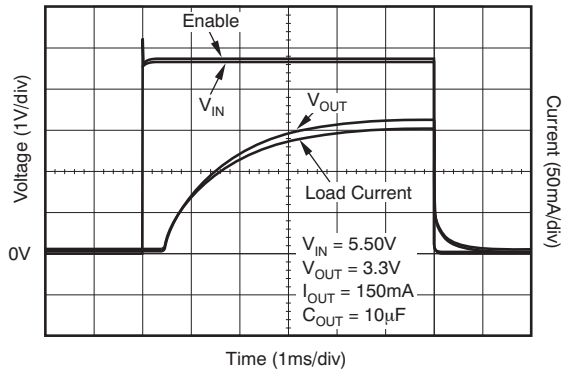


Figure 49. TPS780330220 Enable Pin vs Output Voltage Response and Output Current

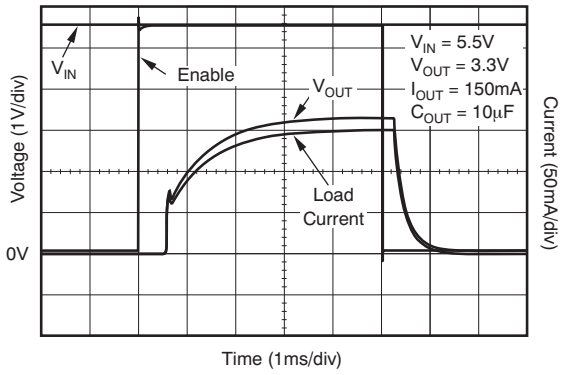


Figure 50. TPS780330220 Enable Pin vs Output Voltage Delay

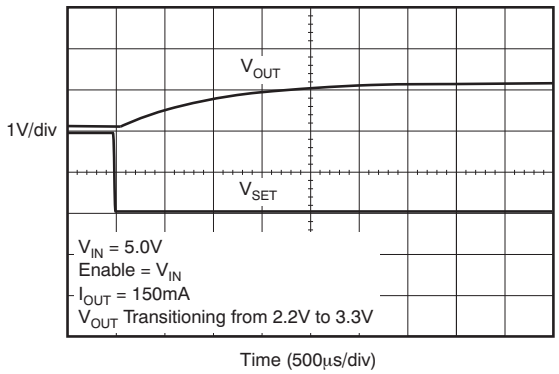


Figure 51. TPS780330220 VSET Pin Toggle

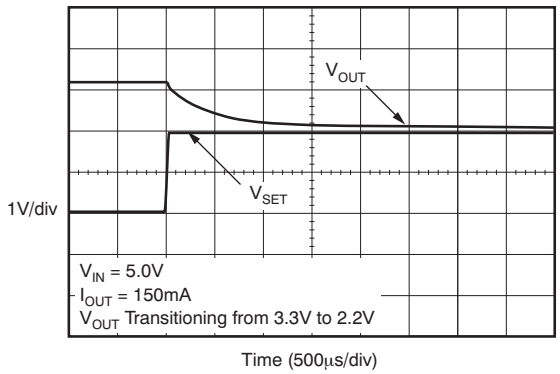


Figure 52. TPS780330220 VSET Pin Toggle

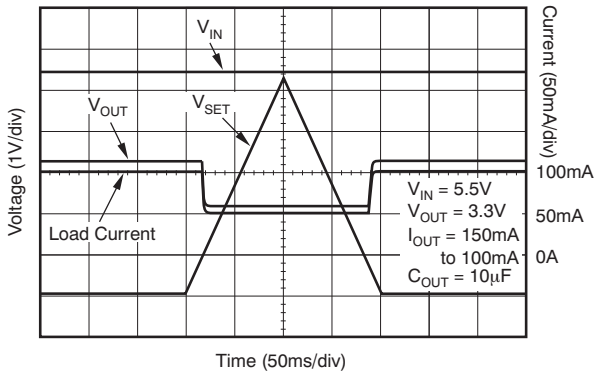


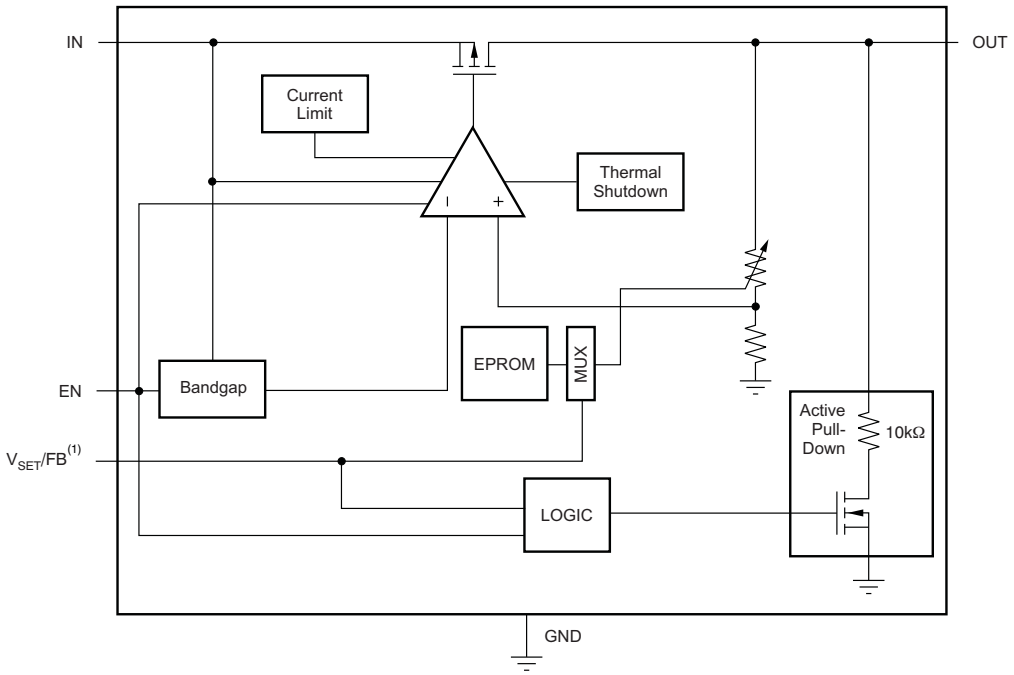
Figure 53. TPS780330220 VSET Pin Toggle (Slow Ramp)

7 Detailed Description

7.1 Overview

The TPS780 family of low-dropout regulators (LDOs) is designed specifically for battery-powered applications where ultralow quiescent current is a critical parameter. The absence of pulldown circuitry at the output of the LDO provides the flexibility to use the regulator output capacitor as a temporary backup power supply for a short period of time (for example, during battery replacement). The TPS780 family is compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO family is stable with any output capacitor greater than 1.0 µF.

7.2 Functional Block Diagram



(1) Feedback pin (FB) for adjustable versions; V_{SET} for fixed voltage versions.

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS780 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS780 family has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, connect EN to the IN pin, as shown in Figure 54.

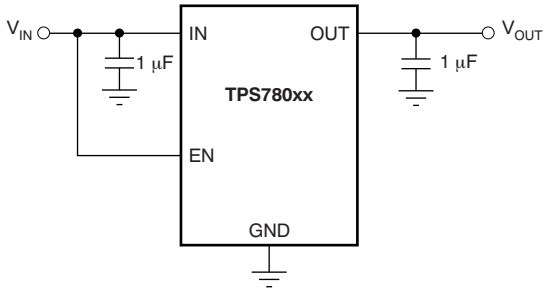


Figure 54. Circuit Showing EN Tied High When Shutdown Capability is not Required

7.3.3 Active V_{OUT} Pulldown

In the TPS780 series, the active pulldown discharges V_{OUT} when the device is off. However, the input voltage must be greater than 2.2 V for the active pulldown to work.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage ($V_{EN} > V_{EN(HI)}$) and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage ($V_{EN} < V_{EN(LO)}$) or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ($T_J > T_{SD}$).

7.5 Programming

7.5.1 Programming the TPS78001 Adjustable LDO Regulator

The output voltage of the TPS78001 adjustable regulator is programmed using an external resistor divider as shown in Figure 55. The output voltage operating range is 1.2 V to 5.1 V, and is calculated using Equation 1:

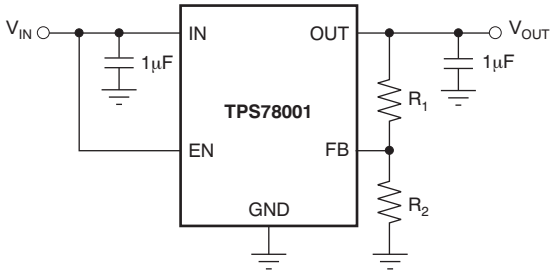
$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where

- V_{FB} = 1.216 V typical (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 1.2-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided because leakage current into/out of FB across R_1/R_2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT}. Table 2 lists several common output voltages and resistor values. The recommended design procedure is to choose R_2 = 1 MΩ to set the divider current at 1.2 µA, and then calculate R_1 using Equation 2:

$$R_1 = \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \times R_2 \quad (2)$$



$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$$

Figure 55. TPS78001 Adjustable LDO Regulator Programming

Table 2. Output Voltage Programming Guide

OUTPUT VOLTAGE	R_1	R_2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS780 family of LDOs is factory-programmable to have a fixed output. Note that during start-up or steady-state conditions, do not allow the EN pin voltage to exceed V_{IN} + 0.3 V.

8.2 Typical Application

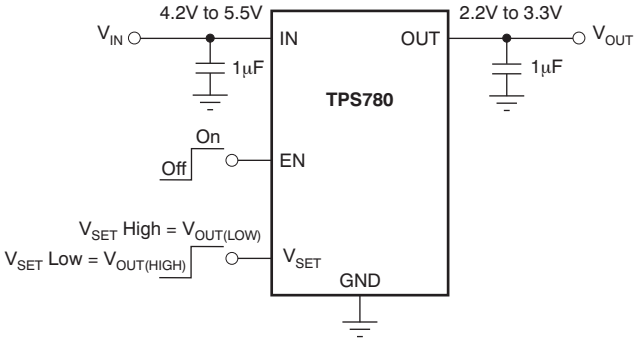


Figure 56. Typical Application Circuit

8.2.1 Design Requirements

Table 3. Design Paramters

PARAMETER	DESIGN REQUIREMENT
Input Voltage	5 V
Output Voltage High	3.6 V
Output Voltage Low	2 V
Maximum Output Current	100 mA

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND pin current, and power the load. Select input and output capacitors based on application needs.

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS780 family is designed to be stable with standard ceramic capacitors with values of 1.0 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 µF.

8.2.2.2 Dropout Voltage

The TPS780 family uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in *Typical Characteristics*. Refer to application report SLVA207, *Understanding LDO Dropout*, available from www.ti.com.

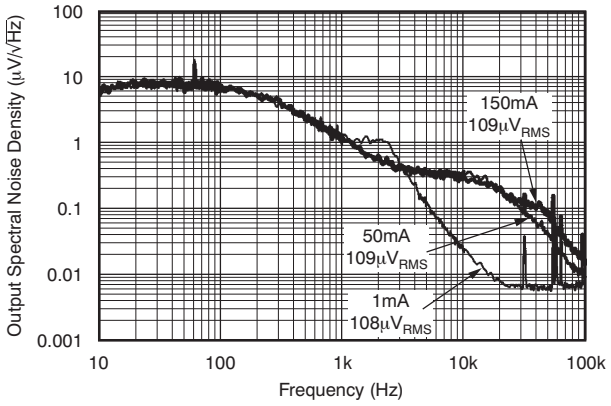
8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response. For more information, see Figure 48.

8.2.2.4 Minimum Load

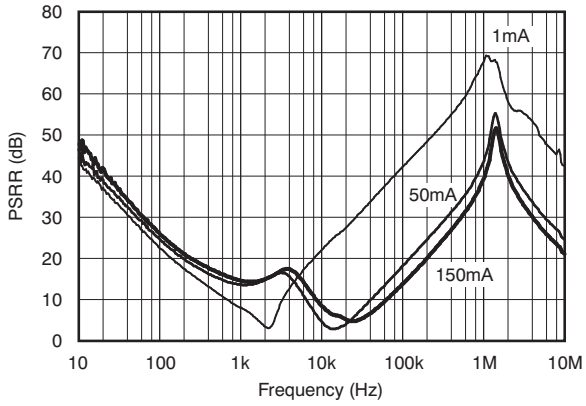
The TPS780 family is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS780 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See for the load transient response.

8.2.3 Application Curves



C_{IN} = 1 µF, C_{OUT} = 2.2 µF, V_{VSET} = 1.2 V, V_{IN} = 2.7 V

Figure 57. TPS780330220 Output Spectral Noise Density vs Frequency



V_{IN} = 2.7 V, V_{OUT} = 1.2 V, C_{OUT} = 2.2 µF

Figure 58. TPS78001 Ripple Rejection vs Frequency

8.3 Do's and Don'ts

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

For best performance, connect a low-output impedance power supply directly to the IN pin of the TPS780. Inductive impedances between the input supply and the IN pin create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

9.1 Powering the MSP430 Microcontroller

Several versions of the TPS780 are ideal for powering the MSP430 microcontroller. Table 4 shows potential applications of some voltage versions.

Table 4. Typical MSP430 Applications

DEVICE	$V_{OUT(HI)}$ (TYP)	$V_{OUT(LO)}$ (TYP)	APPLICATION
TPS780360200	3.6 V	2.0 V	$V_{OUT, MIN}$ > 1.800 V required by many MSP430s. Allows lowest power consumption operation.
TPS780360220	3.6 V	2.2 V	$V_{OUT, MIN}$ > 2.200 V required by some MSP430s FLASH operation.
TPS780360300	3.6 V	3.0 V	$V_{OUT, MIN}$ > 2.700 V required by some MSP430s FLASH operation.
TPS780360220	3.6 V	2.2 V	$V_{OUT, MIN}$ < 3.600 V required by some MSP430s. Allows highest speed operation.

The TPS780 family offers many output voltage versions to allow designers to optimize the supply voltage for the processing speed required of the MSP430. This flexible architecture minimizes the supply current consumed by the particular MSP430 application. The MSP430 total system power can be reduced by substituting the 500-nA I_Q TPS780 series LDO in place of an existing ultralow I_Q LDO (typical best case = 1 µA). Additionally, DVS allows for increasing the clock speed in active mode (MSP430 V_{CC} = 3.6 V). The 3.6-V V_{CC} reduces the MSP430 time in active mode. In low-power mode, MSP430 system power can be further reduced by lowering the MSP430 V_{CC} to 2.2 V in sleep mode.

Key features of the TPS780 series are an ultralow quiescent current (500 nA), DVS, and miniaturized packaging. The TPS780 family are available in SON-6 and TSOT-23 packages. Figure 59 shows a typical MSP430 circuit powered by an LDO without DVS. Figure 60 is an MSP430 circuit using a TPS780 LDO that incorporates an integrated DVS, thus simplifying the circuit design. In a circuit without DVS, as Figure 59 illustrates, V_{CC} is always at 3.0 V. When the MSP430 goes into sleep mode, V_{CC} remains at 3.0 V; if DVS is applied, V_{CC} could be reduced in sleep mode. In Figure 60, the TPS780 LDO with integrated DVS maintains 3.6-V V_{CC} until a logic high signal from the MSP430 forces V_{OUT} to level shift V_{OUT} from 3.6 V down to 2.2 V, thus reducing power in sleep mode.

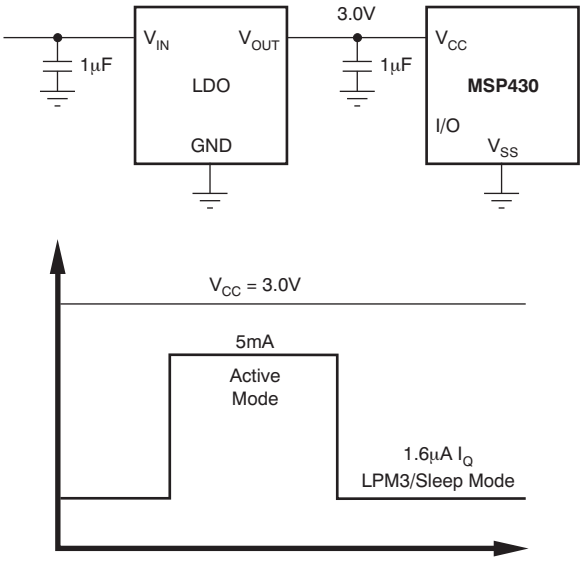


Figure 59. Typical LDO Without DVS

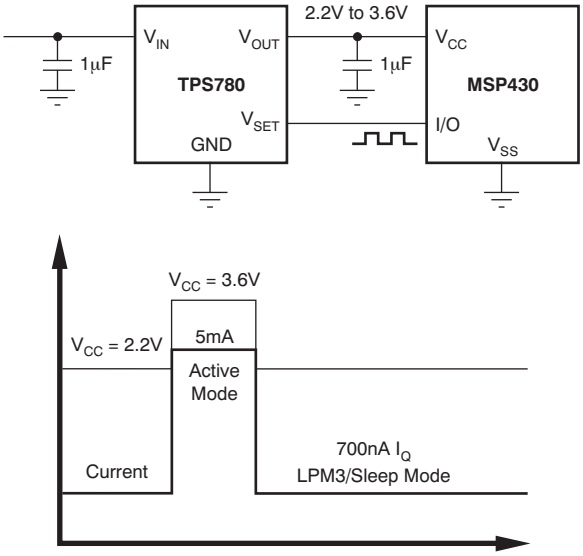


Figure 60. TPS780 With Integrated DVS

The other benefit of DVS is that it allows a higher V_{CC} voltage on the MSP430, increasing the clock speed and reducing the active mode dwell time.

The total system power savings is outlined in Table 5, Table 6, and Table 7. In Table 5, the MSP430 power savings are calculated for various MSP430 devices using a TPS780 series with integrated DVS versus a standard ultralow IQ LDO without DVS. In Table 6, the TPS780 series quiescent power is calculated for a VIN of 4.2 V, with the same VIN used for the ultralow IQ LDO. Quiescent power dissipation in an LDO is the VIN voltage times the ground current, because zero load is applied. After the dissipation power is calculated for the individual LDOs in Table 6, simple subtraction outputs the LDO power savings using the TPS780 series. Table 7 calculates the total system power savings using a TPS780 series LDO in place of an ultralow IQ 1.2-µA LDO in an MSP430F1121 application. There are many different versions of the MSP430. Actual power savings vary depending on the selected device.

Table 5. DDV MSP430 Power Savings With the TPS780 Series on Selected MSP430 Devices

DEVICE	LPM3 AT V_{CC} = 3 V, I_Q (µA)	LPM3 AT V_{CC} = 3.0 V × I_Q (µW)	LPM3 AT V_{CC} = 2.2 V, I_Q (µA)	LPM3 AT V_{CC} = 2.2 V × I_Q (µW)	µW SAVINGS USING ONLY DVS
MSP430F1121	1.6	4.8	0.7	1.5	3.3
MSP430F149	1.6	4.8	0.9	2.0	2.8
MSP430F2131	0.9	2.7	0.7	1.5	1.2
MSP430F249	1.0	3.0	0.9	2.0	1.0
MSP430F413	0.9	2.7	0.7	1.5	1.2
MSP430F449	1.6	4.8	1.1	2.4	2.4

Table 6. Typical Ultralow I_Q LDO Quiescent Power Dissipation vs the TPS780 Series

TYPICAL ULTRALOW I_Q LDO AT 25°C AMBIENT	TYPICAL ULTRALOW I_Q LDO AT 25°C AMBIENT POWER DISSIPATION	TPS780 SERIES TYPICAL I_Q AT 25°C AMBIENT	TPS780 SERIES AT 25°C AMBIENT, POWER DISSIPATION	MSP430 SYSTEM POWER SAVINGS USING THE TPS780 SERIES
I_Q (µA)	$I_Q \times V_{IN}$ = 4.2 V (µW)	TPS780 I_Q (µA)	$I_Q \times V_{IN}$ = 4.2 V (µW)	Quiescent Power Dissipation Savings (µW)
1.20	5.04	0.42	1.76	3.28

Table 7. Total System Power Dissipation

	LDO DISSIPATION	MSP430 DISSIPATION	TOTAL SYSTEM POWER IN SLEEP MODE 3
Typical 1.2 µA LDO, no DVS	5.04 µW	4.8 µW(1)	9.84 µW
TPS780 Series with DVS	1.76 µW	1.5 µW(1)	3.26 µW

(1) Value taken from Table 5 and relative to the MSP430F1121.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the printed circuit board (PCB) with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the output capacitor must be as close as possible to the ground pin of the device to provide a common reference for regulation purposes. High ESR capacitors may degrade PSRR.

10.1.2 Package Mounting

Solder pad footprint recommendations for the TPS780 series are available from the Texas Instruments web site at www.ti.com through the TPS780 series product folders.

10.2 Layout Example

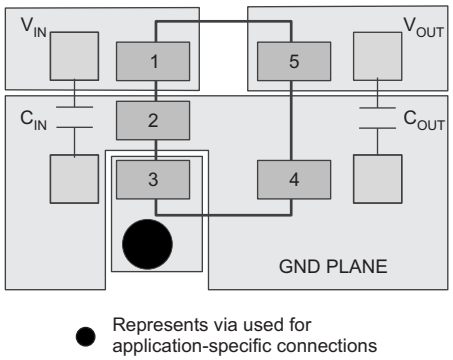


Figure 61. TPS780xx DDC Package Layout Example

10.3 Thermal Considerations

Thermal protection disables the device output when the junction temperature rises to approximately 160°C, allowing the device to cool. After the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 105°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TPS780 family is designed to protect against overload conditions. However, this circuitry is not intended to replace proper heatsinking. Continuously running the TPS780 series into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS780. The TPS780XXEVM-301 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS780 series is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 8. Device Nomenclature(1) (2)

PRODUCT	V_{OUT}
TPS780**vvvxxx** ***yyy z***	**vvv** is the nominal output voltage for $V_{OUT(HI)}$ and corresponds to V_{SET} pin low. **xxx** is the nominal output voltage for $V_{OUT(LO)}$ and corresponds to V_{SET} pin high. **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). Adjustable version(3)(4)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Additional output voltage combinations are available on a quick-turn basis using innovative, factory EPROM programming. Minimum order quantities apply; contact your sales representative for details and availability.
(3) To order the adjustable version, use *TPS78001YYYZ*.
(4) The device is either fixed voltage, dual-level V_{OUT}, or adjustable voltage only. Device design does not permit a fixed and adjustable output simultaneously.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Application note: *Understanding LDO Dropout*, SLVA207.
- *TPS780XXEVM-301 User's Guide*, SLVU235.

11.3 Trademarks

MSP430 is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS78001DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEA
TPS78001DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEA
TPS78001DDCRG4	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEA
TPS78001DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEA
TPS78001DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEA
TPS78001DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEA
TPS78001DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEA
TPS78001DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEA
TPS78001DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEA
TPS780180300DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAX
TPS780180300DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAX
TPS780180300DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAX
TPS780180300DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RAX
TPS780180300DRVTG4.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
TPS780230300DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NXP
TPS780230300DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NXP
TPS780230300DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NXP
TPS780230300DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	NXP
TPS780270200DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN
TPS780270200DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN
TPS780270200DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN
TPS780270200DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS780270200DDCTG4	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN
TPS780270200DDCTG4.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVN
TPS780300250DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OAI
TPS780300250DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OAI
TPS780300250DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OAI
TPS780300250DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OAI
TPS780330200DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13A
TPS780330200DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13A
TPS780330200DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13A
TPS780330200DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13A
TPS780330220DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEC
TPS780330220DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEC
TPS780330220DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEC
TPS780330220DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEC
TPS780330220DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEC
TPS780330220DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEC
TPS780330220DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEC
TPS780330220DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CEC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

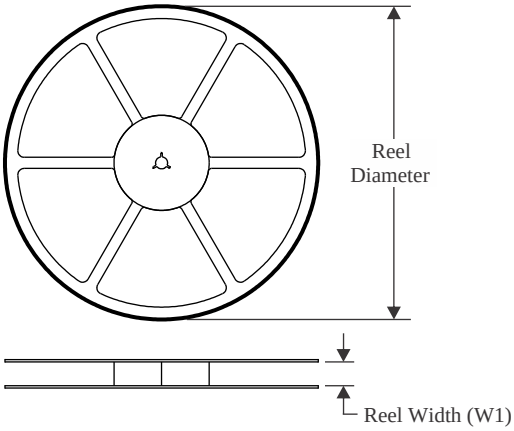
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

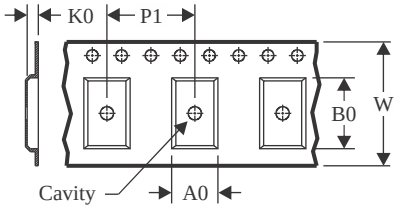
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

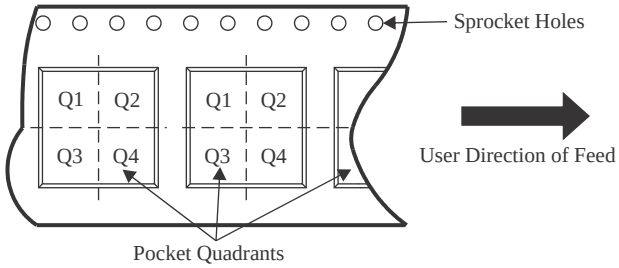


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

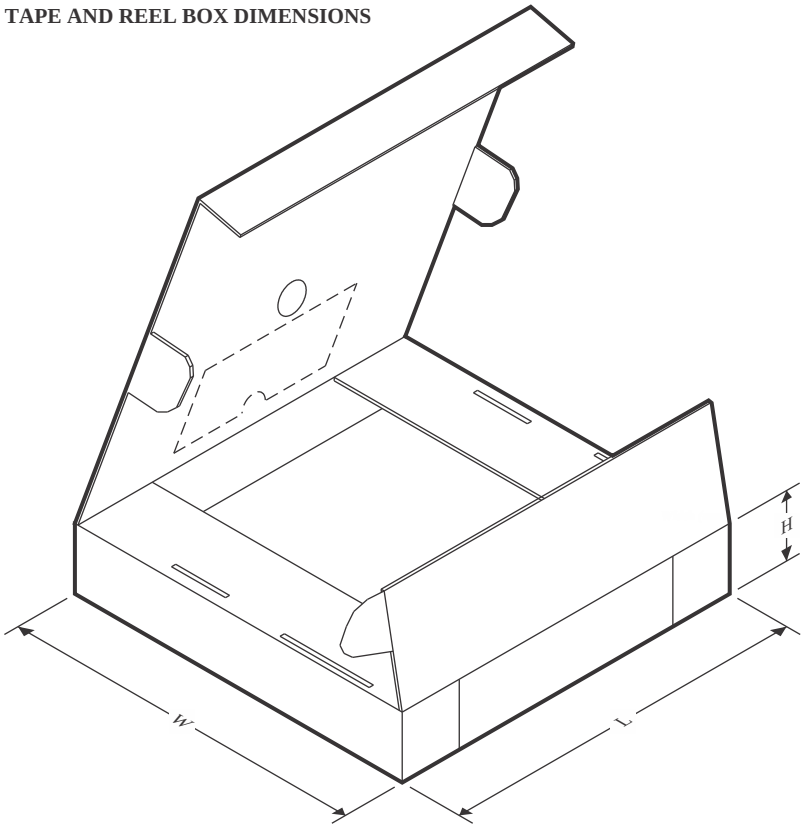


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78001DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78001DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78001DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS78001DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS78001DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS780180300DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780180300DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS780180300DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780230300DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780230300DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS780230300DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780230300DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS780270200DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS780270200DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780270200DDCTG4	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780300250DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780300250DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS780300250DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780330200DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780330200DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780330220DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780330220DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS780330220DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS780330220DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

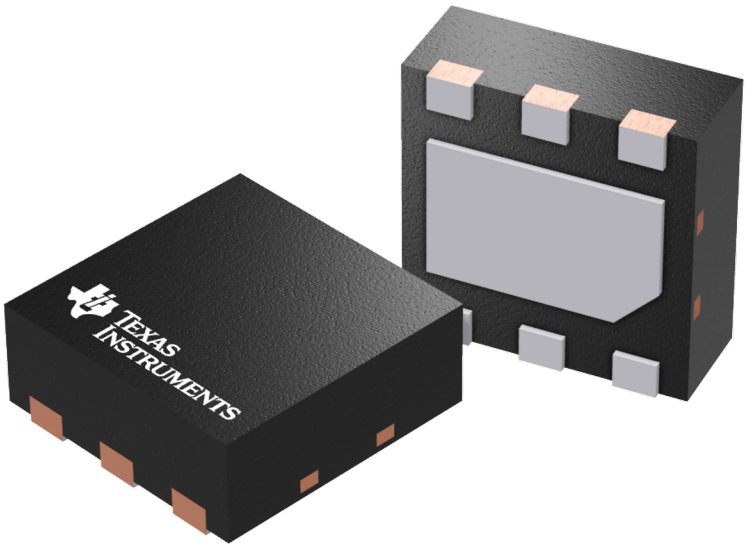
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78001DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78001DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78001DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS78001DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS78001DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS780180300DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS780180300DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS780180300DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS780230300DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS780230300DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS780230300DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS780230300DRVT	WSON	DRV	6	250	203.0	203.0	35.0
TPS780270200DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS780270200DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS780270200DDCTG4	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS780300250DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS780300250DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS780300250DRVT	WSON	DRV	6	250	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS780330200DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS780330200DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS780330220DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS780330220DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS780330220DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS780330220DRVT	WSON	DRV	6	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

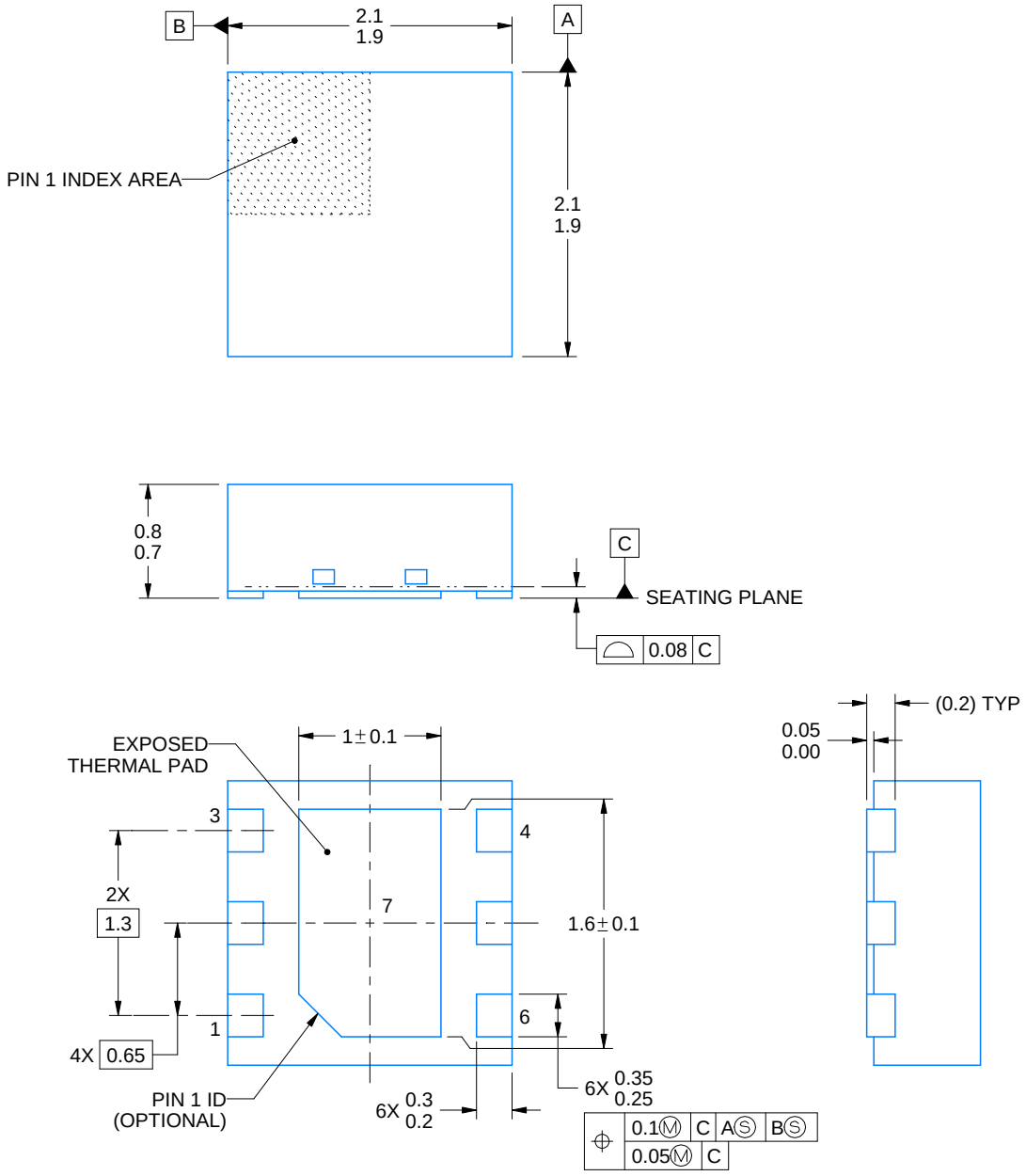
4206925/F

PACKAGE OUTLINE

DRV0006A

WSON - 0.8 mm max height

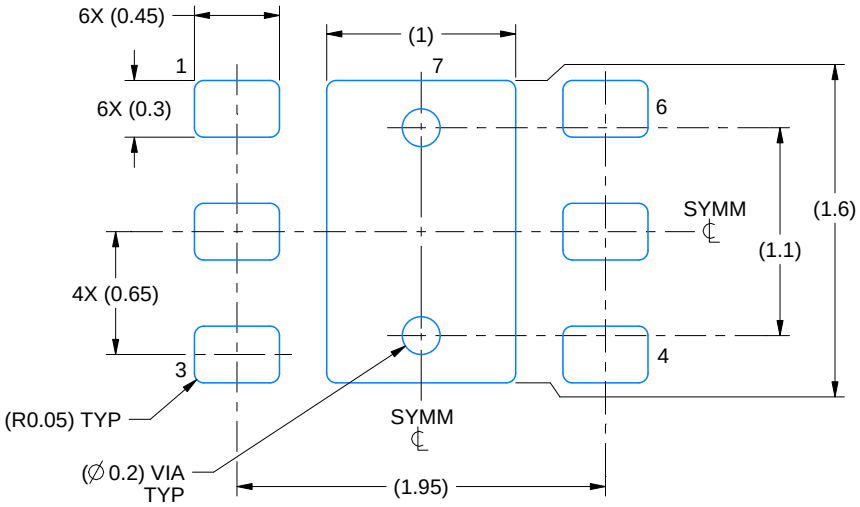
PLASTIC SMALL OUTLINE - NO LEAD



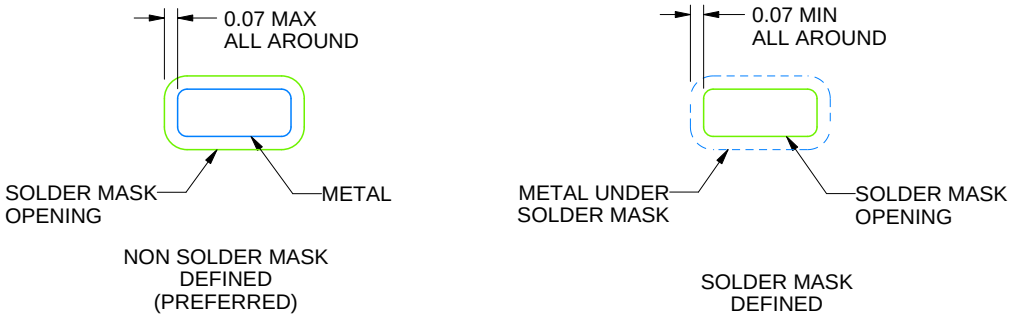
4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

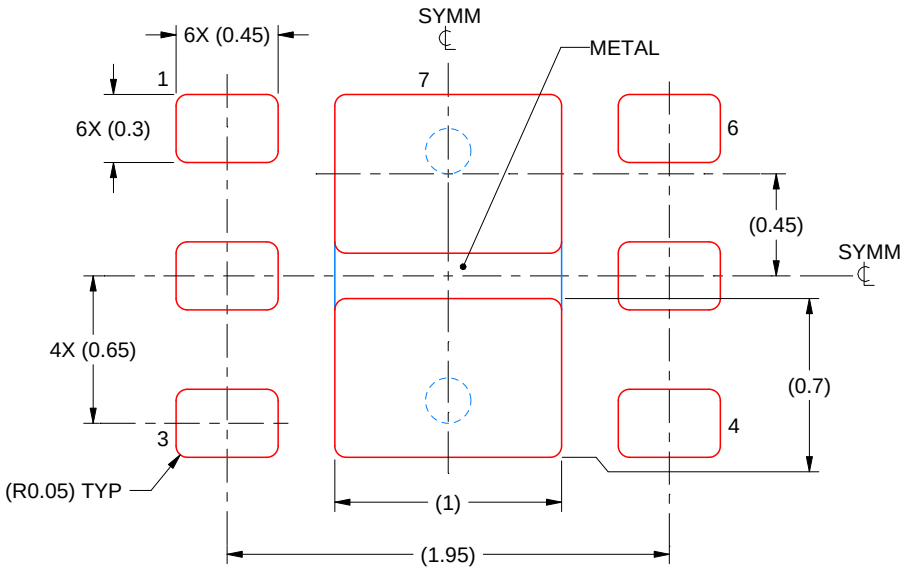


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



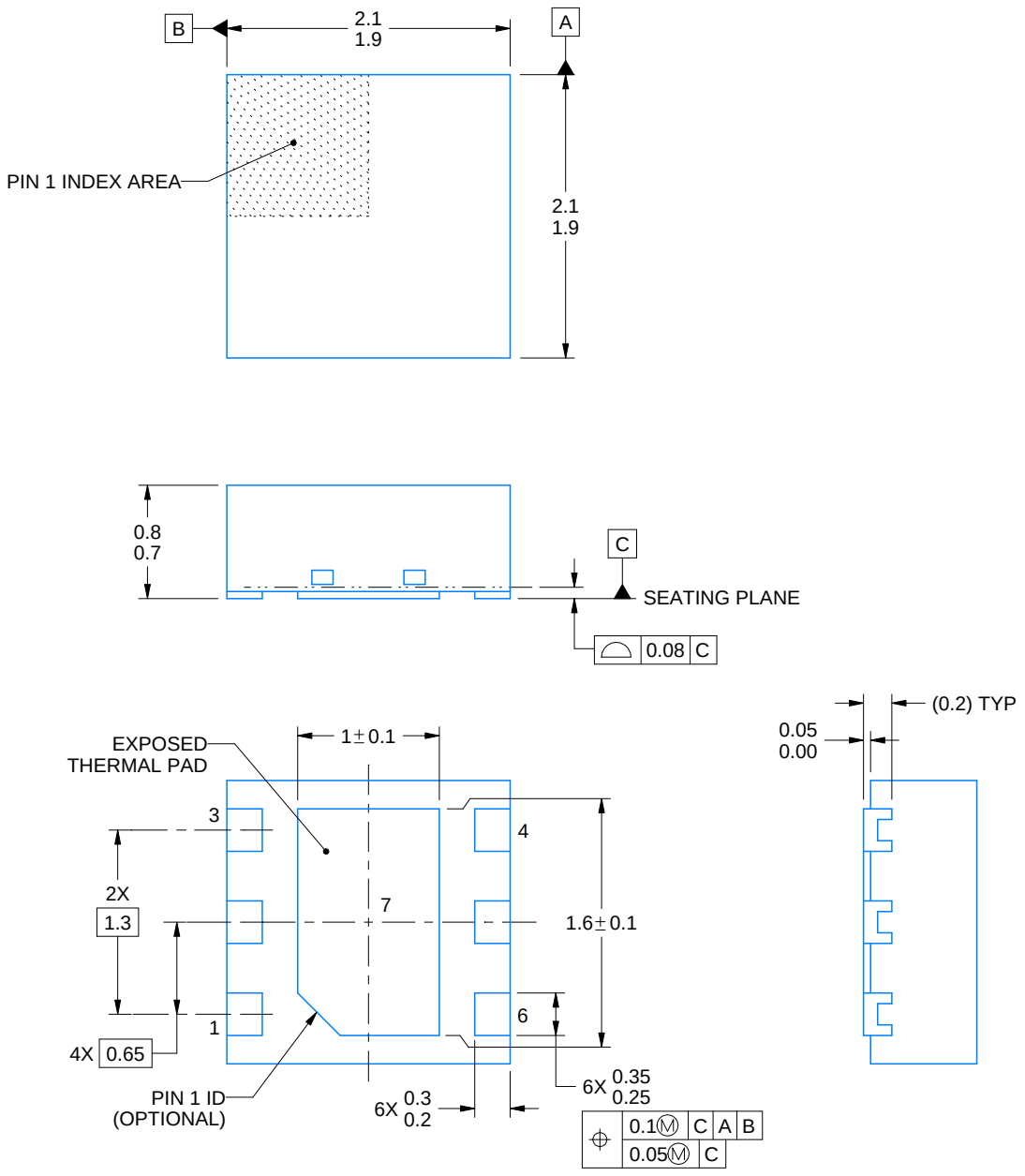
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

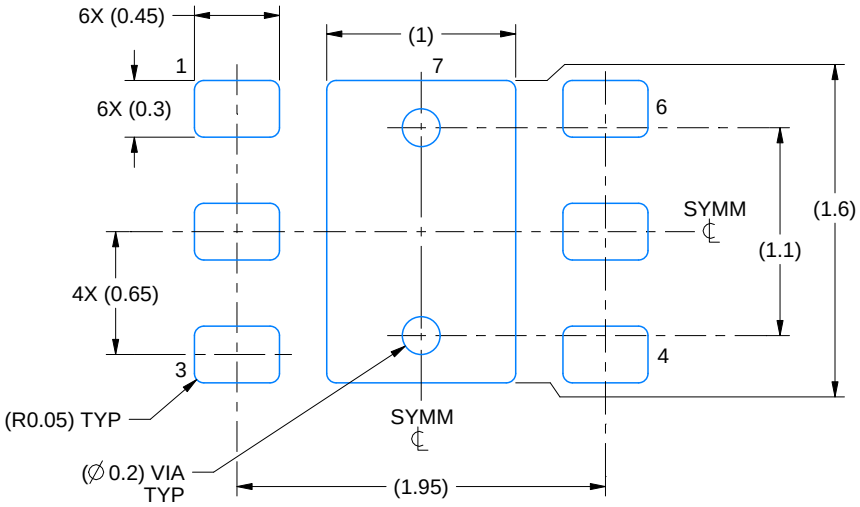
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

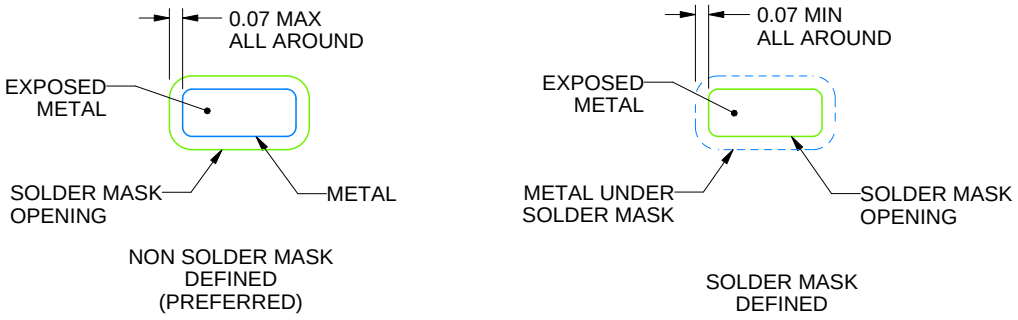


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

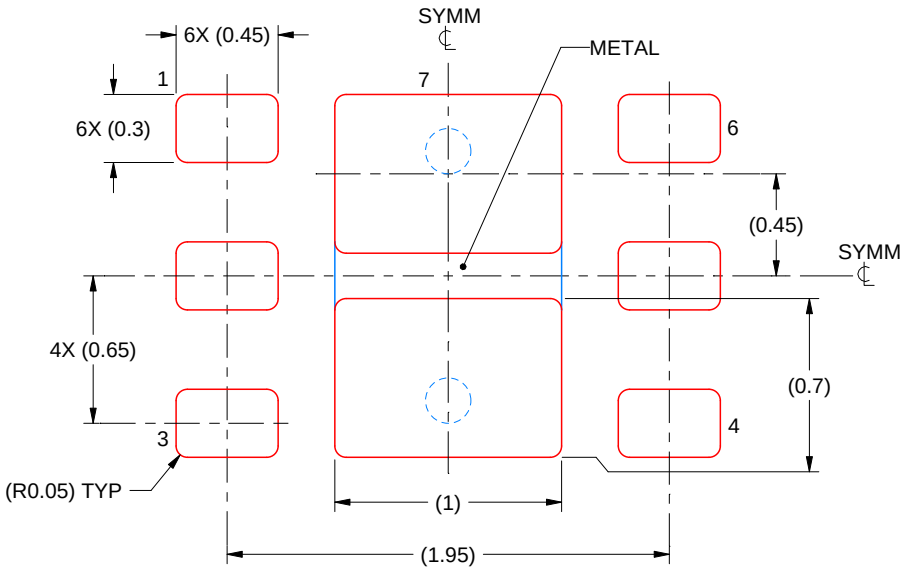


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

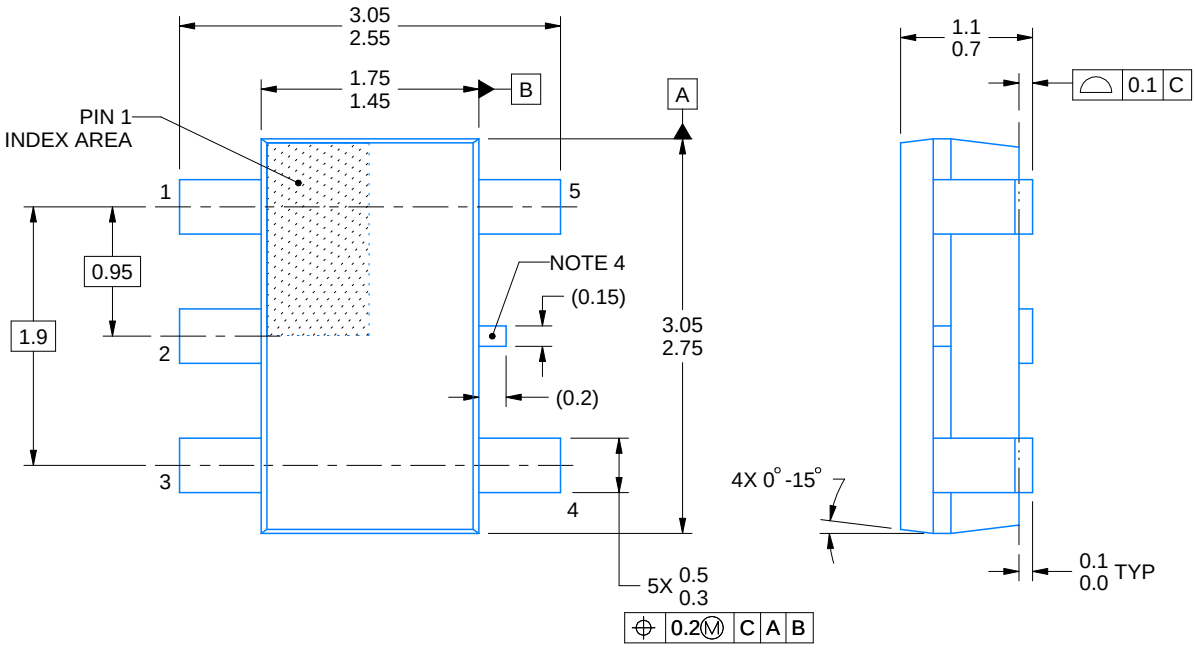
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

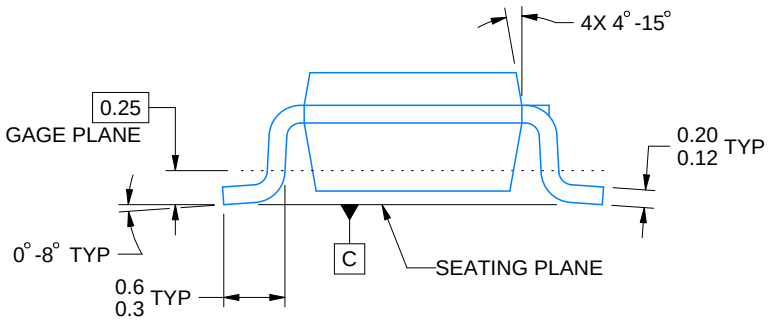
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

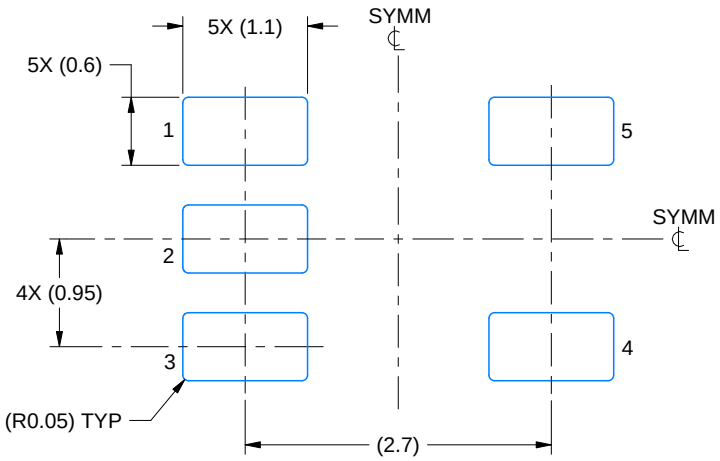




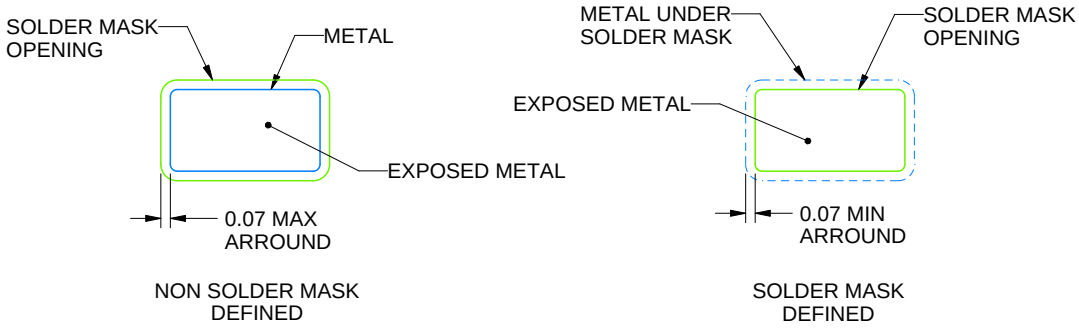
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

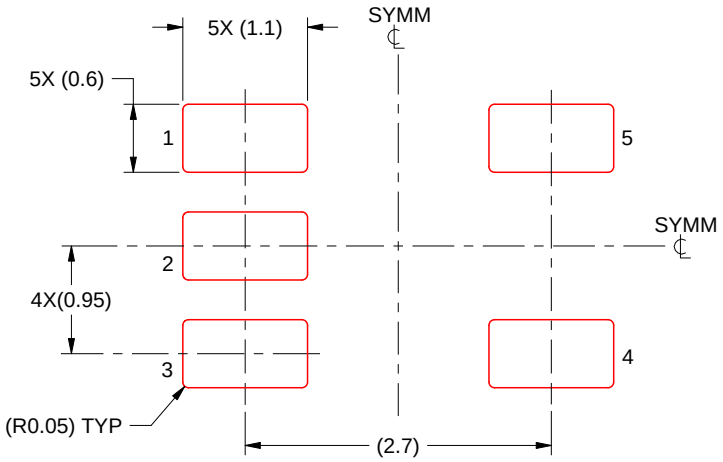


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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