TOSHIBA BiCD Integrated Circuit Silicon Monolithic

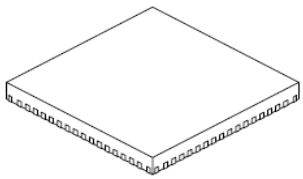
TB67S128FTG

CLOCK-in and Serial controlled Bipolar Stepping Motor Driver

1. Description

TB67S128FTG is a two-phase bipolar stepping motor driver using a PWM chopper. The clock in decoder is built in.
Fabricated with the BiCD process, output rating is 50 V/5.0 A (Motor supply voltage = 44 V).

TB67S128FTG



P-VQFN64-0909-0.50-006

Weight: 0.229 g (typ.)

2. Features

- BiCD process integrated monolithic IC.
- Capable of controlling 1 bipolar stepping motor.
- PWM controlled constant-current drive
- Low on-resistance (High + Low side = 0.25 Ω (typ.))
  MOSFET output stage.
- Allows full, half, quarter, 1/8, 1/16, 1/32, 1/64, and 1/128 step operation.
- High efficiency motor current control mechanism (ADMD: Advanced Dynamic Mixed Decay)
- Built-in Anti-stall architecture (AGC: Active Gain Control)
- Built-in Sense resistor less current control architecture (ACDS: Advanced Current Detection System)
- High voltage and current (For specification, please refer to absolute maximum ratings and operating ranges)
- Multi error detect functions (Thermal shutdown (TSD), Over current (ISD), Power-on-reset (POR), motor load open (OPD)).
- Error detection (TSD/ISD/OPD) flag output function
- Built-in VCC regulator for internal circuit
- Chopping frequency of a motor can be adjusted by external resistance and capacitor.
- Small package with thermal pad
- TB67S128FTG: P-VQFN64-0909-0.50-006

Note: Please be careful about thermal conditions during using.

Start of commercial production
2019-01

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3. Pin Assignment

Pin assignment in CLK mode (IF_SEL pin = L) is shown in below figure.

<TOP View>

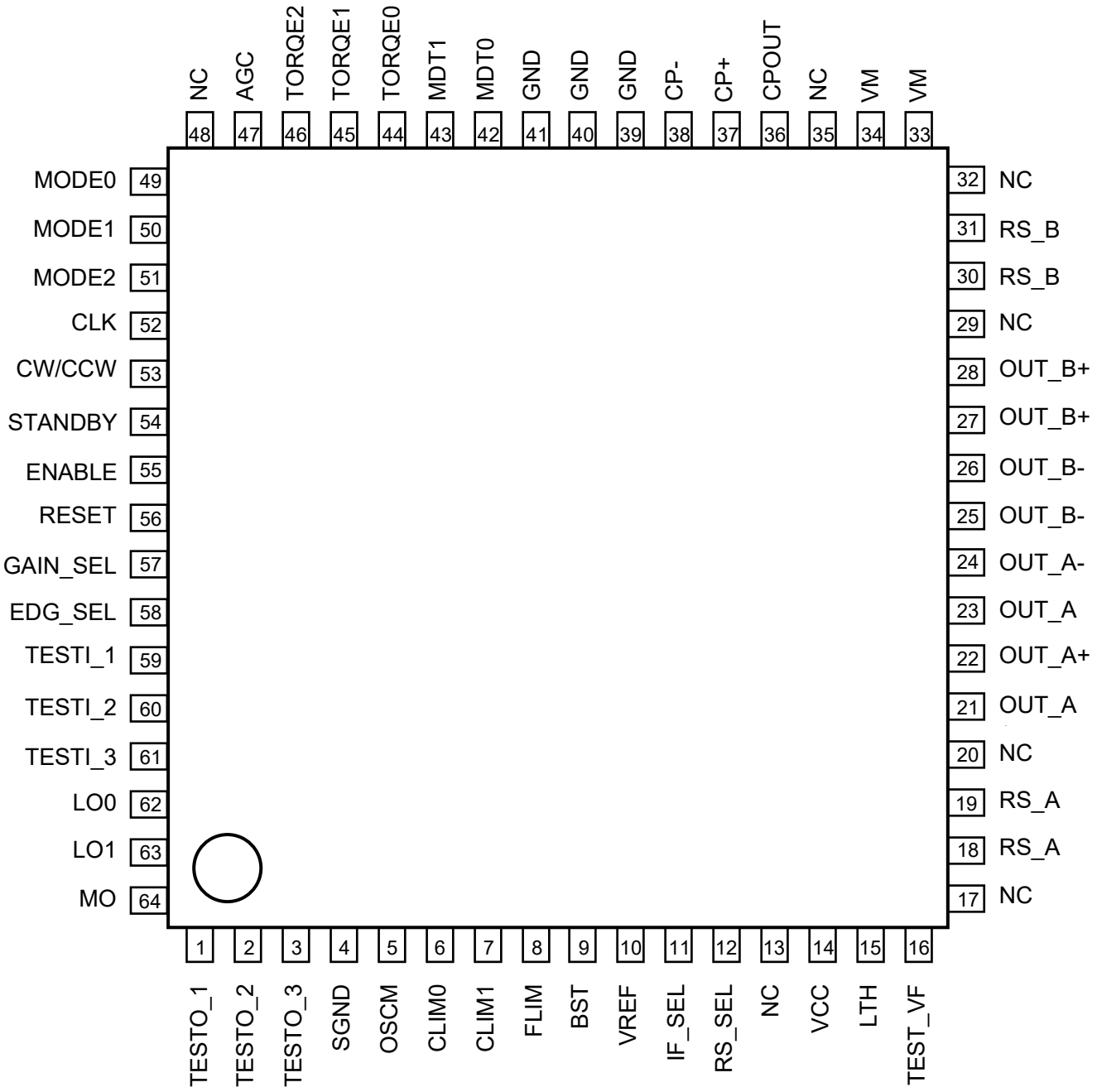

Table 3.1 Pin Assignments

Note: Please solder the corner pads and the rear thermal pad of the QFN package, to the GND pattern of the PCB.

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4. Pin Description

Table 4.1 Pin Function Description

Pin No.	Symbol		Description
	CLK mode	Serial mode	
1	TESTO_1 (Note1)	TESTO_1 (Note1)	TEST OUT pin No.1
2	TESTO_2 (Note1)	TESTO_2 (Note1)	TEST OUT pin No.2
3	TESTO_3 (Note1)	TESTO_3 (Note1)	TEST OUT pin No.3
4	SGND	SGND	Logic ground pin
5	OSCM	OSCM	Internal oscillator frequency monitor and setting pin
6	CLIM0 (Note1)	NC (Note1)	AGC current limiter setup pin No.0
7	CLIM1 (Note1)	NC (Note1)	AGC current limiter setup pin No.1
8	FLIM (Note1)	NC (Note1)	AGC frequency limiter setup pin
9	BST (Note1)	NC (Note1)	AGC current boost setup pin
10	VREF	VREF	Current threshold reference pin
11	IF_SEL	IF_SEL	Interface select pin
12	RS_SEL	NC (Note1)	RS mode select pin
13	NC	NC	NC pin
14	VCC	VCC	Internal regulator voltage monitor pin
15	LTH (Note1)	LTH (Note1)	AGC threshold setup pin
16	TEST_VF (Note1)	TEST_VF (Note1)	TEST monitor (3VF)
17	NC	NC	NC Pin
18	RS_A (Note2)	RS_A (Note2)	Ach current sense resistor connected pin / Ach motor power ground pin
19	RS_A (Note2)	RS_A (Note2)	Ach current sense resistor connected pin / Ach motor power ground pin
20	NC	NC	NC pin
21	OUT_A+ (Note2)	OUT_A+ (Note2)	Ach motor output(+) pin
22	OUT_A+ (Note2)	OUT_A+ (Note2)	Ach motor output(+) pin
23	OUT_A- (Note2)	OUT_A- (Note2)	Ach motor output(-) pin
24	OUT_A- (Note2)	OUT_A- (Note2)	Ach motor output(-) pin
25	OUT_B- (Note2)	OUT_B- (Note2)	Bch motor output(-) pin
26	OUT_B- (Note2)	OUT_B- (Note2)	Bch motor output(-) pin
27	OUT_B+ (Note2)	OUT_B+ (Note2)	Bch motor output(+) pin
28	OUT_B+ (Note2)	OUT_B+ (Note2)	Bch motor output(+) pin
29	NC	NC	NC pin
30	RS_B (Note2)	RS_B (Note2)	Bch current sense resistor connected pin / Bch motor power ground pin
31	RS_B (Note2)	RS_B (Note2)	Bch current sense resistor connected pin / Bch motor power ground pin
32	NC	NC	NC pin
33	VM (Note2)	VM (Note2)	Motor power supply input pin
34	VM (Note2)	VM (Note2)	Motor power supply input pin
35	NC	NC	NC pin
36	CPOUT	CPOUT	Pin for Charge pump
37	CP+	CP+	Pin for Charge pump

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Pin No.	Symbol		Description
	CLK mode	Serial mode	
38	CP-	CP-	Pin for Charge pump
39	GND	GND	GND
40	GND	GND	GND
41	GND	GND	GND
42	MDT0	NC (Note1)	Mixed Decay/ADMD setting pin
43	MDT1	NC (Note1)	Mixed Decay/ADMD setting pin
44	TORQE0	NC (Note1)	Torque setting pin No.0
45	TORQE1	NC (Note1)	Torque setting pin No.1
46	TORQE2	NC (Note1)	Torque setting pin No.2
47	AGC	NC (Note1)	Active Gain Control setup pin
48	NC	NC	NC pin
49	MODE0	NC (Note1)	Excitation setting pin No.0
50	MODE1	NC (Note1)	Excitation setting pin No.1
51	MODE2	NC (Note1)	Excitation setting pin No.2
52	CLK	CLK	Step clock input pin / Serial clock input pin
53	CW/CCW	DATA	Current direction setup pin / Data input pin in serial interface
54	STANDBY	STANDBY	Standby pin
55	ENABLE	LATCH	Motor output ON/OFF pin / Latch Enable input pin
56	RESET	BANK_EN	Electrical angle initialize pin / BANK select pin
57	GAIN_SEL	NC (Note1)	Vref Gain setting pin
58	EDG_SEL	NC (Note1)	CLK edge setting pin
59	TESTI_1 (Note1)	TESTI_1 (Note1)	TEST input pin No.1
60	TESTI_2 (Note1)	TESTI_2 (Note1)	TEST input pin No.2
61	TESTI_3 (Note1)	TESTI_3 (Note1)	TEST input pin No.3
62	LO0	LO0	Error detection flag output pin No.0
63	LO1	LO1	Error detection flag output pin No.1
64	MO	NC (Note1)	Electrical angle monitor pin

Note1: When this pin is not used, the pin should be opened or connected to Ground.
Note2: The same name pins should be connected with PCB pattern to each other.

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5. Block Diagram

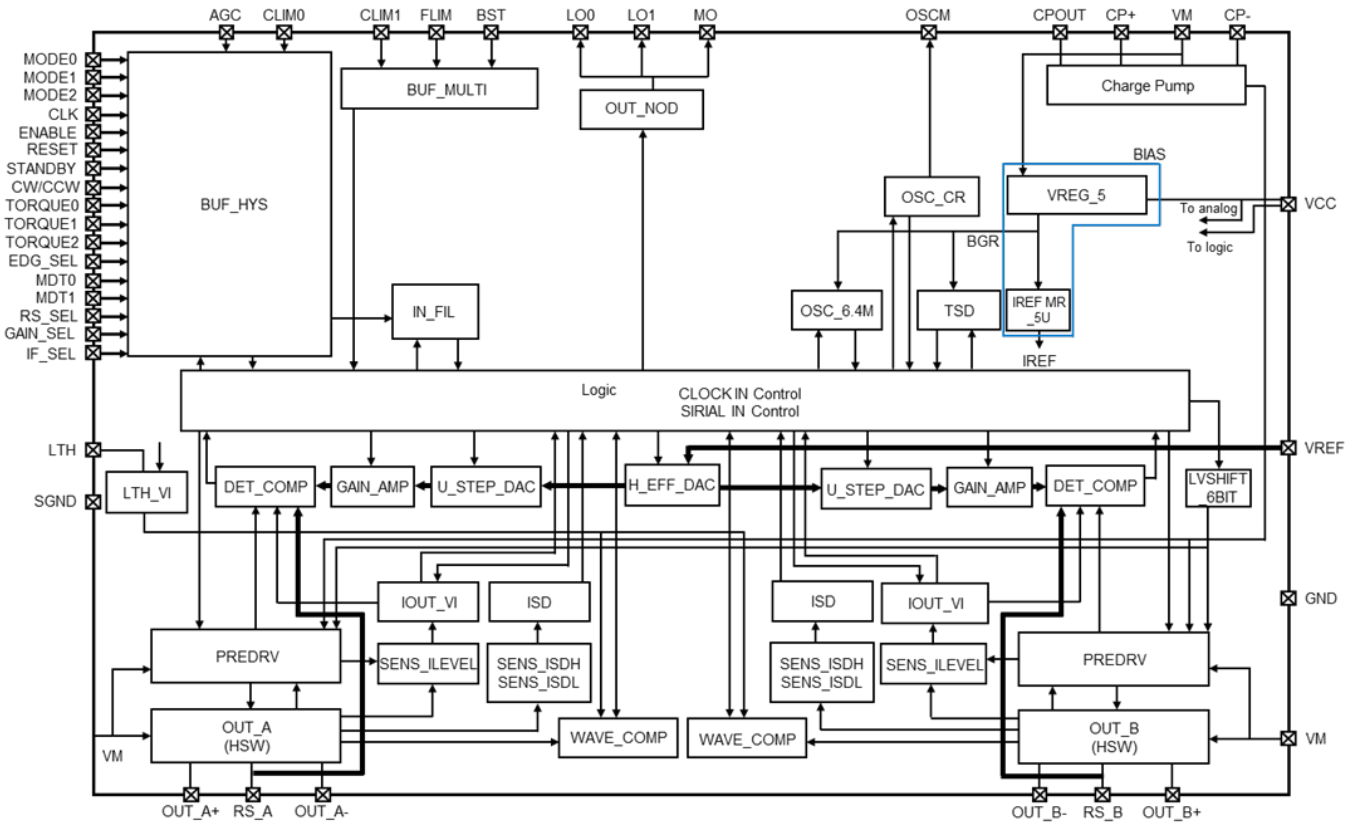

Table 5.1 Block Diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Note: All the grounding wires of TB67S128FTG should run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation. Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged. Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS line, OUT line, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed. The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

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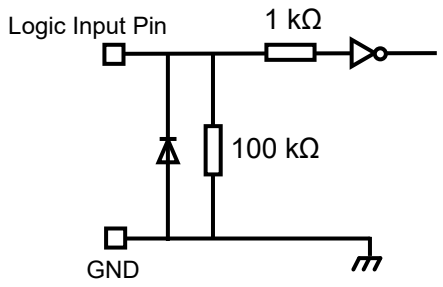
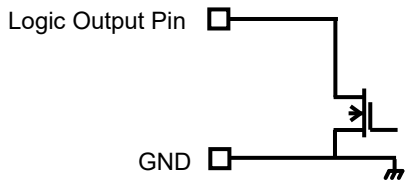
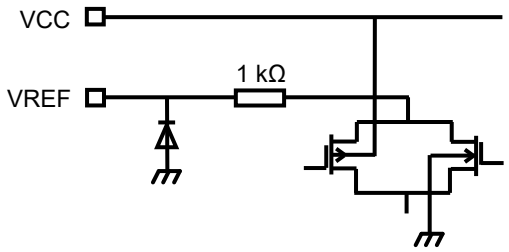
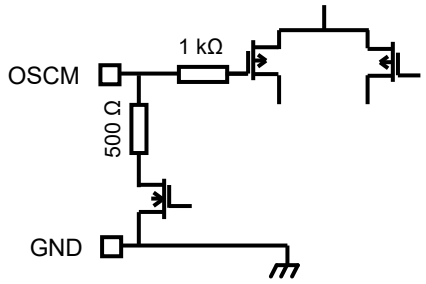
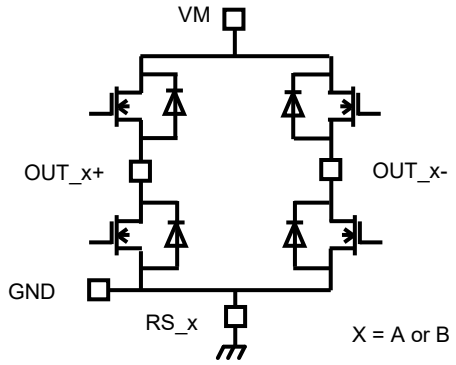
6. INPUT/OUTPUT Equivalent Circuit

Table 6.1 Input and Output Equivalent Circuit 1

Pin name	IN/OUT signal	Equivalent circuit
MODE0, 1, 2 CLK ENABLE RESET CW/CCW TORQE0, 1, 2 EDG_SEL MDT0, 1 RS_SEL GAIN_SEL IF_SEL STANDBY CLIM0 AGC	Digital Input (VIH/VIL) VIH: 2.0 V (min) to 5.5 V (max) VIL: 0 V (min) to 0.8 V (max)	
LO0, LO1 MO	Digital Output (VOH/VOL) (Pullup resistance:10 k to 100 kΩ)	
VCC VREF	VCC voltage range 4.75 V (min) 5.0 V (typ.) 5.25 V (max) VREF voltage range 0 V to 3.6 V	
OSCM	OSCM frequency setting range 0.64 MHz (min) 1.12 MHz (typ.) 2.4 MHz (max)	
OUT_A+ OUT_A- OUT_B+ OUT_B- RS_A RS_B	VM power supply voltage range 6.5 V (min) to 44 V (max)	

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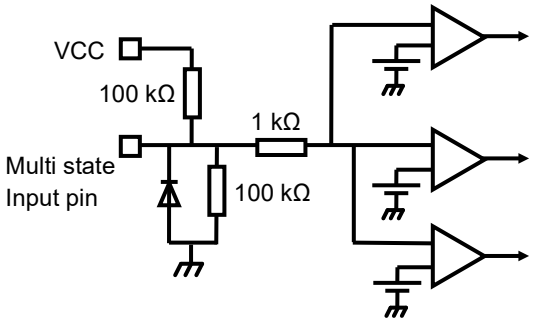
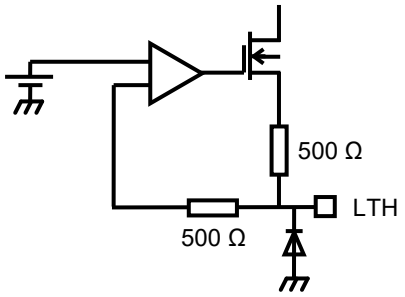
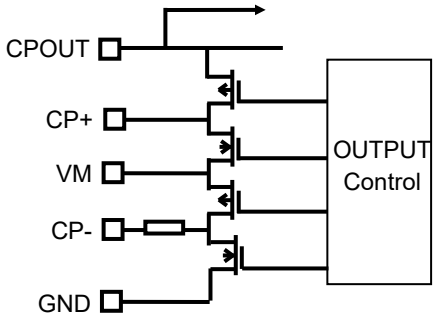
Pin name	IN/OUT signal	Equivalent circuit
CLIM1 FLIM BST	Multi state input pin voltage Connect to VCC Connect to GND Connect to VCC with 100 kΩ pull-up resistor Connect to GND with 100 kΩ pull-down resister (Resistor accuracy should be within ±20 %.)	
LTH	Connect to GND with 100 kΩ pull-down resistor (Resistance accuracy should be within ±20 %.)	
CPOUT CP+ CP-	VM power supply voltage range 6.5 V (min) to 44 V (max) OUTPUT pin voltage 11.2 V (min) to 48.7 V (max)	

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

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7. Interface Select Function

The interface can be selected between CLK mode and serial mode.

Table 7.1 Interface Select Function

IF_SEL pin input	Function
L	CLK mode
H	Serial mode

8. Functional Description 1 (for CLK mode when IF_SEL pin = L)

8.1. CLK Function

Each up-edge of the CLK signal will shift the motor's electrical angle per step.

Table 8.1 When EDG_SEL pin = L (Single Edge)

CLK pin input	Function
Up-edge	Shifts the electrical angle per step.
Down-edge	(State of the electrical angle does not change.)

Table 8.2 When EDG_SEL pin = H (Double Edge)

CLK pin input	Function
Up-edge	Shifts the electrical angle per step.
Down-edge	Shifts the electrical angle per step.

8.2. ENABLE Function

The ENABLE pin controls the ON and OFF of the stepping motor outputs. Motor operation starts and stops by setting H and L to the ENABLE pin. (When ENABLE pin is set to L (OFF), all of the MOSFETs turn off and become high impedance (hereafter, Hi-Z).)
Setting the ENABLE pin to L, and avoiding the motor to operate during VM power-on and power-off (i.e., outside of the operating voltage range) is recommended. Then, switch the ENABLE pin to H after the VM reaches the target voltage and becomes stable.

Table 8.3 ENABLE Function

ENABLE pin input	Function
L	OFF (High impedance mode, later omitted Hi-Z mode later)
H	ON (Normal operation mode)

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8.3. CW/CCW Function and the Output Pin Function (Output logic at the time of a charge start)

The CW/CCW pin controls the rotation direction of the motor. When set to H, the current of OUT_A is output first, with a phase difference of 90°. When set to L, the current of OUT_B is output first with a phase difference of 90°.

Table 8.4 CW/CCW Function and the Output Pin Function

CW/CCW pin input	OUT_x+	OUT_x-
L: Counter clockwise operation (CCW)	L	H
H: Clockwise operation (CW)	H	L

Note: x = A or B

8.4. Step Resolution Select Function

MODE 0, MODE1, and MODE2 pins control the step resolution. Pin levels of MODE0, MODE1, and MODE2 can be switched during operation. The following step current depends on the electrical angle.

Table 8.5 Step Resolution Select Function

MODE2 pin input	MODE1 pin input	MODE0 pin input	Function
L	L	L	Full step resolution
L	L	H	Half step resolution
L	H	L	Quarter step resolution
L	H	H	1/8 step resolution
H	L	L	1/16 step resolution
H	L	H	1/32 step resolution
H	H	L	1/64 step resolution
H	H	H	1/128 step resolution

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8.5. Timing Chart of Step Resolution Setting and Initial Angel

8.5.1. [Full step resolution]

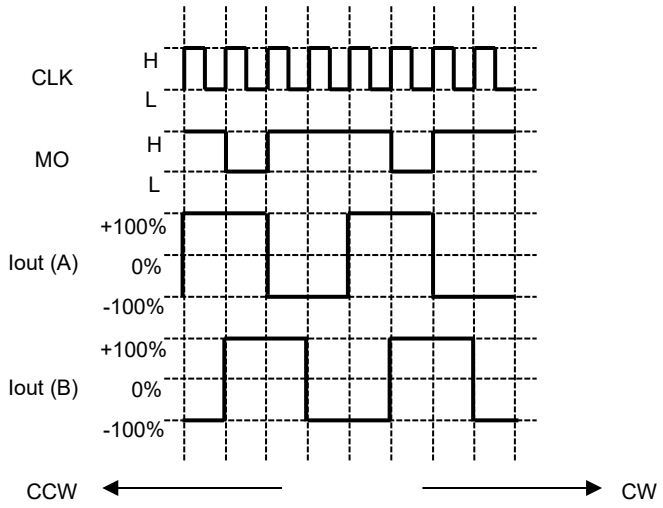

Figure 8.1 Full step resolution

8.5.2. [Half step resolution]

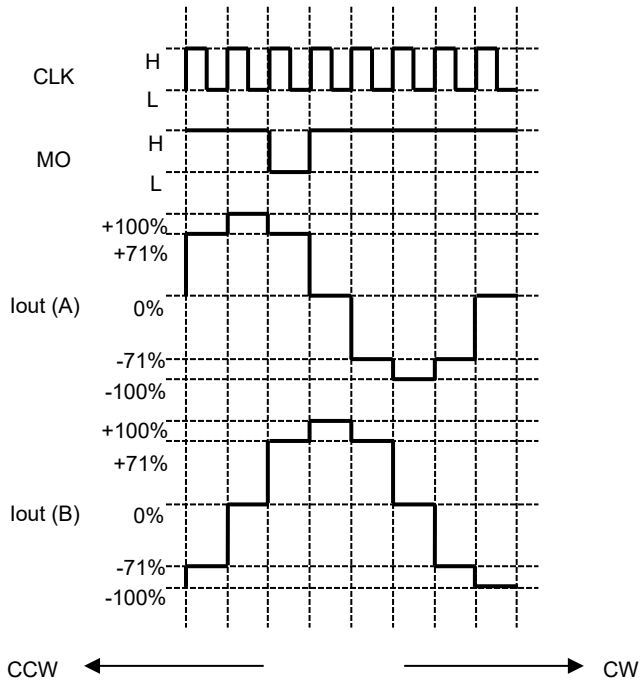

Figure 8.2 Half step resolution

Note: MO signal is shown in the above timing chart when MO pin is connected with a pull-up resistor to VCC.
Note: Timing charts may be simplified for explanatory purpose.

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8.5.3. [Quarter step resolution]

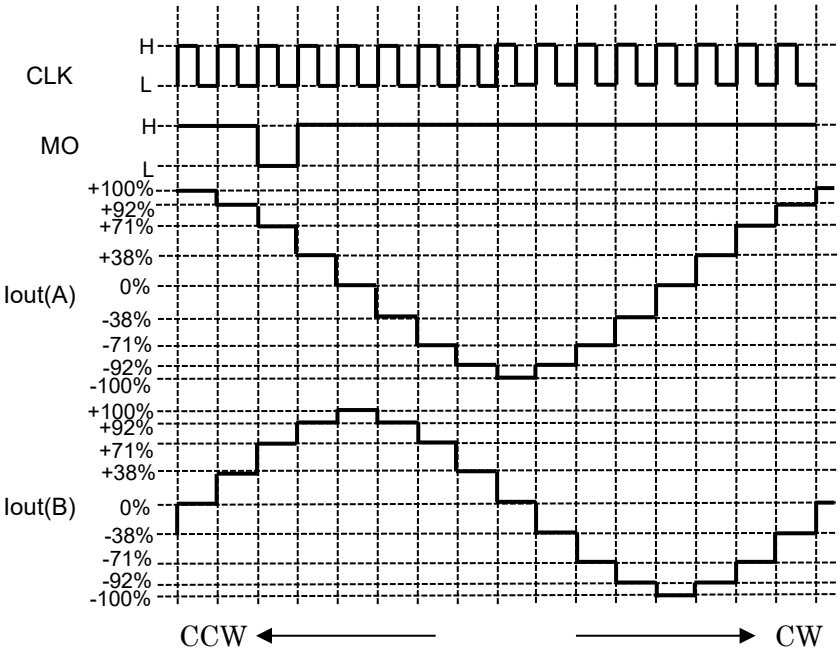

Figure 8.3 Quarter step resolution

Note: MO signal is shown in the above timing chart when MO pin is connected with a pull-up resistor to VCC.
Note: Timing charts may be simplified for explanatory purpose.

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8.5.4. [1/8 step resolution]

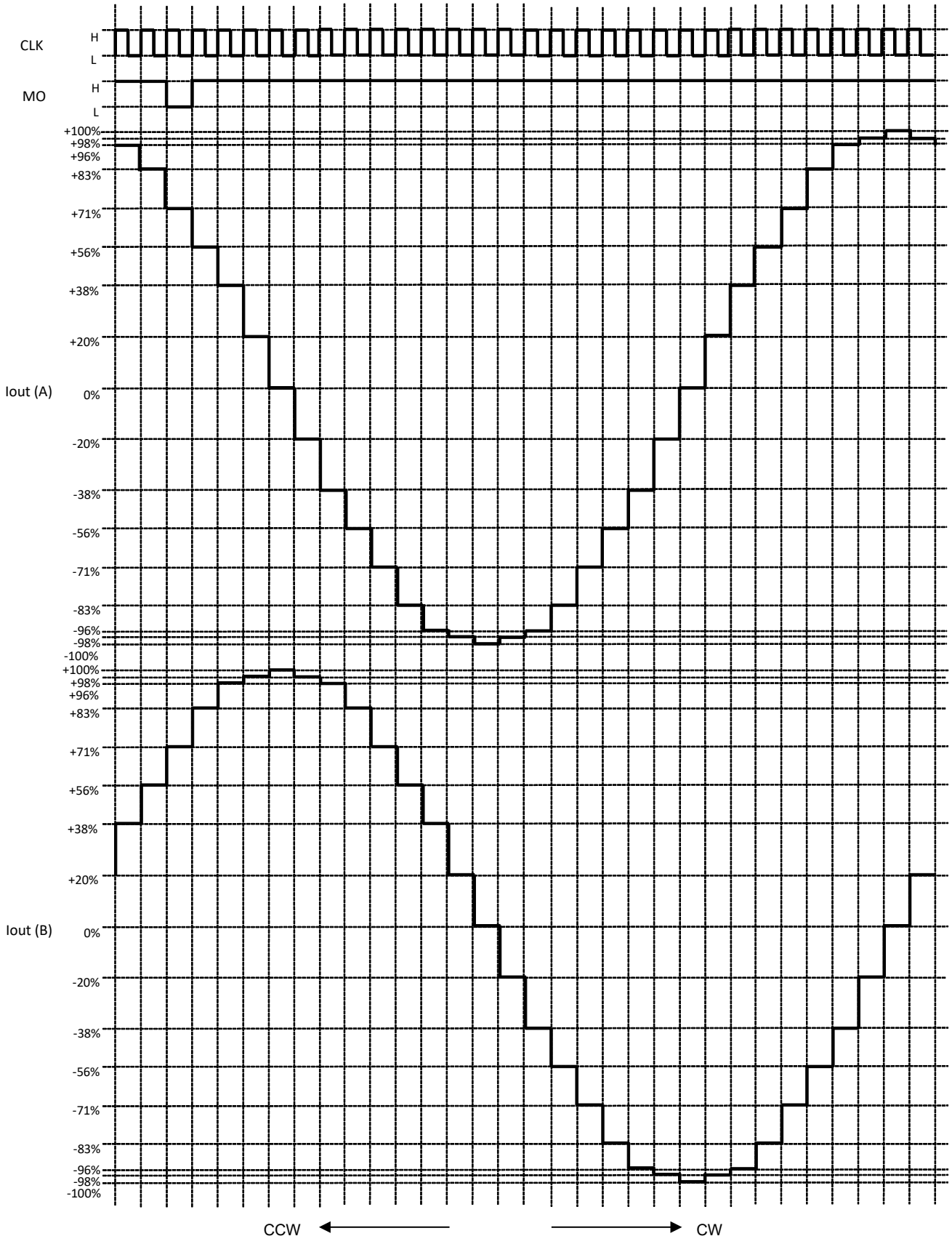

Figure 8.4 1/8 step resolution

Note: MO signal is shown in the above timing chart when MO pin is connected with a pull-up resistor to VCC.
Note: Timing charts may be simplified for explanatory purpose.

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8.5.5. [1/16 step resolution]

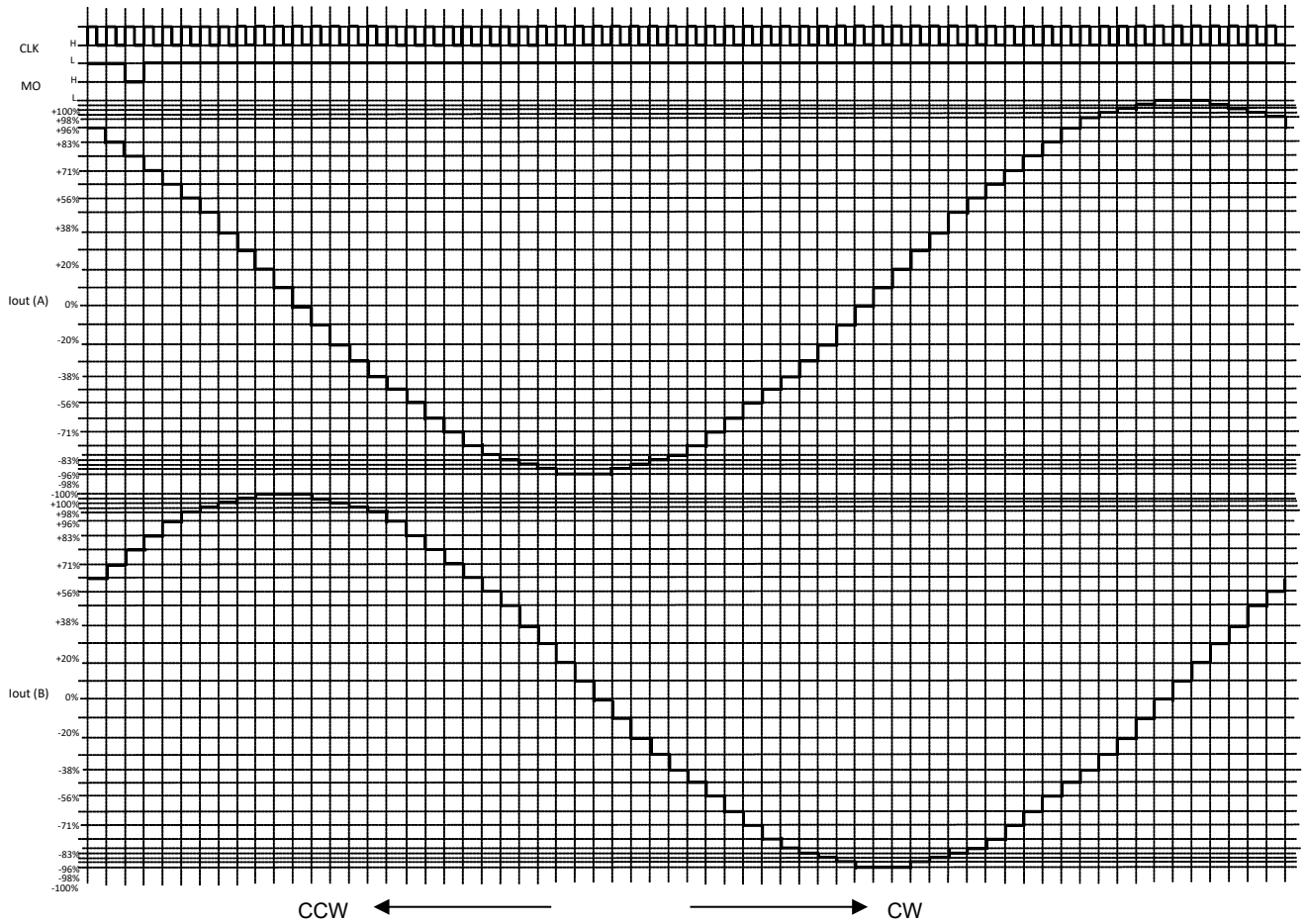

Figure 8.5 1/16 step resolution

Note: MO signal is shown in the above timing chart when MO pin is connected with a pull-up resistor to VCC.
Note: Timing charts may be simplified for explanatory purpose.

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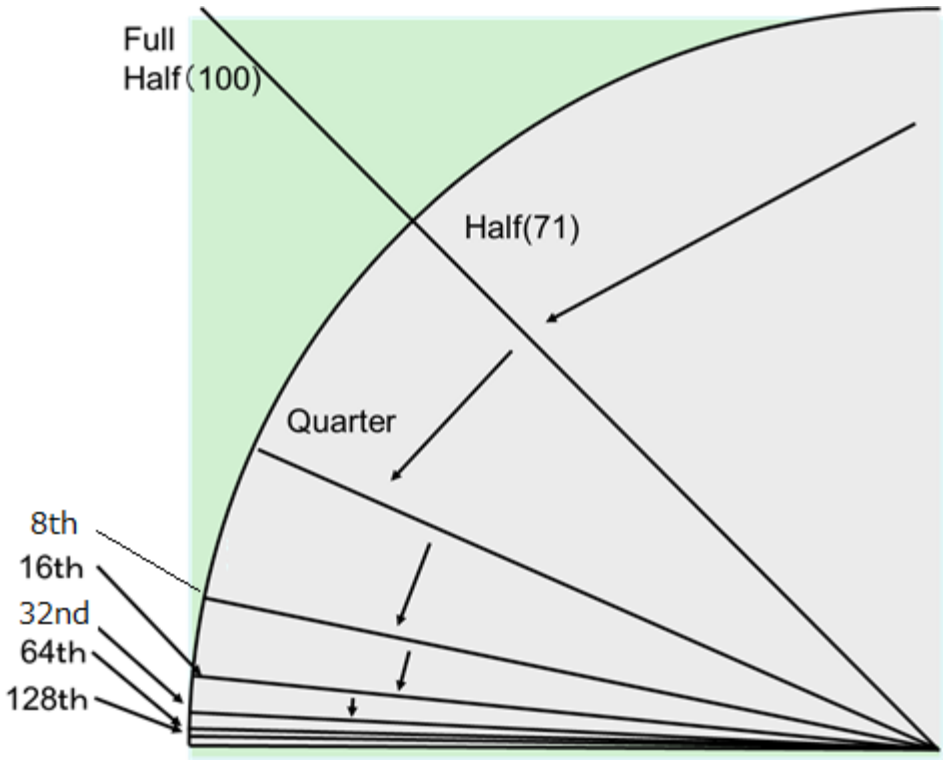

Figure 8.6 Step Resolution

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8.6. Step Setting and Current Percentage

Table 8.6 Step Setting and Current Percentage

Current (%)	Full	Half	Quarter	1/8	1/16	1/32	1/64	1/128
100%	Available	Available	Available	Available	Available	Available	Available	Available
99%					Available	Available	Available	Available
98%				Available	Available	Available	Available	Available
97%					Available	Available	Available	Available
96%				Available	Available	Available	Available	Available
95%							Available	Available
94%						Available	Available	Available
93%							Available	Available
92%			Available			Available	Available	Available
91%							Available	Available
90%					Available	Available	Available	Available
89%							Available	Available
88%						Available	Available	Available
87%							Available	Available
86%						Available	Available	Available
85%								Available
84%							Available	Available
83%				Available	Available	Available	Available	Available
82%							Available	Available
81%								Available
80%						Available	Available	Available
79%							Available	Available
78%								Available
77%					Available	Available	Available	Available
76%							Available	Available
75%								Available
74%						Available	Available	Available
73%								Available
72%							Available	Available
71%		Available	Available	Available	Available	Available	Available	Available
70%								Available
69%							Available	Available
68%								Available
67%						Available	Available	Available
66%								Available
65%							Available	Available
64%								Available
63%					Available	Available	Available	Available
62%							Available	Available
61%								Available
60%						Available	Available	Available

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Current (%)	Full	Half	Quarter	1/8	1/16	1/32	1/64	1/128
59%								Available
58%							Available	Available
57%								Available
56%				Available	Available	Available	Available	Available
55%								Available
53%							Available	Available
52%								Available
51%						Available	Available	Available
50%								Available
49%							Available	Available
48%								Available
47%					Available	Available	Available	Available
46%								Available
45%							Available	Available
44%								Available
43%						Available	Available	Available
42%								Available
41%							Available	Available
39%								Available
38%			Available	Available	Available	Available	Available	Available
37%								Available
36%							Available	Available
35%								Available
34%						Available	Available	Available
33%								Available
31%							Available	Available
30%								Available
29%					Available	Available	Available	Available
28%								Available
27%							Available	Available
25%						Available		Available
24%							Available	Available
23%								Available
22%							Available	Available
21%								Available
20%				Available	Available	Available	Available	Available
18%								Available
17%							Available	Available
16%								Available
15%						Available	Available	Available
13%								Available
12%							Available	Available
11%								Available
10%					Available	Available	Available	Available

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Current (%)	Full	Half	Quarter	1/8	1/16	1/32	1/64	1/128
9%								Available
7%							Available	Available
6%								Available
5%						Available	Available	Available
4%								Available
2%							Available	Available
1%								Available
0%		Available	Available	Available	Available	Available	Available	Available

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8.7. Step Resolution and Set Current

Table 8.7 Step Resolution and Set Current

STEP	1/128		1/64		1/32		1/16		1/8		1/4		1/2		Full	
—	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0		
θ1	100	1														
θ2	100	2	100	2												
θ3	100	4														
θ4	100	5	100	5	100	5										
θ5	100	6														
θ6	100	7	100	7												
θ7	100	9														
θ8	100	10	100	10	100	10	100	10								
θ9	99	11														
θ10	99	12	99	12												
θ11	99	13														
θ12	99	15	99	15	99	15										
θ13	99	16														
θ14	99	17	99	17												
θ15	98	18														
θ16	98	20	98	20	98	20	98	20	98	20						
θ17	98	21														
θ18	98	22	98	22												
θ19	97	23														
θ20	97	24	97	24	97	24										
θ21	97	25														
θ22	96	27	96	27												
θ23	96	28														
θ24	96	29	96	29	96	29	96	29								
θ25	95	30														
θ26	95	31	95	31												
θ27	95	33														
θ28	94	34	94	34	94	34										
θ29	94	35														
θ30	93	36	93	36												
θ31	93	37														
θ32	92	38	92	38	92	38	92	38	92	38	92	38				
θ33	92	39														
θ34	91	41	91	41												
θ35	91	42														
θ36	90	43	90	43	90	43										
θ37	90	44														
θ38	89	45	89	45												

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STEP	1/128		1/64		1/32		1/16		1/8		1/4		1/2		Full	
—	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)
039	89	46														
040	88	47	88	47	88	47	88	47								
041	88	48														
042	87	49	87	49												
043	86	50														
044	86	51	86	51	86	51										
045	85	52														
046	84	53	84	53												
047	84	55														
048	83	56	83	56	83	56	83	56	83	56						
049	82	57														
050	82	58	82	58												
051	81	59														
052	80	60	80	60	80	60										
053	80	61														
054	79	62	79	62												
055	78	62														
056	77	63	77	63	77	63	77	63								
057	77	64														
058	76	65	76	65												
059	75	66														
060	74	67	74	67	74	67										
061	73	68														
062	72	69	72	69												
063	72	70														
064	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100
065	70	72														
066	69	72	69	72												
067	68	73														
068	67	74	67	74	67	74										
069	66	75														
070	65	76	65	76												
071	64	77														
072	63	77	63	77	63	77	63	77								
073	62	78														
074	62	79	62	79												
075	61	80														
076	60	80	60	80	60	80										
077	59	81														
078	58	82	58	82												
079	57	82														

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STEP	1/128		1/64		1/32		1/16		1/8		1/4		1/2		Full	
—	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)
θ80	56	83	56	83	56	83	56	83	56	83						
θ81	55	84														
θ82	53	84	53	84												
θ83	52	85														
θ84	51	86	51	86	51	86										
θ85	50	86														
θ86	49	87	49	87												
θ87	48	88														
θ88	47	88	47	88	47	88	47	88								
θ89	46	89														
θ90	45	89	45	89												
θ91	44	90														
θ92	43	90	43	90	43	90										
θ93	42	91														
θ94	41	91	41	91												
θ95	39	92														
θ96	38	92	38	92	38	92	38	92	38	92	38	92				
θ97	37	93														
θ98	36	93	36	93												
θ99	35	94														
θ100	34	94	34	94	34	94										
θ101	33	95														
θ102	31	95	31	95												
θ103	30	95														
θ104	29	96	29	96	29	96	29	96								
θ105	28	96														
θ106	27	96	27	96												
θ107	25	97														
θ108	24	97	24	97	24	97										
θ109	23	97														
θ110	22	98	22	98												
θ111	21	98														
θ112	20	98	20	98	20	98	20	98	20	98						
θ113	18	98														
θ114	17	99	17	99												
θ115	16	99														
θ116	15	99	15	99	15	99										
θ117	13	99														
θ118	12	99	12	99												
θ119	11	99														
θ120	10	100	10	100	10	100	10	100								

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STEP	1/128		1/64		1/32		1/16		1/8		1/4		1/2		Full	
—	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)	Ach (%)	Bch (%)
θ121	9	100														
θ122	7	100	7	100												
θ123	6	100														
θ124	5	100	5	100	5	100										
θ125	4	100														
θ126	2	100	2	100												
θ127	1	100														
θ128	0	100	0	100	0	100	0	100	0	100	0	100	0	100		

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8.8. RESET Function

The RESET pin initializes the internal electrical angle.

Table 8.8 RESET Function

RESET pin input	Function
L	Normal operation mode
H	Sets the electrical angle to the initial condition.

Note: Digital filter of 0.625 μs (±20 %) is implemented to the RESET pin.

The current for each channel (while RESET pin is applied) is shown in the table below. MO pin will show L at this time.

Table 8.9 Phase current at RESET

Step resolution setting	Ach current setting	Bch current setting	Default electrical angle
Full step	100%	100%	45°
Half step	71%	71%	45°
Quarter step	71%	71%	45°
1/8 step	71%	71%	45°
1/16 step	71%	71%	45°
1/32 step	71%	71%	45°
1/64 step	71%	71%	45°
1/128 step	71%	71%	45°

8.9. Torque Function

By using this pin, it is possible to switch the motor torque setting.

Table 8.10 Torque Function

TORQE2 pin input	TORQE1 pin input	TORQE0 pin input	Function
L	L	L	Set torque: 100%
L	L	H	Set torque: 85%
L	H	L	Set torque: 70%
L	H	H	Set torque: 60%
H	L	L	Set torque: 50%
H	L	H	Set torque: 40%
H	H	L	Set torque: 25%
H	H	H	Set torque: 10%

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8.10. CLK Edge Function

CLK edge function can select the CLK signal's rising edge or the CLK edge's dual (up and down).

Table 8.11 CLK Edge Function

EDG_SEL pin input	Function
L	Single edge (Only Up Edge of CLK Signal)
H	Dual edge (Up and Down edge)

8.11. RS Function

RS function can select either ACDS mode or external sense RS resistor mode.

Table 8.12 RS Function

RS_SEL pin input	Function
L	ACDS (RS resistor less) mode
H	External sense RS resistor mode

Note: PCB board should be designed according to RS Function. When using ACDS mode, RS_x pins should be connected to GND. When using External sense RS resistor mode, the sense resistor should be connected between RS_x pin and GND. (x = A or B)

8.12. Gain Function

Gain function can change Vref(gain). Vref(gain) can be selected either 1/5 or 1/10.

Table 8.13 Gain Function

GAIN_SEL pin input	Function
L	Set Vref(gain) to 1/5
H	Set Vref(gain) to 1/10

8.13. Selectable Mixed Decay Function

The Selectable Mixed Decay can adjust the current regeneration amount during the period of current regeneration (Decay) using pins.
Though the Mixed Decay is determined by controlling 2 different types of decay (Fast Decay and Slow Decay), this function enables the user to select the ratio of the Mixed Decay using MDT0 and MDT1 pin. (2bit, 4 function)

Table 8.14 Selectable Mixed Decay Function

MDT1 pin input	MDT0 pin input	Function
L	L	Fast Decay: 37.5% (Fast Decay = OSCM × 6)
L	H	Fast Decay: 50% (Fast Decay = OSCM × 8)
H	L	Fast Decay only
H	H	ADMD

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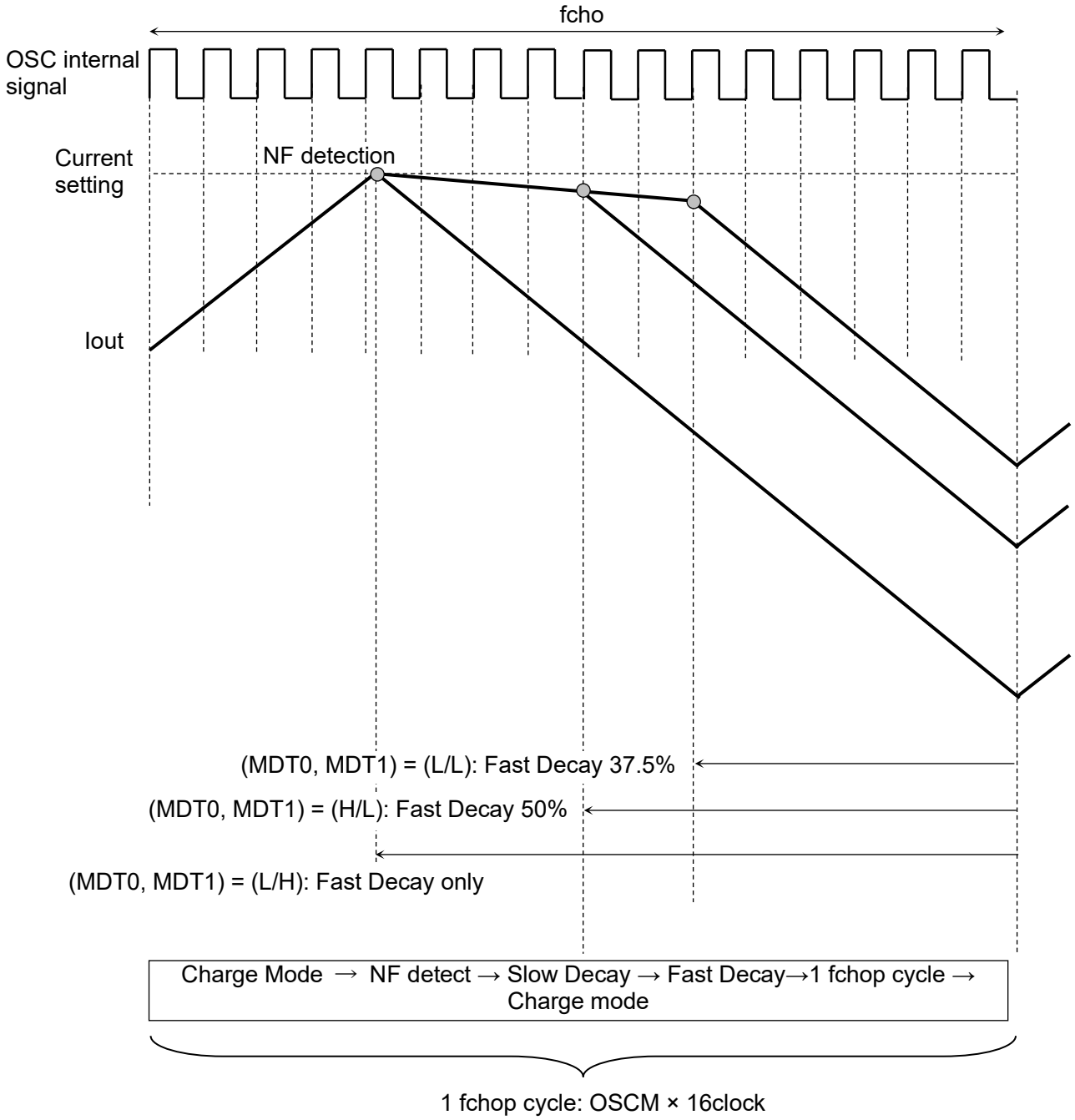

Figure 8.7 Selectable Mixed Decay Function

Note: Timing charts may be simplified for explanatory purpose.

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8.14. Mixed Decay Waveform (Current Waveform)

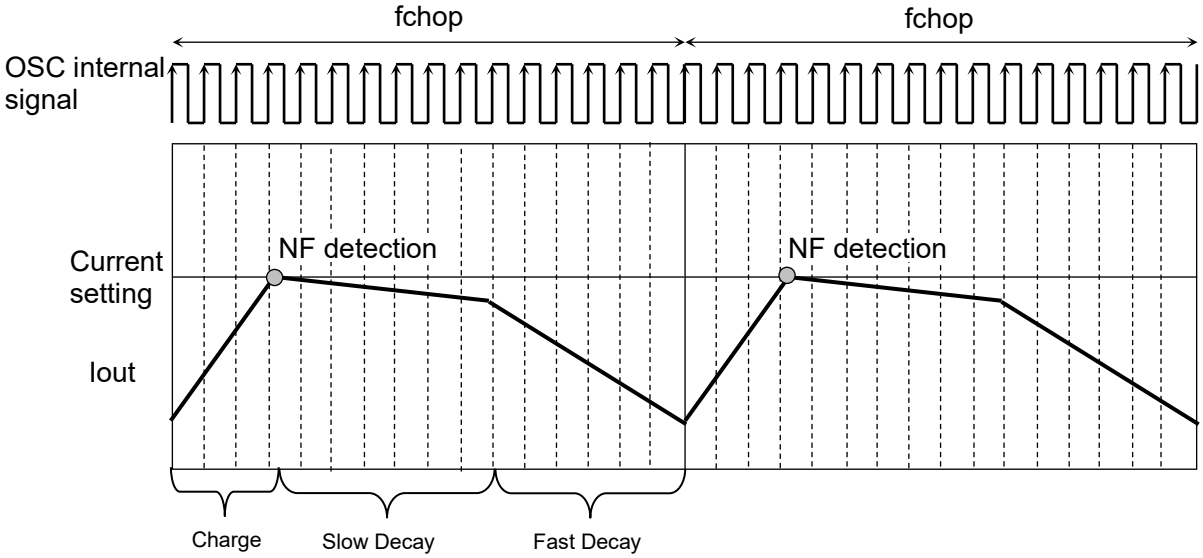

Figure 8.8 Mixed Decay Waveform (Current Waveform)

Note: Timing charts may be simplified for explanatory purpose.

8.14.1. Constant Current PWM Function and Timings

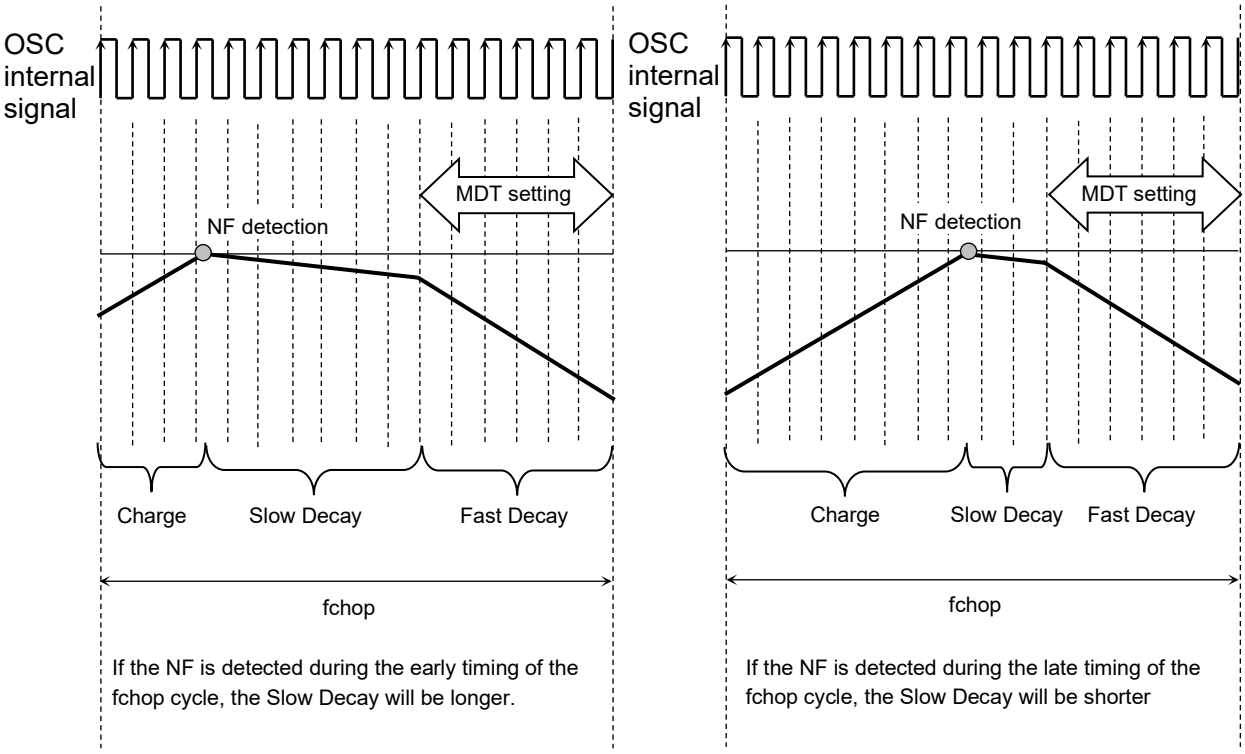

Figure 8.9 Constant Current PWM Function and Timings

The Charge period is determined by the operating status.
Therefore, the NF detect timing with in the chopping cycle will change. If NF is detected in the early period of the fchop cycle, the Slow Decay will be longer. If NF is detected in the late period of the fchop cycle, the Slow Decay will be shorter, as shown above.

Note: The chopping cycle is determined as: fchop - (Charge + Fast decay) = Slow Decay
(Fast Decay ratio can be changed by MDT0 pin and MDT1 pin setting.)
Note: Timing charts may be simplified for explanatory purpose.

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8.14.2. Constant Current PWM Function and Timing

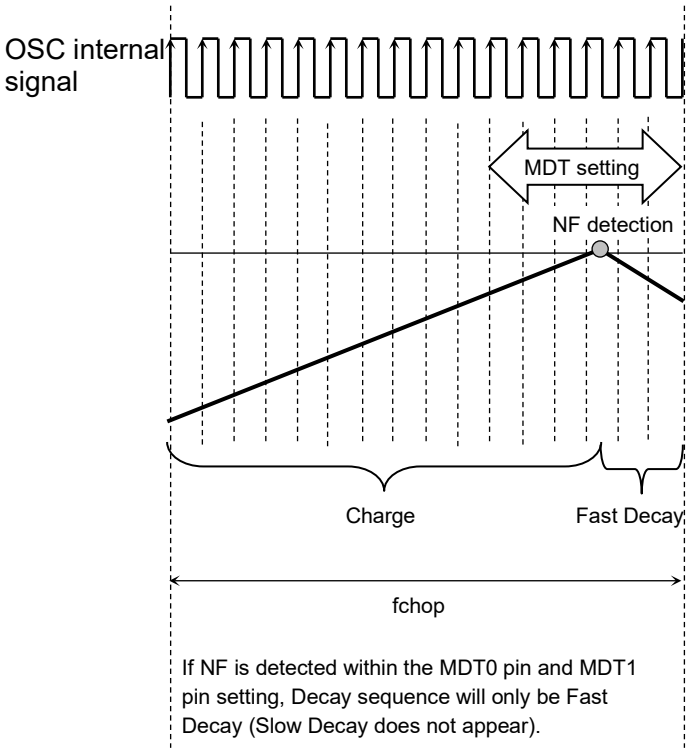

Figure 8.10 Constant Current PWM Function and Timing

Note: Timing charts may be simplified for explanatory purpose.

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8.15. Mixed Decay current waveform

8.15.1. When the next current step is higher:

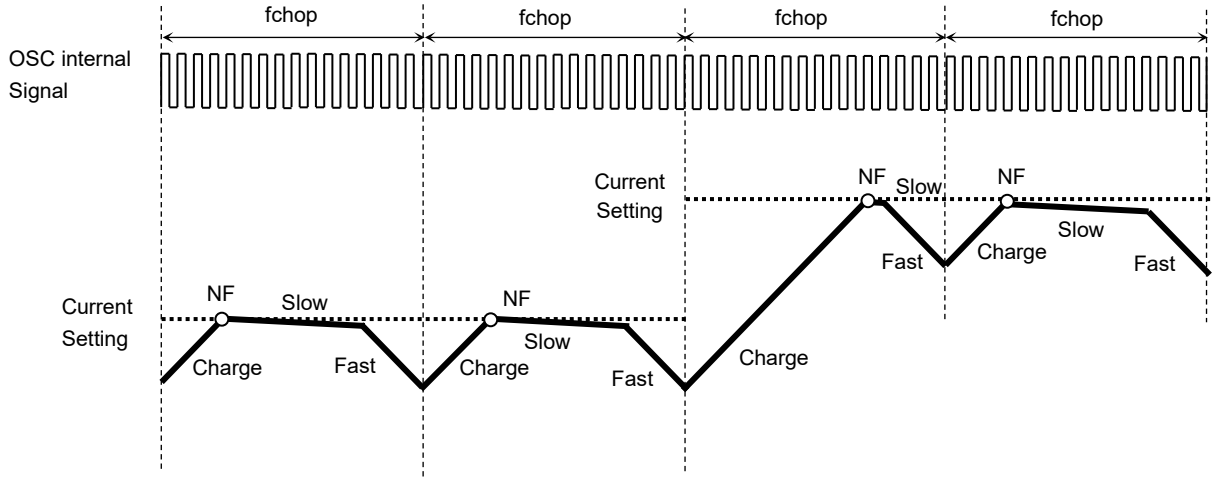

Figure 8.11 When the next current step is higher

8.15.2. When Charge Period is More Than 1 fchop Cycle:

When the Charge period is longer than fchop cycle, the Charge period extends until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence goes on to decay mode.

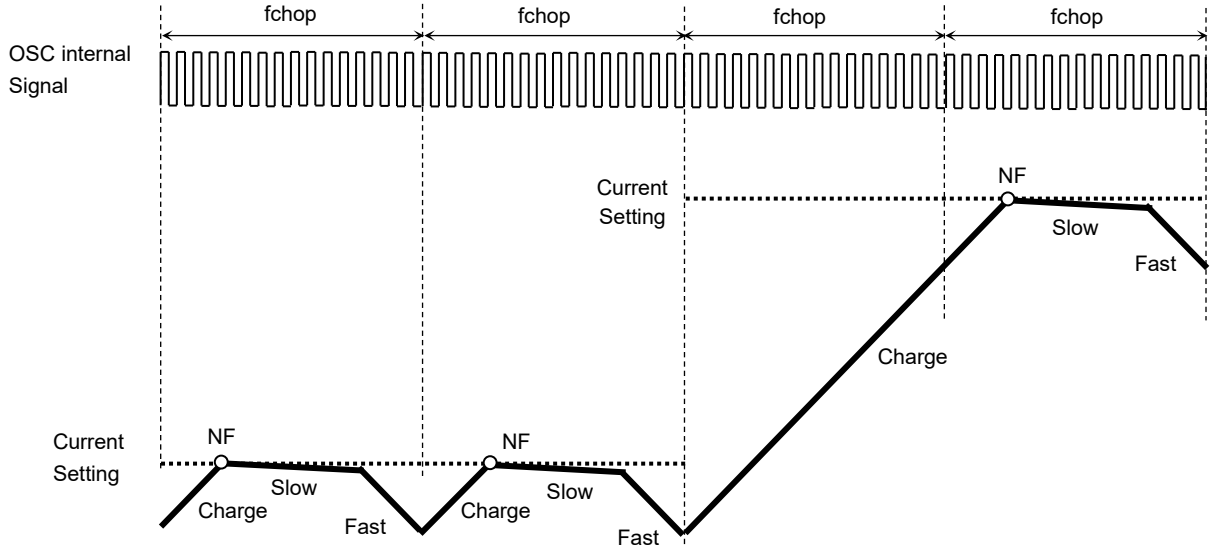

Figure 8.12 When Charge Period is More Than 1 fchop Cycle

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8.15.3. When the Next Current Step is Lower:

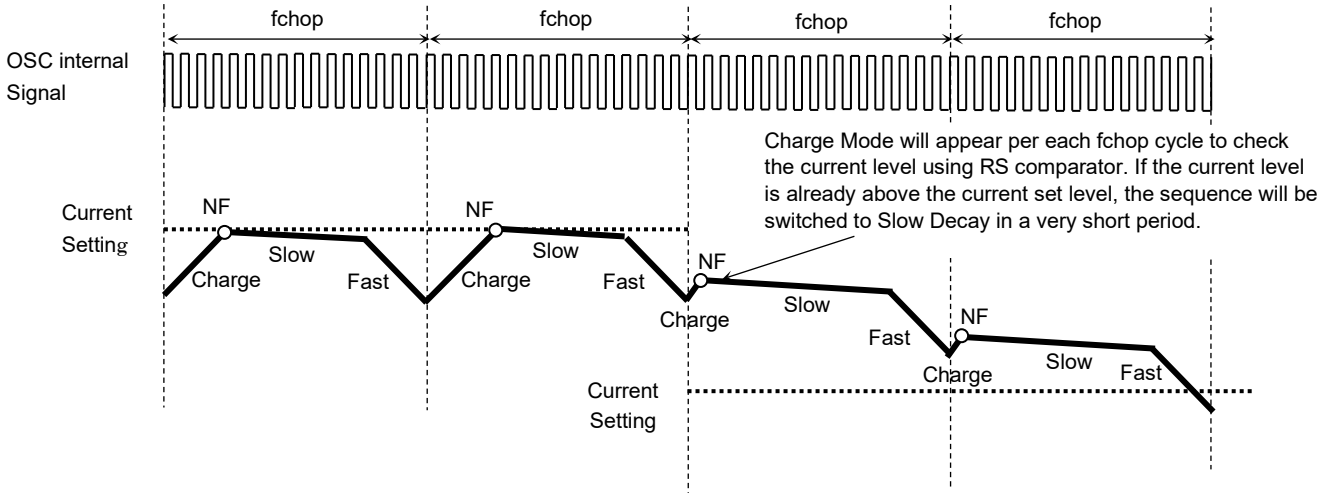

Figure 8.13 When the Next Current Step is Lower

Note: Timing charts may be simplified for explanatory purpose.

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8.16. ADMD (Advanced Dynamic Mixed Decay) Constant Current Control (MDT0 pin = H, MDT1 pin = H)

TB67S128FTG supports the Advanced Dynamic Mixed Decay (ADMD) which monitors both charge and discharge current during constant current PWM.
The basic sequence of the ADMD is as shown below.

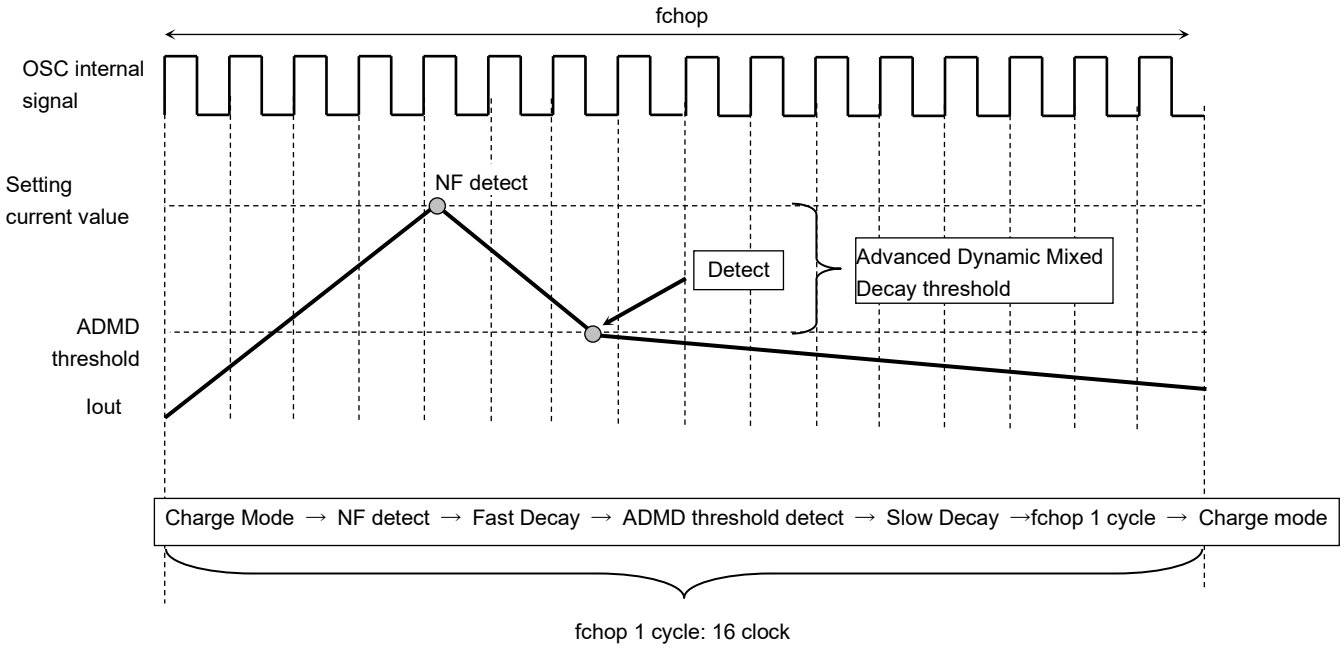

Figure 8.14 ADMD (Advanced Dynamic Mixed Decay) Constant Current Control

Note: Timing charts may be simplified for explanatory purpose.

8.16.1. Auto Decay Mode Current Waveform 1

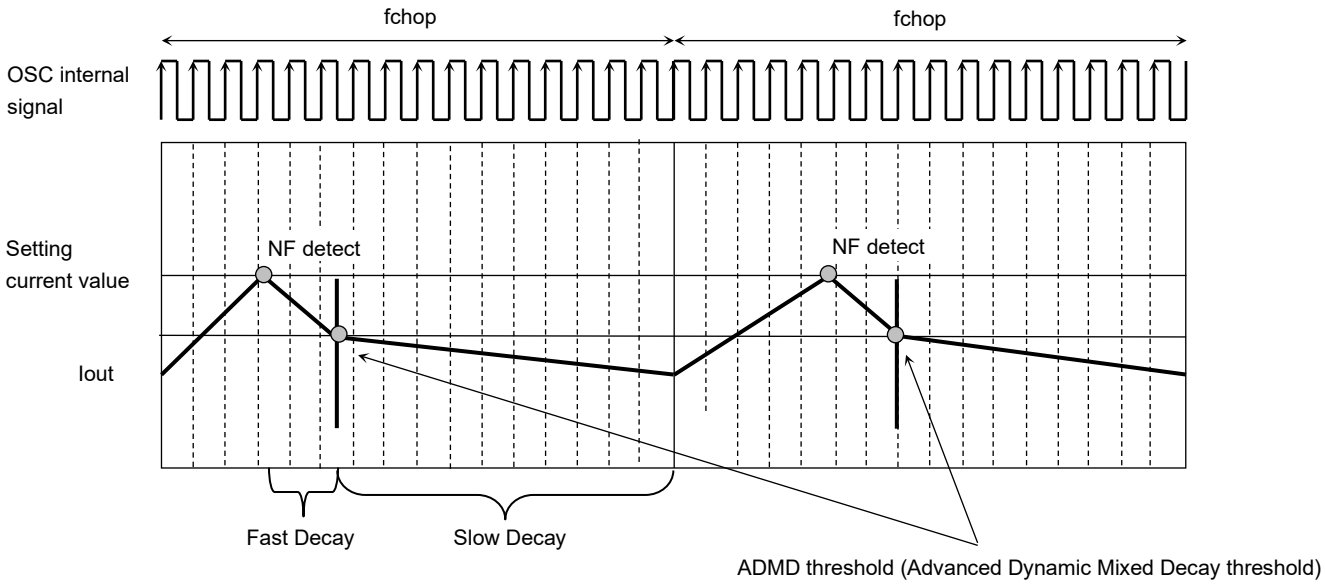

Figure 8.15 Auto Decay Mode Current Waveform 1

Note: Timing charts may be simplified for explanatory purpose.

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8.16.2. Auto Decay Mode Current Waveform 2

8.16.2.1. When the Next Current Step is Higher:

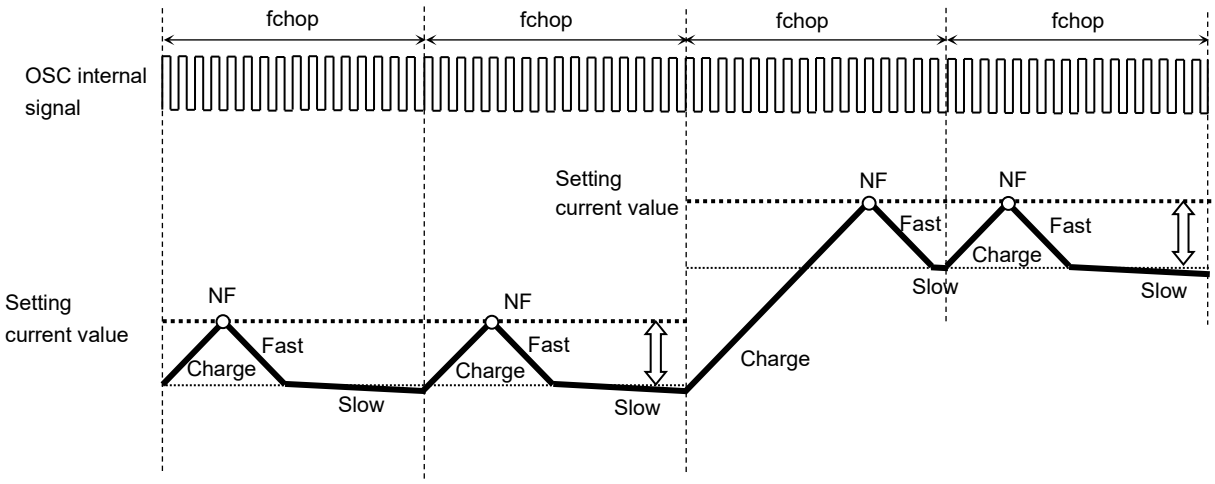

Figure 8.16 When the Next Current Step is Higher

8.16.2.2. When Charge Period is More Than 1 fchop Cycle:

When the Charge period is longer than fchop cycle, the Charge period will be extended until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence will go on to decay mode.

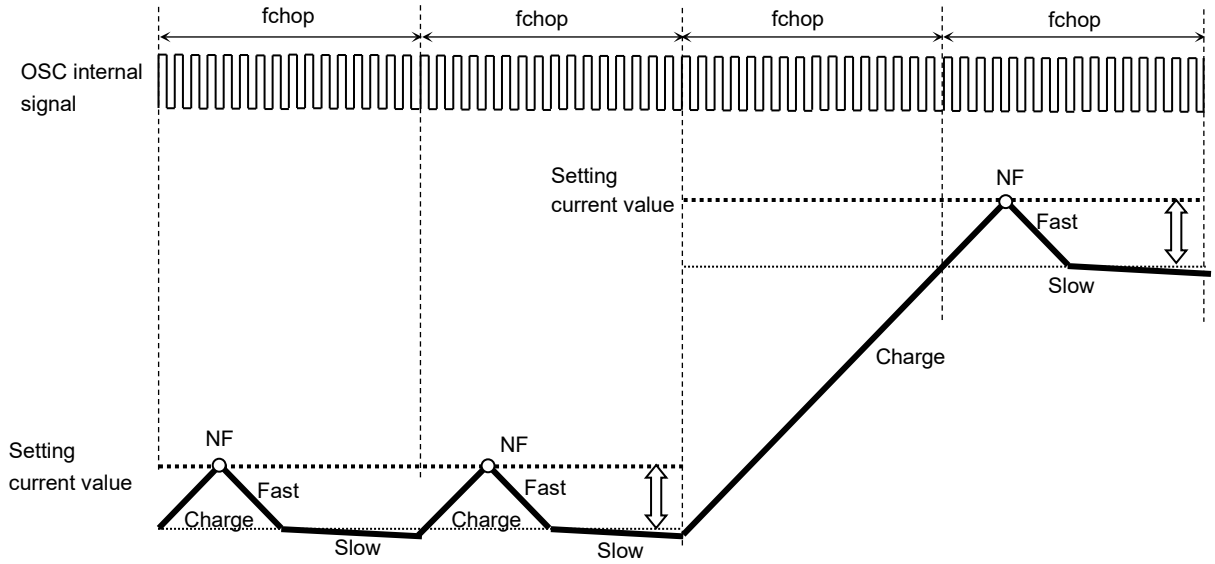

Figure 8.17 When Charge Period is More Than 1 fchop Cycle

Note: Timing charts may be simplified for explanatory purpose.

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8.16.2.3. When the Next Current Step is Lower:

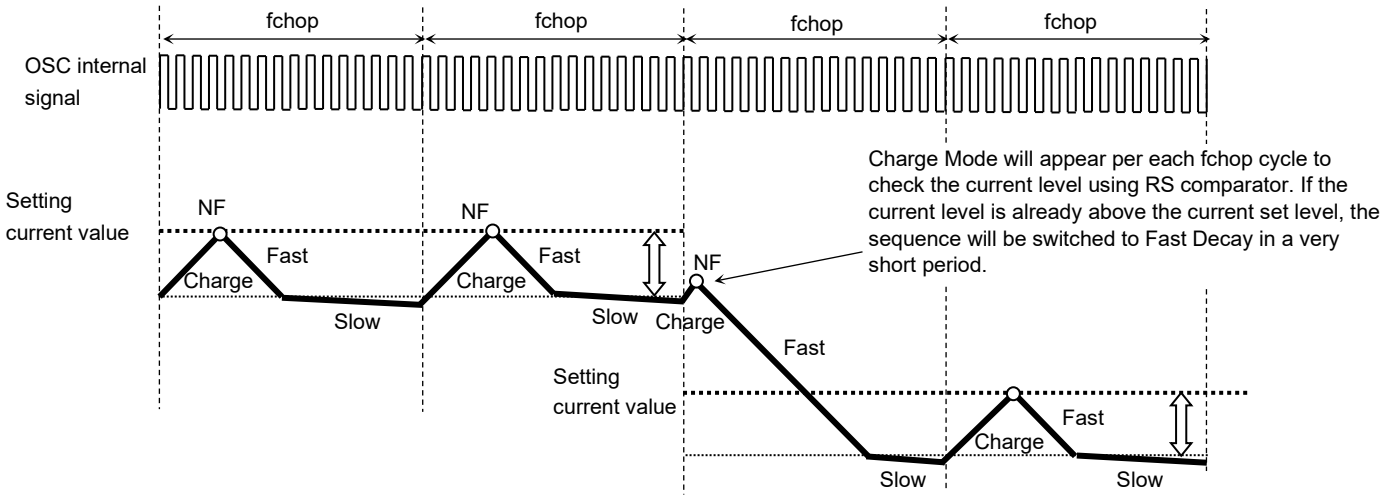

Figure 8.18 When the Next Current Step is Lower

8.16.2.4. When the Fast Continues Past 1 fchop Cycle (the motor current not reaching the ADMD threshold during 1 fchop cycle)

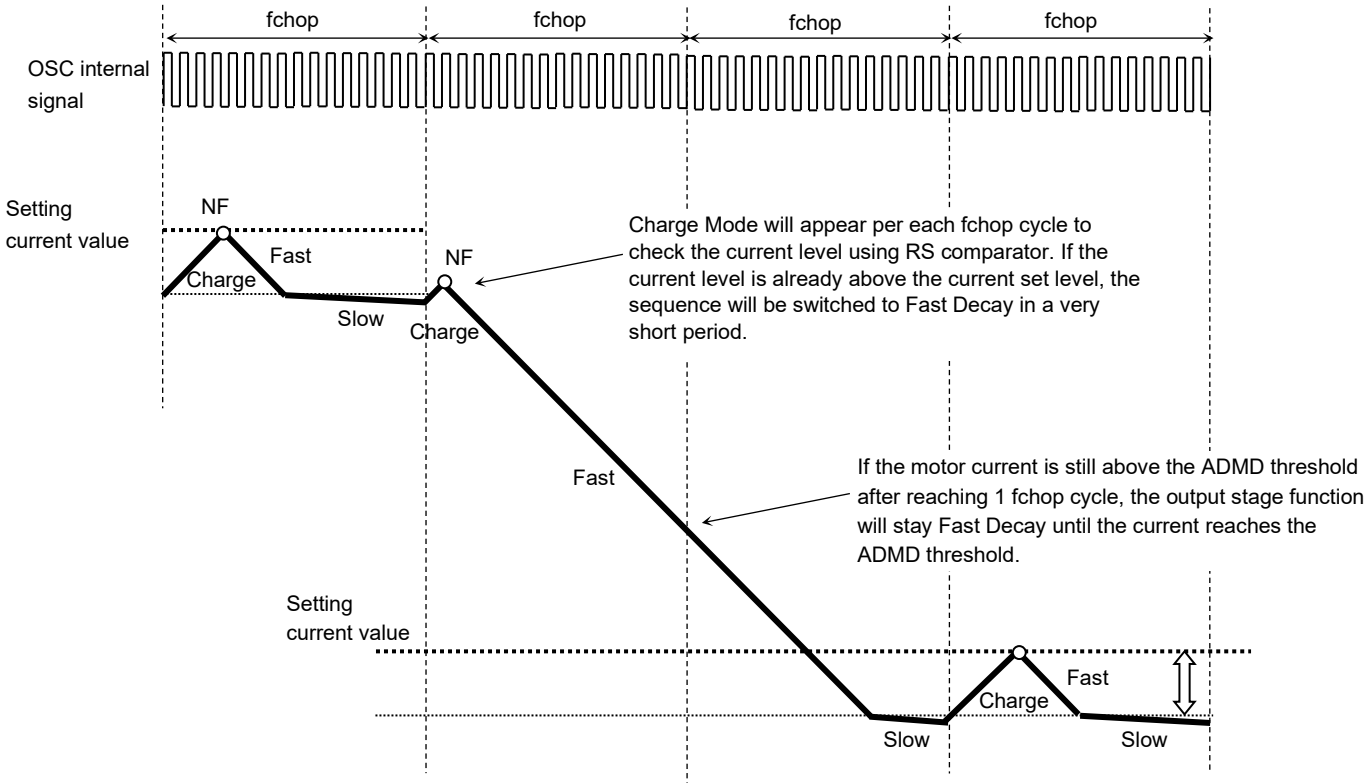

Figure 8.19 When the Fast Continues Past 1 fchop Cycle (the motor current not reaching the ADMD threshold during 1 fchop cycle)

Note: Timing charts may be simplified for explanatory purpose.

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9. Functional Description 2 (for Serial mode when IF_SEL pin = H)

When IF_SEL pin = H, the interface is serial mode. It performs setting and motor control in the following 32-bit format.
When BANK_EN pin is L, initial setting is performed. When the BANK_EN pin is H, the motor is controlled.
For the motor control, each current value is set in the serial setting, and the output is updated to the set current value at the timing of the LATCH signal.

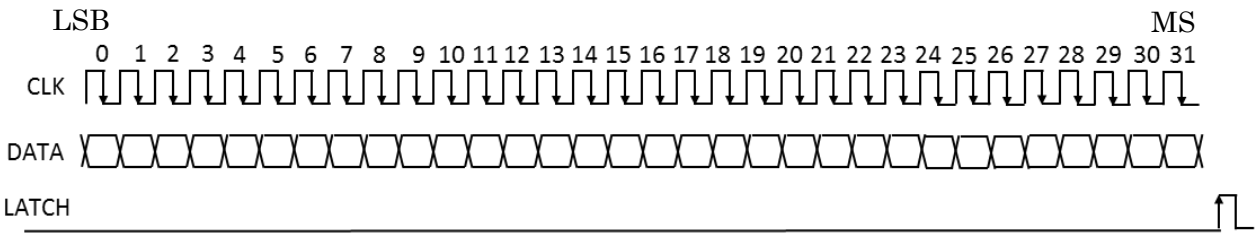

Figure 9.1 LATCH signal timing

Table 9.1 BANK_EN = L: Initial setting

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	AGC	CLIM 0	CLIM 1	CLIM 2	FLIM 0	FLIM 1	BST0	BST1	0	0	RS_ SEL	GAIN _SEL	0	0

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: The data which has a same name as a pin name in CLK mode performs as same as the pin in CLK mode.

Table 9.2 BANK_EN = H: Motor controlling

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	TOR QE0	TOR QE1	TOR QE2	0	MDT _A0	MDT _A1	PHA	CA0	CA1	CA2	CA3	CA4	CA5	CA6

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
CA7	CA8	CA9	MDT _B0	MDT _B1	PHB	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9

Note: Every issuing a command, the current setting transfers by one step.

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9.1. Registers When BANK_EN pin = H

The registers when BANK_EN pin = H are shown below.

9.1.1. PHx (x = A and B)

The polality of the output current can be selected by PHx register for each channels.

Table 9.3 PHx (x = A and B)

PHx register setting	Function
L	Setting the direction of the output current to minus
H	Setting the direction of the output current to plus

9.1.2. Cx0 to Cx9 (x = A or B)

The output of each channel's DAC for current limitation can be set by Cx0 to Cx9.
The relation between Setting DAC and the output current (Iout) are shonw below.

A) External Sense Resistor mode

$$\mathrm{Iout\ (max)} = \mathrm{Vref(gain)} \times \frac{\mathrm{Vref\ (V)}}{\mathrm{RS\ (\Omega)}} \times \frac{\mathrm{Cx[9:0]}}{1023}$$

$$\times \text{Setting torque by the torque function (\%)}$$

(x = A or B)

B) RS Resistor Less Mode (ACDS)

$\mathrm{Vref(gain)} = \frac{1}{5}\ (\mathrm{typ.})$ (when GAIN_SEL pin = L)

Iout (max) = $1.56 \times \mathrm{Vref\ (V)} \times \frac{\mathrm{Cx[9:0]}}{1023} \times$ Setting torque by the torque function (%)

$\mathrm{Vref(gain)} = \frac{1}{10}\ (\mathrm{typ.})$ (when GAIN_SEL pin= H)

Iout (max) = $0.78 \times \mathrm{Vref\ (V)} \times \frac{\mathrm{Cx[9:0]}}{1023} \times$ Setting torque by the torque function (%)

(x = A or B)

9.1.3. TORQE[0:2]

The motor torque can be set by TORQE[0:2].

Table 9.4 TORQE[0:2]

TORQE2	TORQE1	TORQE0	Function
0	0	0	Set torque:100%
0	0	1	Set torque: 85%
0	1	0	Set torque: 70%
0	1	1	Set torque: 60%
1	0	0	Set torque: 50%
1	0	1	Set torque: 40%
1	1	0	Set torque: 25%
1	1	1	Set torque: 10%

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9.1.4. MDT_x[0:1] (x = A or B)

The Selectable Mixed Decay can adjust the current regeneration amount during the period of current regeneration (Decay).

Table 9.5 MDT_x[0:1] (x = A or B)

MDT_x1	MDT_x0	Function
0	0	Fast Decay: 37.5% (Fast Decay = OSCM × 6)
0	1	Fast Decay: 50% (Fast Decay = OSCM × 8)
1	0	Fast Decay only
1	1	ADMD

9.1.5. RS_SEL

RS_SEL can select either ACDS mode or external sense RS resistor mode.

Table 9.6 RS_SEL

RS_SEL	Function
L	ACDS (RS resistor less) mode
H	External sense RS resistor mode

Note: PCB board should be designed according to RS Function. When using ACDS mode, RS_x pins should be connected to GND. When using External sense RS resistor mode, the sense resistor should be connected between RS_x pin and GND. (x = A or B)

9.1.6. GAIN_SEL

Vref(gain) can be selected either 1/5 or 1/10.

Table 9.7 GAIN_SEL

GAIN_SEL	Function
L	Vref(gain) = 1/5
H	Vref(gain) = 1/10

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9.2. Serial setting example when driving a motor

Serial setting example for motor operation is shown below.

1. Set the BANK_EN pin L. Initial setting for AGC, etc. is performed under this condition.
2. Then, set the BANK_EN pin H and configure the motor control to turn on the output transistors.
3. Transmit the 1st to 4th commands repeatedly by keeping the BANK_EN pin level H. The motor operates with full step resolution.

Table 9.8 Serial setting example when driving a motor

1st command

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1

2nd command

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1

3rd command

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1

4th command

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30	D31
1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1

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9.3. Stepping Motor Application Features (Anti-stall, RS resistor less PWM)

9.3.1. Active Gain Control (Anti-stall) Function

AGC pin will set the Active Gain Control to turn on or off. When this pin is set to H, the AGC is turned on, and when this pin is set to L, the AGC is turned off.
When the AGC is ON, the motor current is equal or more than the value by setting the VREF pin. TB67S128FTG reduces gradually the motor current depending on the load torque.
When the AGC is OFF, the motor current is the value by setting the VREF pin.

Table 9.9 AGC Function

AGC pin input	Function
L	AGC: OFF
H	AGC: ON

Note: Please do not change the AGC pin when TB67S128FTG is powered on.
Note: There is a built-in digital filter of 0.625 μs (±20%) for AGC pin.

Serial setting is shown below.

Table 9.10 AGC Function (Serial setting)

AGC bit	Function
0	AGC: OFF
1	AGC: ON

9.3.2. CLIM (AGC Bottom Current Limit) Function

When AGC is active, the motor current is reduced according to the load torque. The CLIM0 and CLIM1 pins set the lower threshold of the current threshold for AGC.
The CLIM0 pin is a 2 stated logic input, and the CLIM1 pin is a 4 stated logic input.

Table 9.11 CLIM Function

CLIM0 pin input	CLIM1 pin input	Function
L	VCC short	AGC bottom current limit: Iout × 60%
	VCC - 100 kΩ pull-up	AGC bottom current limit: Iout × 55%
	GND - 100 kΩ pull-down	AGC bottom current limit: Iout × 50%
	GND short	AGC bottom current limit: Iout × 45%
H	VCC short	AGC bottom current limit: Iout × 80%
	VCC - 100 kΩ pull-up	AGC bottom current limit: Iout × 75%
	GND - 100 kΩ pull-down	AGC bottom current limit: Iout × 70%
	GND short	AGC bottom current limit: Iout × 65%

Note: Pull-up and pull-down resistor tolerance should be kept within ±20 %.
Note: There is a built-in digital filter of 0.625 μs(±20%) for CLIM0 and CLIM1 pin.

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Serial setting is shown below.

Table 9.12 CLIM Function (Serial setting)

CLIM2 bit	CLIM1 bit	CLIM0 bit	Function
0	0	0	AGC bottom current limit: Iout × 45%
		1	AGC bottom current limit: Iout × 50%
	1	0	AGC bottom current limit: Iout × 55%
		1	AGC bottom current limit: Iout × 60%
1	0	0	AGC bottom current limit: Iout × 65%
		1	AGC bottom current limit: Iout × 70%
	1	0	AGC bottom current limit: Iout × 75%
		1	AGC bottom current limit: Iout × 80%

9.3.3. BOOST (Current Boost) Function

When AGC is active, the motor current is reduced according to the load torque. In this state, the BST pin sets the current boost level when the load torque increases. The BST pin is a 4 stated logic input pin.

Table 9.13 BOOST Function

BST pin input	Function
VCC short	Takes 5 steps maximum (Design value)
VCC - 100 kΩ pull-up	Takes 7 steps maximum (Design value)
GND - 100 kΩ pull-down	Takes 9 steps maximum (Design value)
GND short	Takes 11 steps maximum (Design value)

Note: Pull-up and pull-down resistor tolerance should be kept within ±20 %.
Note: There is a built-in digital filter of 0.625 μs(±20%) for BST pin.
Note: Current boost step is largest when BST pin is tied to VCC, and smallest when tied to the GND.

Serial setting is shown below.

Table 9.14 BOOST Function (Serial setting)

BST1 bit	BST0 bit	Function
0	0	Takes 11 steps maximum (Design value)
	1	Takes 9 steps maximum (Design value)
1	0	Takes 7 steps maximum (Design value)
	1	Takes 5 steps maximum (Design value)

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9.3.4. FLIM (AGC Frequency limit) function

The FLIM pin will set the lower frequency limit for the AGC to be active. The FLIM function is effective when the AGC is used to avoid the motor resonance frequency during ramp up.
The FLIM pin is a 4 stated logic input.

Table 9.15 FLIM function

FLIM pin input	Function
VCC short	Frequency limit: ON, AGC is invalid when fCLK is below 675 Hz
VCC - 100 kΩ pull-up	Frequency limit: ON, AGC is invalid when fCLK is below 450 Hz
GND - 100 kΩ pull-down	Frequency limit: ON, AGC is invalid when fCLK is below 225 Hz
GND short	FLIM: OFF

Note: Pull-up and pull-down resistor tolerance should be kept within ±20 %.
Note: There is a built-in digital filter of 0.625 μs(±20%) for FLIM pin.

The frequency (fCLK) shown above is for full step resolution. The frequency limit threshold will depend on the step resolution setting.

Table 9.16 Frequency limit threshold

FLIM pin input	1/1	1/2	1/4	1/8	1/16	1/32	1/64	1/128
VCC short	675 Hz	1.35 kHz	2.7 kHz	5.4 kHz	10.8 kHz	21.6 kHz	43.2 kHz	86.4 kHz
VCC - 100 kΩ pull-up	450 Hz	900 Hz	1.8 kHz	3.6 kHz	7.2 kHz	14.4 kHz	28.8 kHz	57.6 kHz
GND - 100 kΩ pull-down	225 Hz	450 Hz	900 Hz	1.8 kHz	3.6 kHz	7.2 kHz	14.4 kHz	28.8 kHz
GND short	FLIM: OFF							

Note: Pull-up and pull-down resistor tolerance should be kept within ±20 %.

Serial setting is shown below.

Table 9.17 FLIM function (Serial setting)

FLIM1 bit	FLIM0 bit	Function
0	0	FLIM: OFF
	1	Frequency limit: ON, AGC is invalid when fCLK is below 225 Hz
1	0	Frequency limit: ON, AGC is invalid when fCLK is below 450 Hz
	1	Frequency limit: ON, AGC is invalid when fCLK is below 675 Hz

Note: The fCLK in serial mode will depend on the step of output current which changes with Cx[0:9] and PHx setup

9.4. LTH (AGC detection threshold) function

The LTH pin sets the AGC detection threshold. Connect a 100 kΩ pull-down resistor to GND.

Table 9.18 LTH function

LTH	Function
GND - 100 kΩ pull-down	Sensitivity of the Anti-stall detection standard setting

Note: Pull-down resistor tolerance should be kept within ±20 %.

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10. Common Function (When CLK Mode and Serial Mode)

10.1. LO (Error detect flag output) Function

When an error detection function performs, the LO function outputs an error detection as a signal from LO0 and LO1 pins to the outside of TB67S128FTG.
The LO0 and LO1 pins are open-drain output pins. The LO0 and LO1 pins need to be pulled up to VCC level via 10 k to 100 kΩ resistor.
During regular operation, the level of LO0 and LO1 pins will stay Hi-Z (the internal MOSFET is OFF, the level of these pins are VCC level).
When the thermal shutdown (TSD), Over current (ISD), or motor load open (OPD) occurs, the LO0 and/or LO1 pins will become L (the internal MOSFET is ON).
When the error detection is released by reasserting the VM power supply or setting the device to STANDBY mode, the LO0 and LO1 pins show “normal status”.
Leave the LO0 and LO1 pins open when not using these functions.

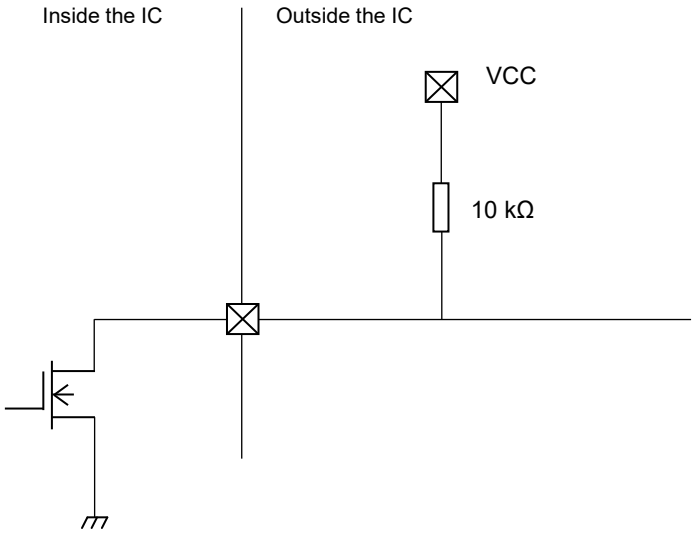

Figure 10.1 LO (Error detect flag output) Function

Note: This figure may be simplified for explanatory purpose.

Table 10.1 LO (Error detect flag output) Function

LO0 pin output	LO1 pin output	Function
Hi-Z	Hi-Z	Normal status (Normal operation)
Hi-Z	L	Detected motor load open (OPD)
L	Hi-Z	Detected over current (ISD)
L	L	Detected thermal shutdown (TSD)

10.2. STANDBY Function

It is possible to switch to Standby mode by switching this pin.

Table 10.2 STANDBY Function

STANDBY pin input	Function
L	Standby mode
H	Normal operation

Note: In STANDBY pin = L, an internal oscillating circuit and a motor output part are stopped. At this time, the motor cannot be driven.

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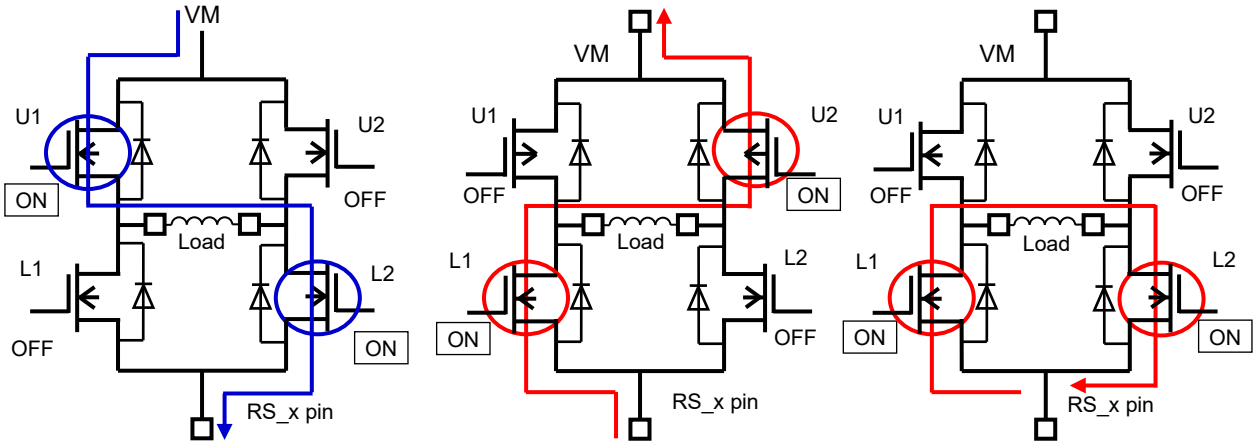
10.3. Output Transistor Function Mode



Charge mode
A current flow into the motor coil.

Fast mode
The energy of the motor coil is feed back to the power.

Slow mode
A current circulates around the motor coil and this device.

Note: x = A or B
Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

10.4. Output transistor function

Table 10.3 Output transistor function

MODE	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above.
If the current flows in the opposite direction, refer to the following table.

Table 10.4 Output transistor function (opposite direction)

MODE	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

This IC controls the motor current to be constant by changing 3 modes listed above automatically.

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10.5. Calculation of the Predefined Output Current

10.5.1. External Sense Resistor mode

For PWM constant-current control, this IC uses a clock generated by the OSCM oscillator.
The peak output current (Setting current value) can be set via the current-sensing resistor (RS) and the reference voltage (Vref), as follows:

$$\mathrm{Iout\ (max)} = \mathrm{Vref(gain)} \times \frac{\mathrm{Vref\ (V)}}{\mathrm{RS\ (\Omega)}}$$

Note: When GAIN_SEL pin = L, $\mathrm{Vref(gain)} = \frac{1}{5}\ (\mathrm{typ.})$. And When GAIN_SEL pin = H, $\mathrm{Vref(gain)} = \frac{1}{10}\ (\mathrm{typ.})$.

For example:

When Vref = 3.0 (V), RS = 0.22 Ω, Torque = 100% and $\mathrm{Vref(gain)} = \frac{1}{5}\ (\mathrm{typ.})$ (When GAIN_SEL pin = L), motor constant current (Setting current value) will be calculated by the following expressions.

$$\mathrm{Iout\ (max)} = \frac{1}{5} \times \frac{3\ (\mathrm{V})}{0.22\ (\Omega)} = 2.73\ \mathrm{A}$$

10.5.2. RS Resistor Less Mode (ACDS)

The Iout (max) will be calculated by the following expressions.

When $\mathrm{Vref(gain)} = \frac{1}{5}\ (\mathrm{typ.})$ (GAIN_SEL = L)
Iout (max) = 1.56 × Vref (V)

When $\mathrm{Vref(gain)} = \frac{1}{10}\ (\mathrm{typ.})$ (GAIN_SEL = H)
Iout (max) = 0.78 × Vref (V)

10.6. Calculation of the OSCM Oscillation Frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (fOSCM) and chopper frequency (fchop) can be calculated by the following expressions.

$$\mathrm{fOSCM} = \frac{1}{0.56 \times \{\mathrm{COSC} \times (\mathrm{ROSC} + 500)\}}$$

$$\mathrm{fchop} = \frac{\mathrm{fOSCM}}{16}$$

Note: COSC: Capacitor connected to OSCM pin, ROSC: Resistor connected to OSCM pin

For example:

When COSC = 270 pF and ROSC = 5.1 kΩ, fOSCM frequency will be calculated by following expressions.

$$\mathrm{fOSCM} = \frac{1}{0.56 \times \{270\ \mathrm{pF} \times (5.1\ \mathrm{k\Omega} + 500)\}} \approx 1.2\ (\mathrm{MHz})(\mathrm{typ.})$$

$$\mathrm{fchop} = \frac{\mathrm{fOSCM}}{16} = \frac{1.2\ (\mathrm{MHz})}{16} \approx 75\ (\mathrm{kHz})$$

If chopping frequency is raised, Rippl of current will become small and wave-like reproducibility will improve. However, the gate loss inside IC goes up and generation of heat becomes large.
By lowering chopping frequency, reduction in generation of heat is expectable. However, Rippl of current may become large.
It is a standard about 70 kHz. A setup in the range of 50k to 100 kHz is recommended.

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11. Absolute Maximum Ratings (Ta = 25°C)

Table 11.1 Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit	Remarks
Motor output voltage	Vout	50	V	—
Motor power supply (non active)	VM	50	V	STANDBY pin = L
Motor power supply (active)		-0.4 to 44	V	STANDBY pin = H
Motor output current	Iout	5.0	A	(Note1)
Charge pump voltage	VCPP	VM ± 6 V	V	STANDBY pin = H
	VCPM	VM ± 6 V	V	STANDBY pin = H
	VCPO	50	V	—
Internal Logic power supply	VCC	6.0	V	—
Logic input voltage	VIN(H)	6.0	V	—
	VIN(L)	-0.4	V	—
MO output voltage	VMO	6.0	V	—
LO0, LO1 output voltage	VLO	6.0	V	—
MO Inflow current	IMO	6.0	mA	—
LO0, LO1 Inflow current	ILO	6.0	mA	—
Power dissipation	P_D	1.2	W	(Note2)
Operating temperature	Topr	-40 to 85	°C	—
Storage temperature	Tstg	-55 to 150	°C	—
Junction temperature	Tj(max)	150	°C	—

Note1: Usually, the maximum current value at the time should use 70% or less of the absolute maximum ratings for a standard on thermal rating. The maximum output current may be further limited in view of thermal considerations, depending on ambient temperature and board conditions.

Note2: Device alone (Ta =25°C)
When Ta exceeds 25°C, it is necessary to do the derating with 9.6 mW/°C.

Ta: Ambient temperature
Topr: Ambient temperature while the IC is active
Tj: Junction temperature while the IC is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 120°C.

Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. TB67S128FTG does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

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12. Operating Ranges (Ta=-40 to 85°C)

Table 12.1 Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	6.5	24	44	V	—
Motor output current	Iout	—	3.0	5.0	A	(Note1)
Logic input voltage	VIN(H)	2.0	—	5.5	V	Logic input H Level
	VIN(L)	0	—	0.8	V	Logic input L Level
MO output pin voltage	VMO	—	3.3	5.0	V	—
LO0, LO1 output pin voltage	VLO	—	3.3	5.0	V	—
Clock input frequency	fCLK	—	—	200	kHz	—
Chopper frequency	fchop (range)	40	70	150	kHz	—
Vref input voltage	Vref	GND	2.0	3.6	V	—

Note1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (exciting mode, operating time, and so on), ambient temperature, and heat conditions (board condition and so on).

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13. Electrical Specifications

13.1. Electrical Specifications 1 (Ta = 25°C, VM = 24 V, unless otherwise specified)

Table 13.1 Electrical Specifications 1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage	HIGH	VIN(H)	Logic input (Note1)	2.0	—	5.5	V
	LOW	VIN(L)	Logic input (Note1)	0	—	0.8	V
Logic input hysteresis voltage		VIN(HYS)	Logic input (Note1)	100	—	300	mV
Logic input current	HIGH	IIN(H)	VIN(H) = 3.3 V	—	33	—	μA
	LOW	IIN(L)	VIN(L) = 0 V	—	—	1	μA
MO output pin voltage	LOW	VOL(MO)	IOL = 5 mA, output = L	—	0.2	0.5	V
LO0, LO1 output pin voltage	LOW	VOL(LO)	IOL = 5 mA, output = L	—	0.2	0.5	V
Current consumption		IM1	Output pins = open Standby mode	—	1.8	3.2	mA
		IM2	Output pins = open ENABLE pin = L in releasing Standby mode	—	5.5	8.6	mA
		IM3	Output pins = open Full step resolution	—	8.2	10.4	mA
Output leakage current	High side	IOH	VM = 44 V, Vout = 0 V	—	—	1	μA
	Low side	IOL	VM = Vout = 44 V	-1	—	—	μA
Motor current channel differential		ΔIout1	External Sense Resistor mode: VREF=3.3V, IOUT=3.0A setting RS Resistor Less Mode: VREF=1.92V, IOUT=3.0A setting (When GAIN_SEL= L) VREF=3.85V, IOUT=3.0A setting (When GAIN_SEL= H) (Note2)	0	—	5	%
Motor current setting accuracy		ΔIout2	External Sense Resistor mode: VREF=3.3V, IOUT=3.0A setting RS Resistor Less Mode: VREF=1.92V, IOUT=3.0A setting (When GAIN_SEL= L) VREF=3.85V, IOUT=3.0A setting (When GAIN_SEL= H)	-5	0	5	%
RS pin current		IRS	VRS = 0 V	0	—	10	μA
Motor output ON resistance (High side+Low side)		Ron(H+L)	Tj = 25°C, High side+Low side	—	0.25	0.35	Ω

Note: When the logic signal is applied to the device whilst the VM power supply is not asserted; the device is designed not to function, but for safe usage, please apply the logic signal after the VM power supply is asserted and the VM voltage reaches the proper operating range.

Note1: VIN(H) is defined as the VIN voltage that causes the outputs (OUT_A+ pin, OUT_A- pin, OUT_B+ pin, OUT_B- pin) to change when a pin under test is gradually raised from 0 V.VIN(L) is defined as the VIN voltage that causes the outputs (OUT_A+ pin, OUT_A- pin, OUT_B+ pin, OUT_B- pin) to change when the pin is then gradually lowered. The difference between VIN(H) and VIN(L) is defined as the VIN(HYS).

Note2: Motor current channel differential satisfies the following equation.
The absolute value of the difference in output current settings between any two channels [A] ≤ average of the output setting current values × output current error (Maximum) [A]

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13.2. Electrical Specifications 2 (Ta =25°C, VM = 24 V, unless otherwise specified)

Table 13.2 Electrical Specifications 2

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Vref input current	Iref	Vref = 2.0 V	—	0	1	μA
VCC voltage	VCC	ICC = 5.0 mA	4.75	5	5.25	V
VCC current	ICC	VCC = 5.0 V	—	2.5	5	mA
Vref gain rate	Vref(gain)	Vref = 2.0 V GAIN_SEL pin = L	1/5.2	1/5	1/4.8	—
Thermal shutdown (TSD) threshold (Note1)	TjTSD	—	145	160	175	°C
VM recovery voltage	VMR	—	5.7	6	6.3	V
Over current detection (ISD) threshold (Note2)	ISD	—	5.7	7.2	10	A

Note1: About TSD

When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection. Once the TSD circuit is triggered, the device will be set to standby mode, and can be cleared by reasserting the VM power source, or setting the MODE pins to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

Note2: About ISD

When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. Once the ISD circuit is triggered, the device keeps the output off until power-on reset (POR), is reasserted or the device is set to standby mode by MODE pins. For fail-safe, please insert a fuse to avoid secondary trouble.

13.2.1. Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that TB67S128FTG or other components will be damaged or fail due to the motor back-EMF.

13.2.2. Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

13.2.3. IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

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13.3. AC Electrical Specification (Ta = 25°C, VM = 24 V, 6.8 mH/5.7 Ω)

Table 13.3 AC Electrical Specification

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Inside filter of CLK input minimum High width	tCLK(H)	The CLK(H) minimum pulse width	300	—	—	ns
Inside filter of CLK input minimum Low width	tCLK(L)	The CLK(L) minimum pulse width	250	—	—	ns
Output transistor switching specific	tr	—	30	80	130	ns
	tf	—	40	90	140	ns
	tpLH(CLK)	CLK output	—	1000	—	ns
	tpHL(CLK)	CLK output	—	1500	—	ns
Analog noise blanking time	AtBLK	VM = 24 V, Iout = 3.0 A Analog tblank	250	400	550	ns
Oscillator frequency accuracy	ΔfOSCM	COSC = 270 pF, ROSC = 5.1 kΩ	-15	—	+15	%
Oscillator reference frequency	fOSCM	COSC= 270 pF, ROSC =5.1 kΩ	1020	1200	1380	kHz
Chopping frequency	fchop	Output: Active (Iout = 1.5 A), fOSC = 1200 kHz	—	75	—	kHz

AC Electrical Specification Timing chart

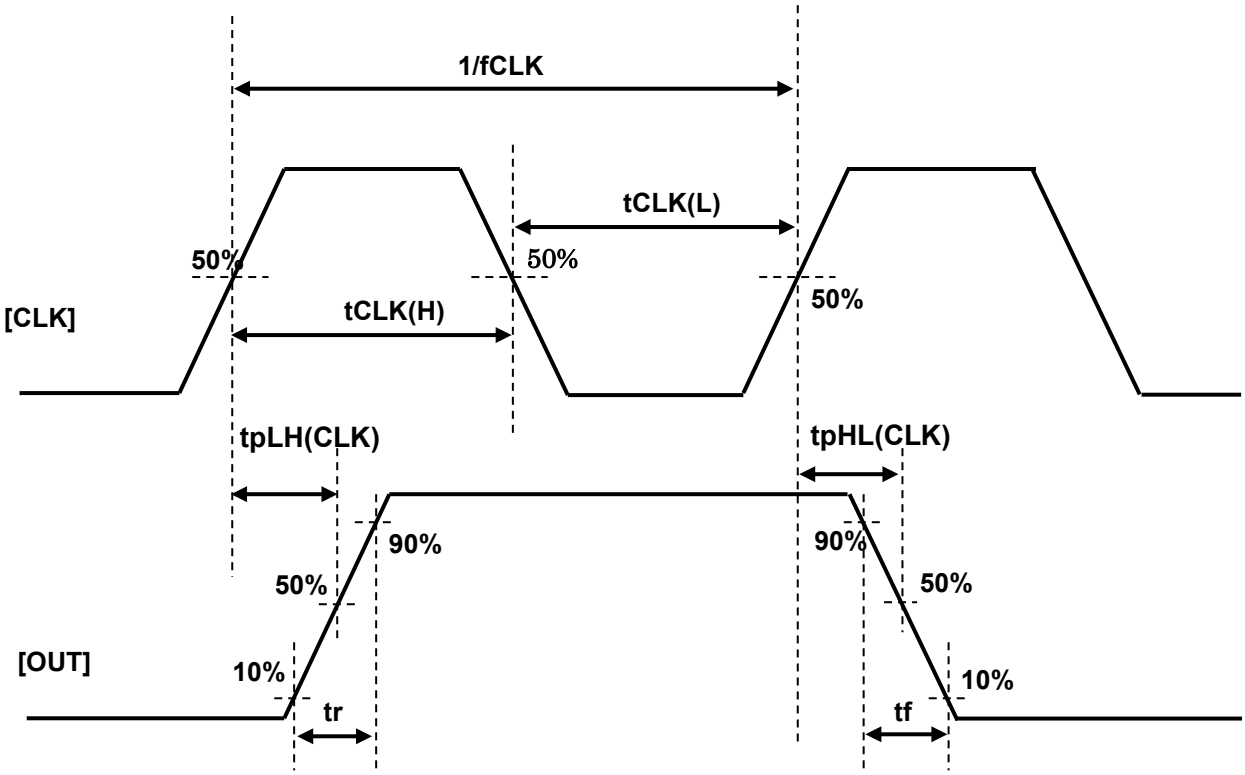

Figure 13.1 TB67S128FTG(Relationship between CLK and output)

Note: Timing charts may be simplified for explanatory purpose.

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13.4. Other AC Electrical Specification
(Ta = 25°C, VM = 24 V, unless otherwise specified)

Table 13.4 Other AC Electrical Specification

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	No. in Timing Chart
Serial CLK frequency	fSCLK	VIN = 3.3 V	1.0	—	25	MHz	—
CLK Cycle	tsCKW	VIH = 3.3 V, VIL = 0 V, tr = tf = 23 ns	46	—	—	ns	—
Minimum CLK pulse width	tw(CLK)	VIN = 3.3 V	40	—	—	ns	**1**
	twp(CLK)		20	—	—	ns	**2**
	twn(CLK)		20	—	—	ns	**3**
Minimum STROBE pulse width	tSTROBE	VIN = 3.3 V	40	—	—	ns	**4**
	tSTROBE(H)		20	—	—	ns	**5**
	tSTROBE(L)		20	—	—	ns	**6**
Data setup time	tsuSIN - CLK	VIN = 3.3 V	10	—	—	ns	**7**
	tsuST - CLK		10	—	—	ns	**8**
Data hold time	thSIN - CLK	VIN = 3.3 V	10	—	—	ns	**9**
	thST - CLK		10	—	—	ns	**10**

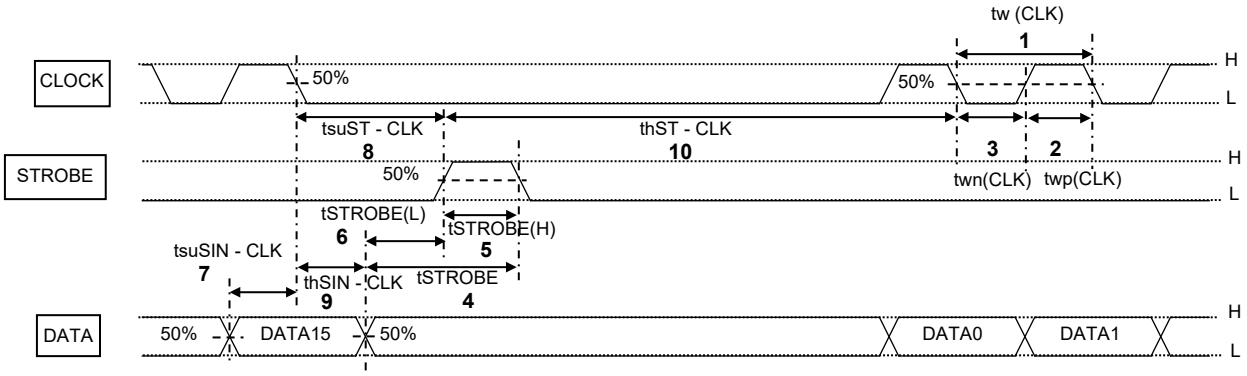

Figure 13.2 Timing chart of clock/ strobe/ data signals

Note: The CLK whose frequency is 1MHz or less may be used if the above conditions are met.

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14. Application Circuit Example (RS_SEL pin = H, IF_SEL pin = L)

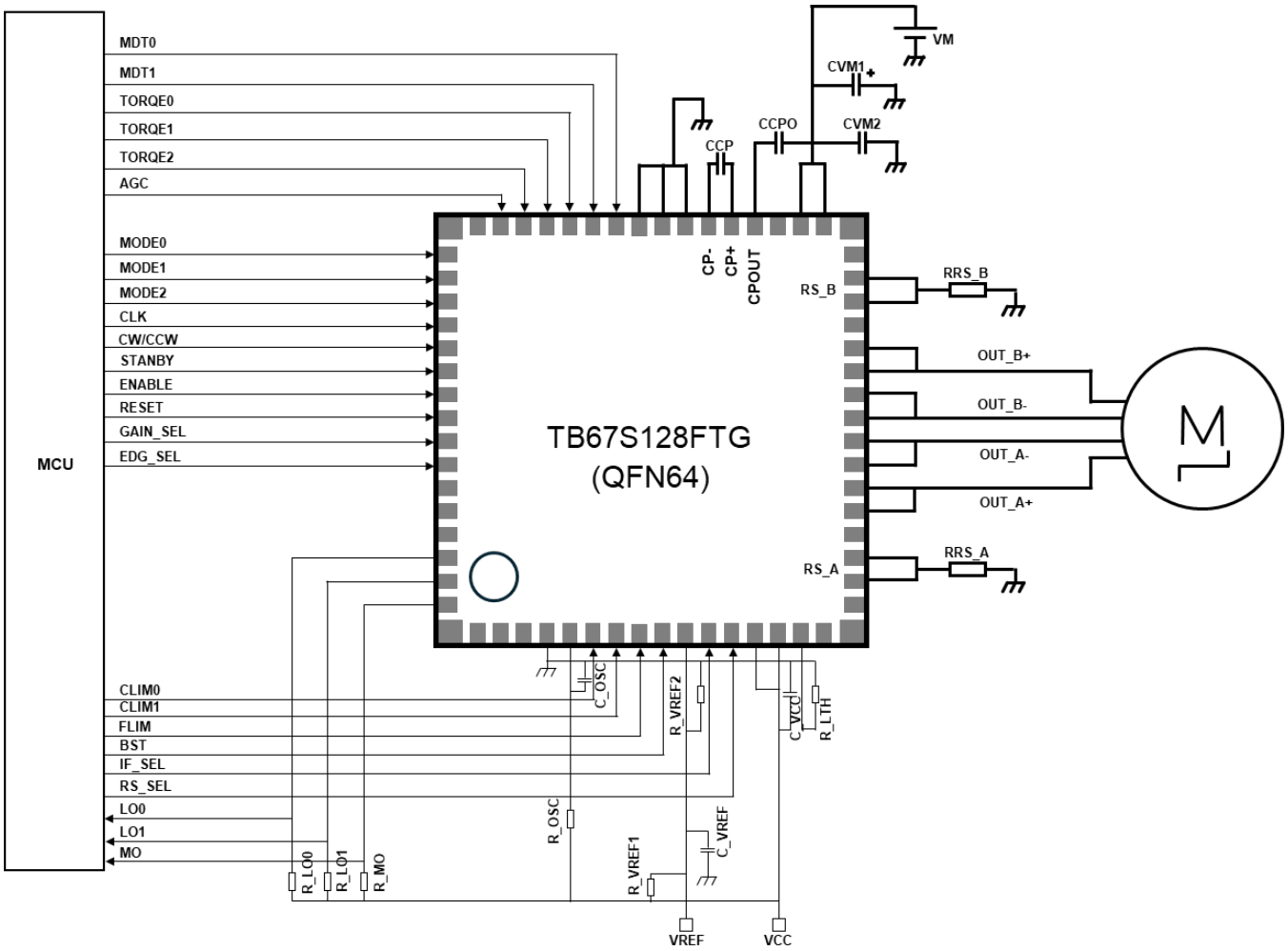

Figure 14.1 Application Circuit Example

Note: The application circuit shown in this document is provided for reference purposes only. The data for mass production are not guaranteed.

Table 14.1Component values (for reference only)

Part's symbol	Component	Reference component values
CVM1	Electrolytic capacitor	100 μF (CVM1 ≥ 10 μF)
CVM2	Ceramic capacitor	(0.1 μF)
CCP	Ceramic capacitor	0.022 μF
CCPO	Ceramic capacitor	0.22 μF
C_VCC	Ceramic capacitor	0.1 μF
R_OSC	Resistor	5.1 kΩ (1.8 kΩ to 8.2 kΩ)
C_OSC	Ceramic capacitor	270 pF
R_VREF1, R_VREF2	Resistor	Arbitrary (10 kΩ ≤ R_VREF1 + R_VREF2 ≤ 50 kΩ)
C_VREF	Ceramic capacitor	(0.1 μF)
R_MO	Resistor	10 kΩ (10 kΩ to 100 kΩ)
R_LO0, R_LO1	Resistor	10 kΩ (10 kΩ to 100 kΩ)
R_LTH	Resistor	100 kΩ

Note: Component values in above table are for reference only. Some components outside of the range can be adopted depending on the usage conditions.

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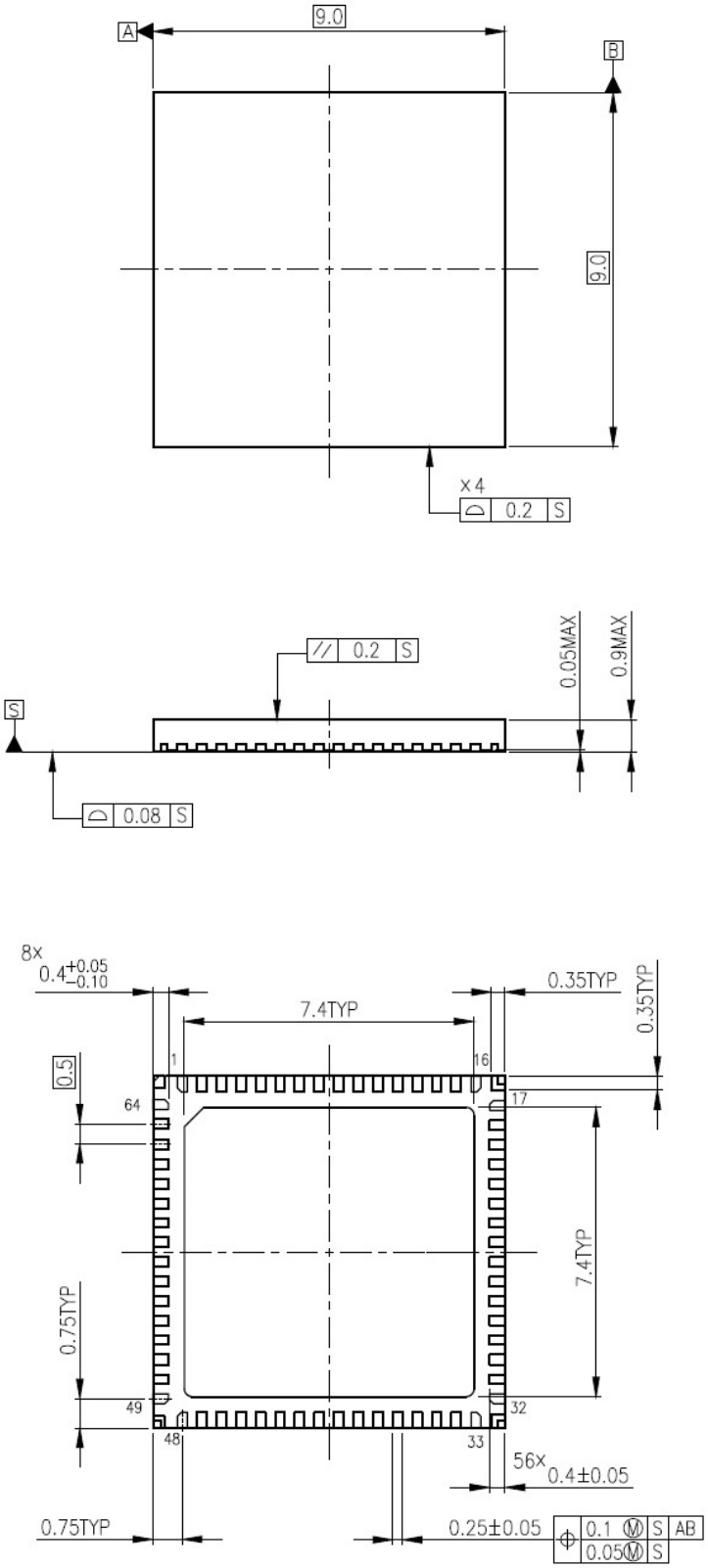
15. Package Dimensions

P-VQFN64-0909-0.50-006

Unit: mm



Weight: 0.229 g (typ.)

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Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

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Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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