

Quad-Channel Driver for Airbag Deployment

Check for Samples: [TPIC71004-Q1](#)

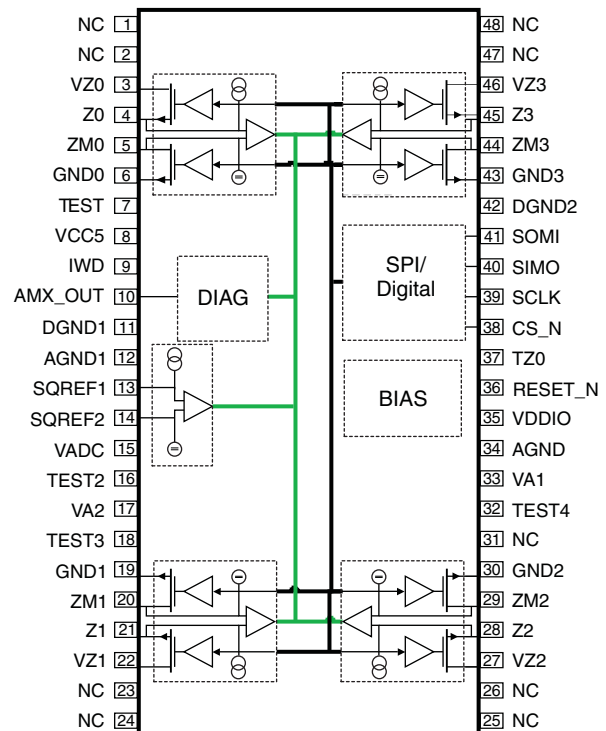
FEATURES

- Quad-Channel Squib Drivers for Airbag Application
- Loop Diagnostics Monitor and Reporting
- Two Logic Inputs Providing Independent Safety Logic for Enabling/Disabling Deployment
- Four Independent Thermally Protected High-Side Drivers That can Source Deployment or Diagnostic Current Level to Each Squib Load
- Four Independent Avalanche Voltage and Thermally Protected Low-Side Drivers That Can Sink Deployment or Diagnostic Current Level From Each Squib Load
- Each Output Capable of 1.2 A/1.75 A Firing Current for Typical 2 ms/0.5 ms
- SPI Slave Interface for Serial Bus Communication with Parity Check
- Firing VZx Voltage Range 10 V to 35 V, Transients up to 40 V
- Programmable Firing Time up to 8.2 ms
- Common Load Current Settings for All Deployment Loops, Using Registers
- Individual Firing Current Timer Limit Set for Each Deployment Loop, Using Registers
- Firing Current Timer to Monitor Firing Current Over Deployment Time for Each Deployment Loop
- Independent Switch Control for Both High- and Low-Side Switches
- Diagnostic Mode for Fault Checking
- Internal Fault Monitoring for Safe Operation
- A Multiplex-able Output Buffer for Analog Voltage Measurements
- Use of External Clamping devices on Squib Pins is Not Required to Protect the Deployment ASIC Against Substrate Injection Effects During Deployment Due to Dynamic Shorts to Ground

- An External Pin Connection to the Microprocessor ADC Supply for Ratio-metric Squib Resistance Measurement
- 40-V Pin Capability on All Pins (Except GNDx, AGND, DGND, VCC5, VDDIO, AMX_OUT)
- Operating Ambient Temperature Range: –40°C to 105°C
- Thermally Enhanced 48-Pin TSSOP DCA PowerPad™ Package

APPLICATIONS

- Squib Drivers for Airbag Application



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DESCRIPTION

The TPIC71004-Q1 is a quad channel squib driver for airbags deployment in automotive applications. Each channel consists of a high side and a low side switch with independent control logic for protection against inadvertent deployment. Both the high and the low side switches have internal current limits, over-temperature protection.

The IC registers are used for four channel configuration, control and status monitoring. To prevent inadvertent deployment, the high and the low side switches will be turned on only if the proper configuration sequence is used and multiple inputs to the deploy controller logic are at the correct level. The registers are programmed using a serial communications interface.

The maximum on time for each channel is limited by programmable Firing Time Out Timer to prevent excessive power dissipation. In addition, a current limit register is used to program the maximum current through the switches during a deployment. The current limitation on the low side switch is larger than the corresponding high side switch. During deployment, the low side switch will be full enhanced and operate with RDS_ON mode and the high side switch will be in current regulation mode.

The implemented diagnostic functions monitor deployment ASIC pin voltages to provide High Side switch test, Low Side switch test, squib resistance measurements, squib leakage measurement to battery, ground and between any squib channels. Furthermore, the squib leakage measurement is provided for both Zx and ZMx pins and does not require the squib load to be present to operate properly. Diagnostic information is communicated through the AMX_OUT pin (for analog signals) and SPI mapped status registers (for status signals latched in digital core).

The high-side and low-side squib drivers have a diagnostic level current limit and a deployment level current limit. The default current limit for high-side and low-side squib drivers is the diagnostic level current limit. The high-side switch deployment current limit for all high-side drivers can be set to either 1.2 A min or 1.75 A min (see [Table 1](#)) through SPI mapped registers, device EEPROM settings (see [Table 2](#)). The low-side switch deployment current limit is not programmable and is fixed to a level greater than the high-side driver current limit. The ON time duration for each individual squib driver can be programmed through SPI mapped registers.

The deployment sequence requires a specific set of software commands combined with external hardware enable logic lines (TZ0=H, IWD=L) to provide deployment capability. The turn-on sequence of the high-side driver and low-side drivers is software controlled via SPI commands, but the turn-off procedure is automatically provided by the deployment ASIC. After the programmed ON time duration has been achieved, the high-side switch is deactivated first then followed by the low-side driver deactivation by approximately 100µsec.

The RESET_N is an active low input reset signal. This input will be released high by the power supply unit and/or the µC once the external voltage supplies are within the specified limits. The external microcontroller is required to configure and control device through the serial communication interface. Reliable software is critical for the system operation.

Table 1. Potential Deployment Settings for Typical Firing Current

FIRING VOLTAGE	MAXIMUM AVERAGE FIRING VOLTAGE BETWEEN VZx AND Zx PINS TO ACHIEVE DEPLOYMENT	TYPICAL FIRING CURRENT	DWELL (FIRING) TIME ⁽¹⁾
35 V	32.56 V	1.2 A	2 ms
35 V	35.0 V	1.75 A	0.5 ms

(1) For programming desired dwell (firing) time.

Extended deployment duration activates the over temperature protection circuit and terminates deployment. If short-to-ground condition occurs during deployment, 35V firing voltage is completely dropped across the HS_FET: therefore, thermal shut down protection kicks in to protect the device.

Table 2. Potential Deployment Settings for Maximum Firing Current

FIRING VOLTAGE	MAXIMUM AVERAGE FIRING VOLTAGE BETWEEN VZx AND Zx PINS TO ACHIEVE DEPLOYMENT	MAX FIRING CURRENT ⁽¹⁾	DWELL (FIRING) TIME ⁽²⁾
35 V	30 V	2.6 A (for 1.75 A current setting)	0.7 ms
35 V	31 V	2.0 A (for 1.2 A current setting)	2.0 ms

(1) The max firing current levels are set through device EEPROM setting

(2) For programming desired dwell (firing) time

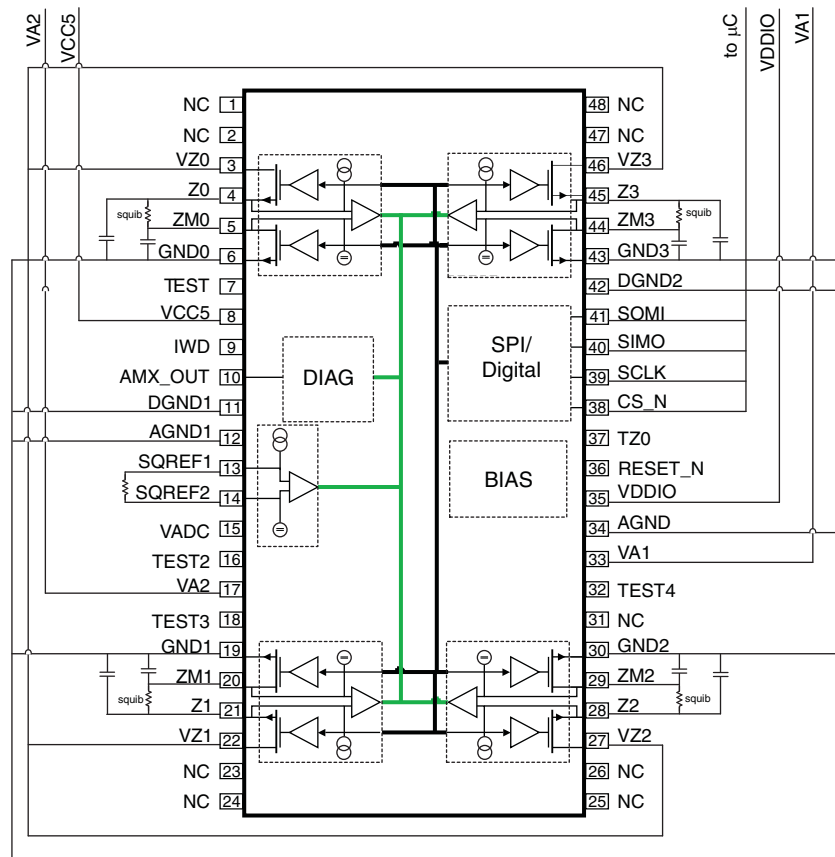
For the full version of this document, please contact msamktg@list.ti.com.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	HTSSOP – DCA	Tape and reel	TPIC71004TDCAQ1	TPIC71004
			TPIC71004TDCARQ1	

- (1) "Pb-Free" is defined to be compliant with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials unless exempt. Where designed to be soldered at high temperatures, TI "Pb-Free" and "RoHS Compliant" products are suitable for use in specified lead-free processes.

Functional Block Diagram



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPIC71004TDCARQ1	Active	Production	HTSSOP (DCA) 48	2000 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPIC71004T

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

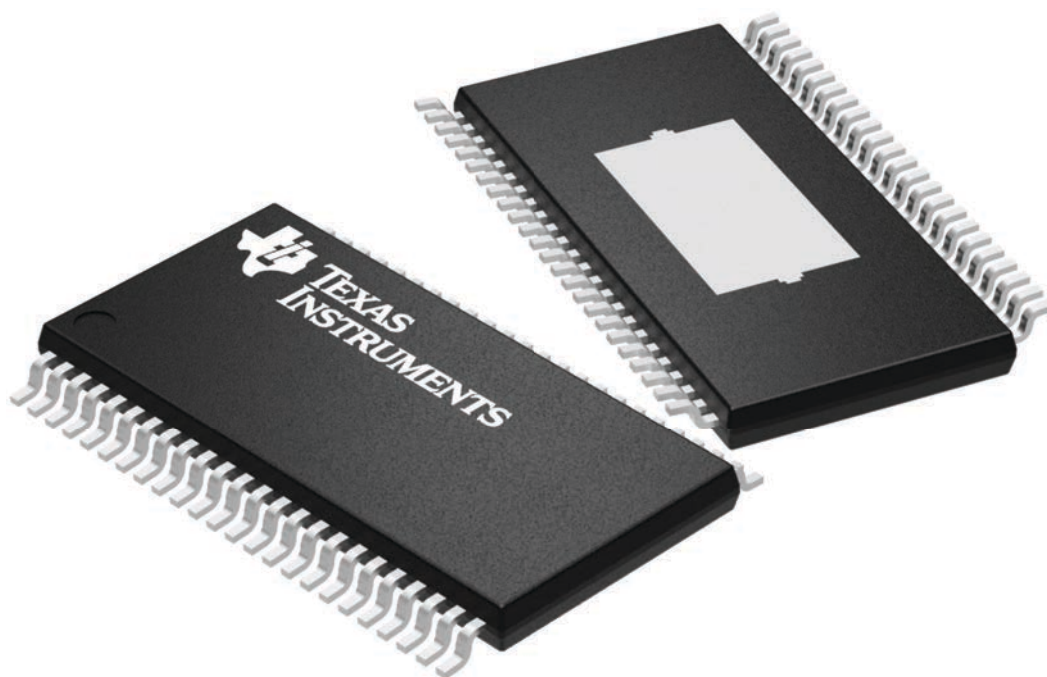
DCA 48

HTSSOP - 1.2 mm max height

12.5 x 6.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

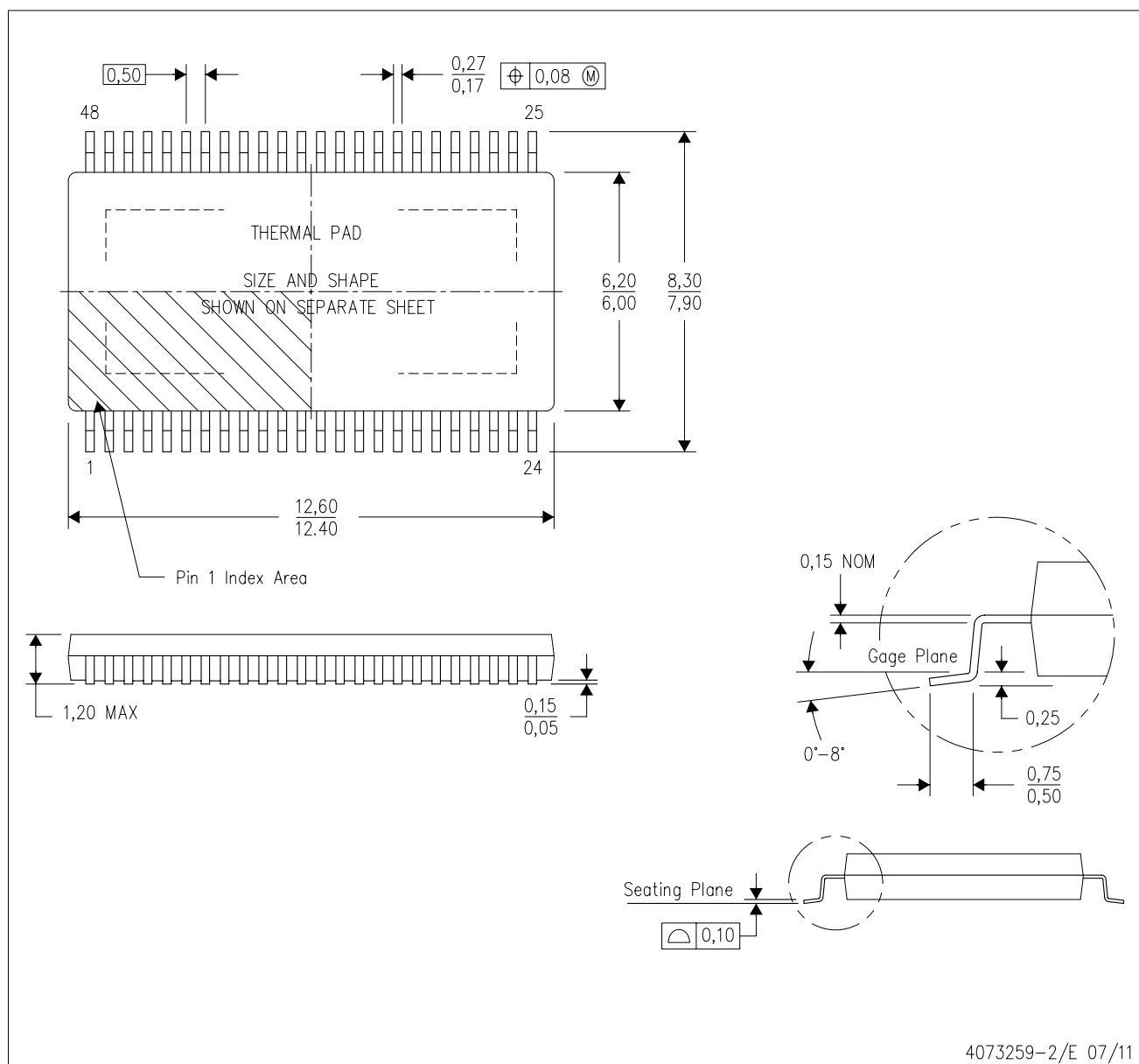
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224608/A

DCA (R-PDSO-G48)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

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DCA (R-PDSO-G48)

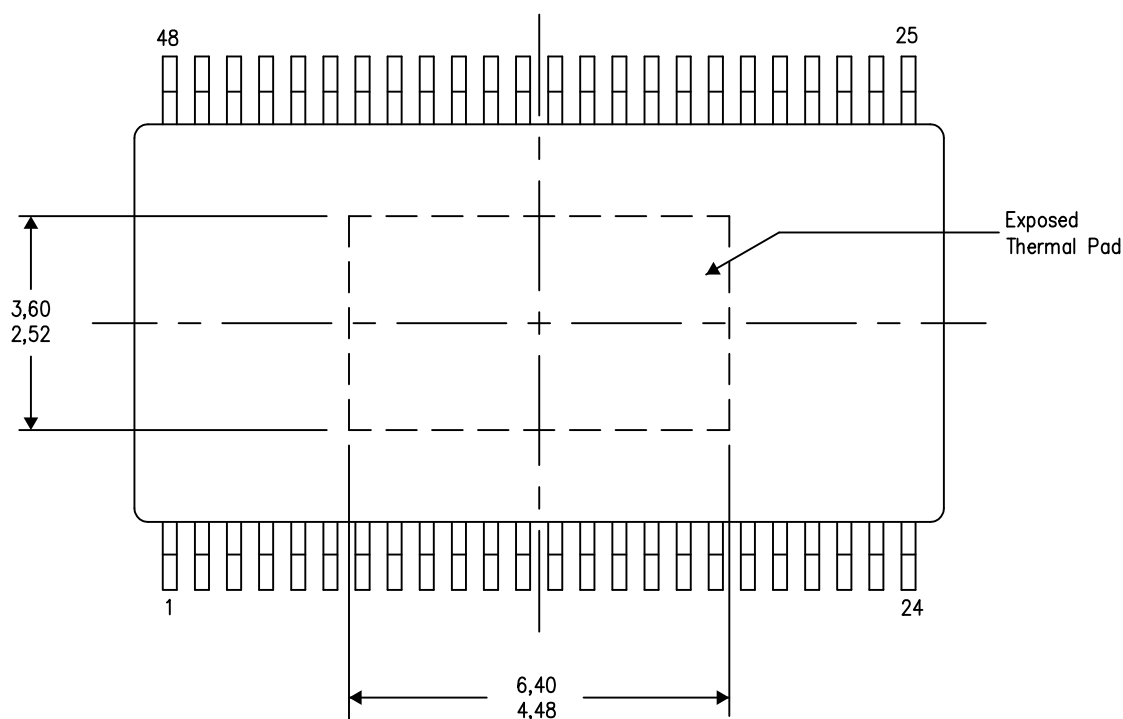
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



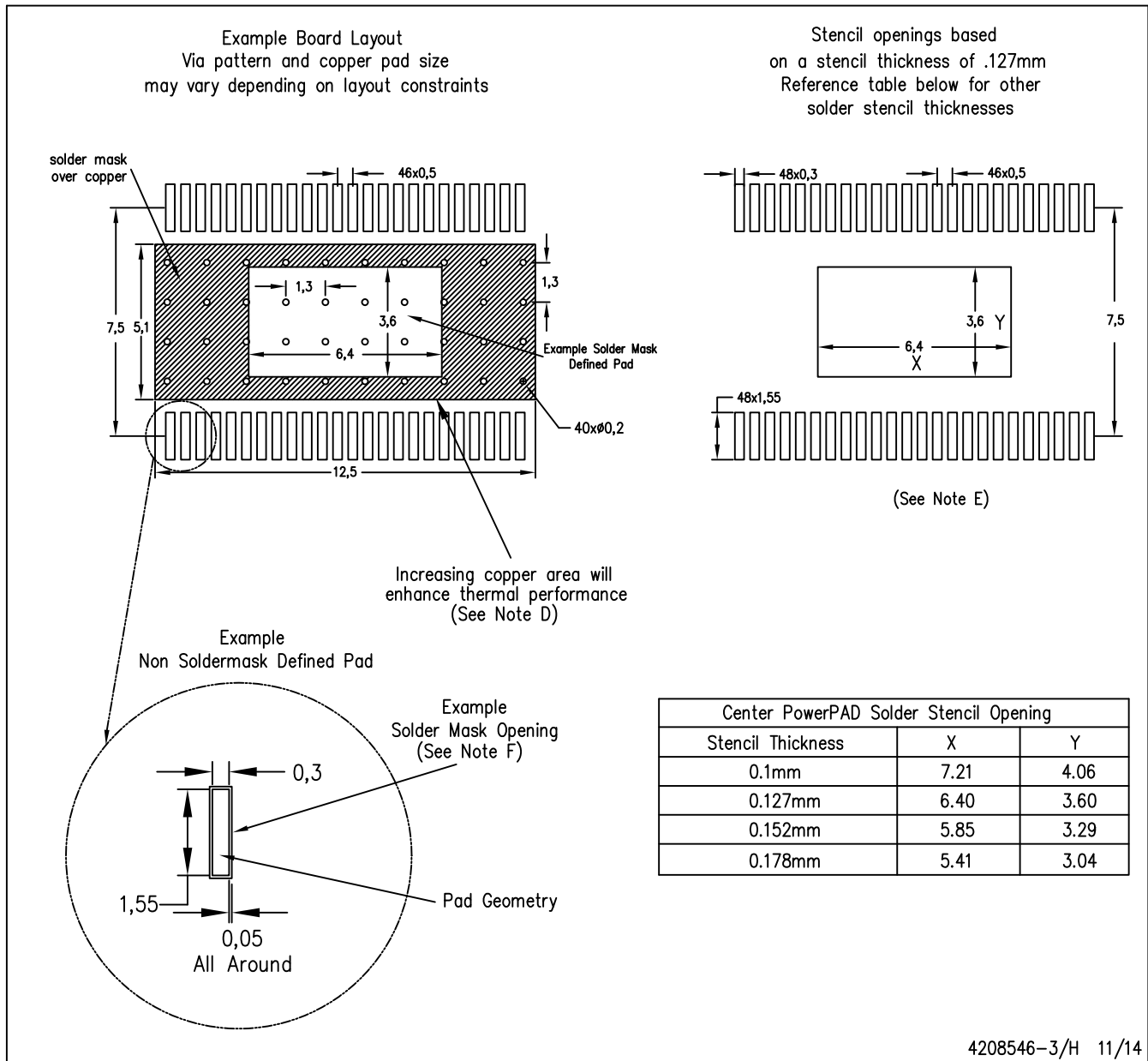
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NOTE: A. All linear dimensions are in millimeters

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DCA (R-PDSO-G48)

PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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