

## Wide Input Voltage, Adjustable Frequency, 3 A, 2 MHz Synchronous Buck Regulator

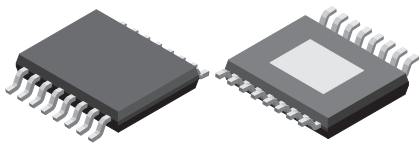
### FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Operating voltage range: 4 to 36 V
- UVLO STOP threshold:  $2.6 V_{TYP}$
- Maximized duty cycle for low-dropout operation
- Withstands surge voltages up to 40 V
- Capable of 3 A steady-state output current
- Integrated high-side and low-side switching MOSFETs
- Adjustable switching frequency ( $f_{SW}$ ): 100 kHz to 2.2 MHz
- Synchronization capability to external clock: 100 kHz to 2.2 MHz
- Frequency dithering for lower EMI signature
- External adjustable compensation network
- Soft-start time externally set via the SS pin
- Pre-bias startup compatible
- Active-low, power-on reset (NPOR) output

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### PACKAGES:

16-Pin eTSSOP (LP) with exposed thermal pad



Not to scale

### DESCRIPTION

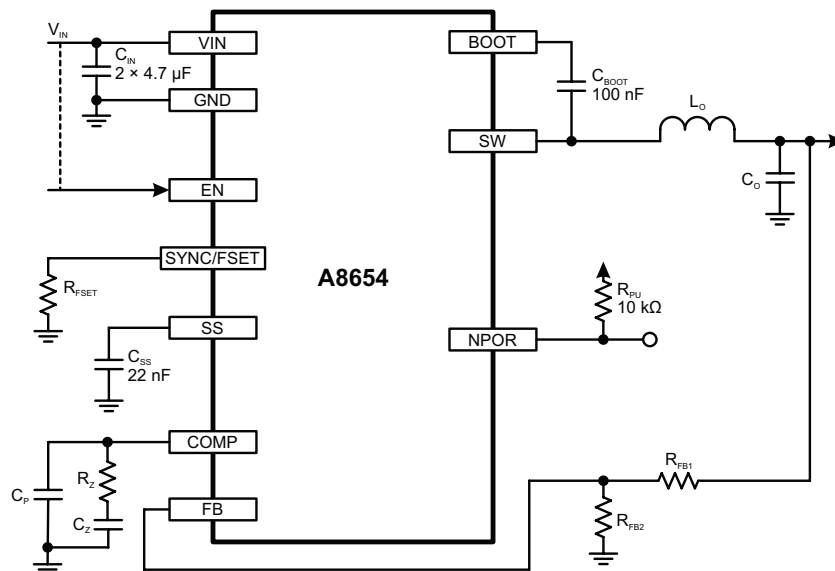
The A8654 is a high output current synchronous buck regulator that integrates low  $R_{DS(ON)}$  high-side and low-side N-channel MOSFETs. The A8654 incorporates PWM current-mode control to provide simple compensation, excellent loop stability and fast transient response. The A8654 uses external compensation to accommodate a wide range of power components to achieve both excellent loop stability and desirable transient response. The A8654 regulates nominal input voltages from 4 to 36 V and remains operational when  $V_{IN}$  drops as low as 2.6 V. When the input voltage approaches the output voltage, the duty cycle is maximized to maintain the output voltage. The A8654 is able to provide 3 A steady-state load current.

The A8654 features externally set soft-start time, external compensation network, an EN input to enable  $V_{OUT}$ , a SYNC/FSET input to synchronize or set the PWM switching frequency,

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### APPLICATIONS

- Automotive infotainment systems
  - Audio, video navigation systems
  - Rear seat media display
  - Instrument clusters
  - Telematics
- Advanced driver assistance systems
  - Radar, lidar, mmWave systems
  - Vision and detection system
- Industrial
  - General 24 V/36 V applications



Typical Application Diagram 1

### FEATURES AND BENEFITS (continued)

- Overvoltage protection, pulse-by-pulse current limit, hiccup mode short-circuit and thermal protections
- Open-circuit and adjacent pin short-circuit tolerant
- Short-to-ground tolerant at every pin
- Stable with ceramic output capacitors

### DESCRIPTION (continued)

and an NPOR output validated by the output voltage. Protection features include  $V_{IN}$  undervoltage lockout (UVLO), pulse-by-pulse overcurrent protection, hiccup mode short-circuit protection, overvoltage protection, and thermal shutdown. A8654 provides open-circuit, adjacent pin short-circuit and short-to-ground protection at every pin to satisfy the most demanding automotive and nonautomotive applications.

The maximum junction temperature is 150°C. The A8654 device is available in a 16-pin eTSSOP package with exposed pads for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte-tin leadframe plating.

### SELECTION GUIDE

Part Number	Packing	Package
A8654KLPTR-T	4000 pieces per 13-inch reel	4.4 mm × 5 mm, 1.2 mm nominal height 16-pin eTSSOP with exposed thermal pad



## SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN, SS			-0.3 to 40	V
SW to GND [2]	$V_{SW}$	Continuous	-0.3 to $V_{IN} + 0.3$	V
		$V_{IN} \leq 36$ V, $t < 50$ ns	-1.0 to $V_{IN} + 2.0$	V
BOOT Pin Above SW Pin	$V_{BOOT}$	Continuous	$V_{SW} - 0.3$ to $V_{SW} + 5.5$	V
		< 1 ms	$V_{SW} - 0.3$ to $V_{SW} + 7.0$	V
All other pins			-0.3 to 5.5	V
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature Range	$T_{stg}$		-55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

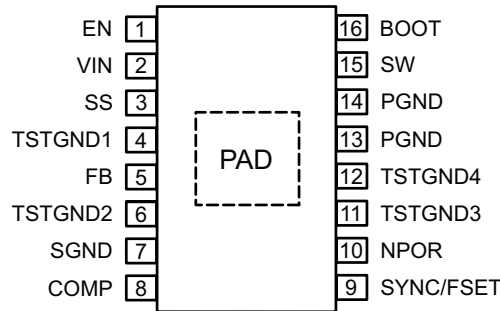
[2] SW has internal clamp diodes to GND and VIN. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limits.

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP Package, 4-layer PCB based on JEDEC standard	34	°C/W

[3] Additional thermal information available on the Allegro website.

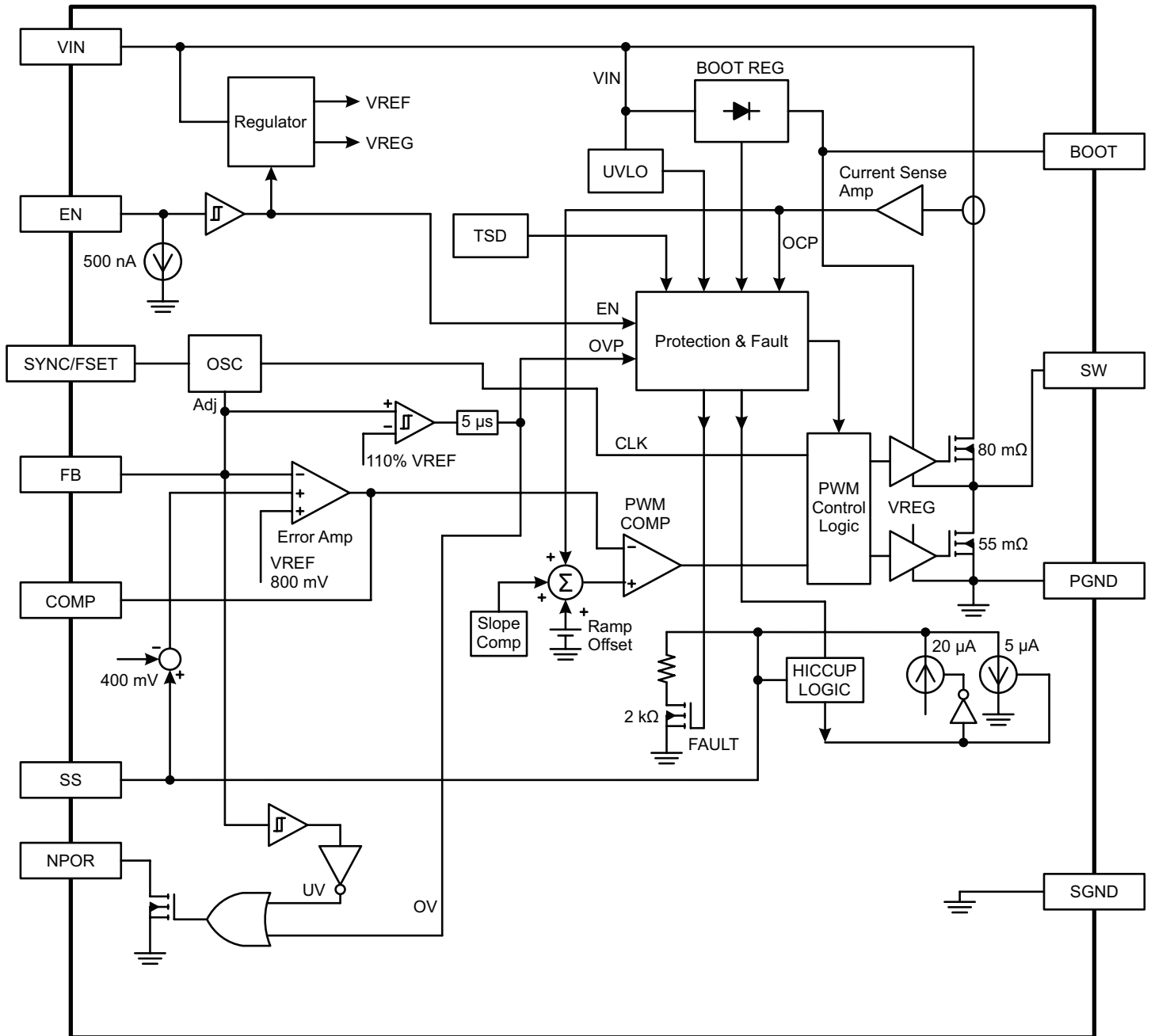
## PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 16-Pin eTSSOP Pinout Diagram

### Terminal List Table

Symbol	Number	Function
EN	1	Enable input. This pin is used to turn the converter on or off; set this pin high to turn the converter on or set this pin low to turn the converter off. May be connected to VIN.
VIN	2	Power input for the control circuits and the drain of the internal high-side N-channel MOSFET. A high-quality ceramic capacitor should be placed very close to this pin.
SS	3	Soft-Start pin. Connect a capacitor ( $C_{SS}$ ) from this pin to GND to set the soft-start time. This capacitor also determines the hiccup period during overcurrent.
FB	5	Feedback (negative) input to the error amplifier. Connect a resistor divider from the converter output node ( $V_{OUT}$ ) to this pin to program the output voltage.
SGND	7	Signal (quiet) ground.
COMP	8	Output of the error amplifier and compensation node for the control loop. Connect a series RC network from this pin to GND for loop compensation.
SYNC/FSET	9	Frequency setting and synchronization pin. A resistor, $R_{FSET}$ , from this pin to GND sets the PWM switching frequency.
NPOR	10	Active-low, power-on reset output signal. This pin is an open-drain output that transitions from low to high impedance after the output has maintained regulation for $t_{D,NPOR}$ .
TSTGND1-4	4, 6, 11, 12	Internal test pins, not for use. Should be connected to ground but do not use as main power ground.
PGND	13, 14	Power ground.
SW	15	The source of the high-side N-channel MOSFET. The output inductor ( $L_O$ ) should be connected to this pin. $L_O$ should be placed as close as possible to this pin and connected with relatively wide traces.
BOOT	16	High-side gate drive boost input. Connect a 100 nF ceramic capacitor from BOOT to SW
PAD	–	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad.



Functional Block Diagram

**ELECTRICAL CHARACTERISTICS:** Valid at  $4.0\text{ V} \leq V_{IN} \leq 36\text{ V}$ ;  $T_A = 25^\circ\text{C}$ ; • indicates specifications guaranteed  $-40^\circ\text{C} \leq T_A = T_J \leq 150^\circ\text{C}$ , unless noted otherwise.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>INPUT VOLTAGE SPECIFICATIONS</b>							
Operating Input Voltage Range [2]	$V_{IN}$		• 4.0	–	36.0	V	
UVLO Start Threshold	$V_{UVLO(START)}$	$V_{IN}$ rising	–	3.4	3.7	V	
UVLO Stop Threshold	$V_{UVLO(STOP)}$	$V_{IN}$ falling	–	2.6	2.9	V	
UVLO Hysteresis	$V_{UVLO(HYS)}$		–	800	–	mV	
<b>INPUT CURRENTS</b>							
Input Quiescent Current [1]	$I_Q$	$V_{EN} = 5\text{ V}$ , $V_{FB} = 1.0\text{ V}$ , no PWM switching	• –	3.0	6.5	mA	
Input Sleep Supply Current [1]	$I_{Q(SLEEP)}$	$V_{IN} = 12\text{ V}$ , $V_{EN} \leq 0.4\text{ V}$ , $-40^\circ\text{C} < T_A = T_J < 85^\circ\text{C}$	–	1	240	$\mu\text{A}$	
		$V_{IN} = 12\text{ V}$ , $V_{EN} \leq 0.4\text{ V}$ , $T_A = T_J = 125^\circ\text{C}$	–	40	900	$\mu\text{A}$	
<b>VOLTAGE REGULATION</b>							
Feedback Voltage Accuracy [3]	$V_{FB}$	$V_{FB} = V_{COMP}$ , $-40^\circ\text{C} < T_A = T_J < 125^\circ\text{C}$		792	800	808	mV
		$V_{FB} = V_{COMP}$	•	788	800	812	mV
Output Dropout Voltage [3]	$V_{O(PWM)}$	$V_{IN} = 5.9\text{ V}$ , $I_O = 3\text{ A}$ , $f_{SW} = 500\text{ kHz}$	•	4.9	–	–	V
		$V_{IN} = 7.5\text{ V}$ , $I_O = 3\text{ A}$ , $f_{SW} = 2\text{ MHz}$	•	4.9	–	–	V
<b>ERROR AMPLIFIER</b>							
Feedback Input Bias Current [1]	$I_{FB}$		–100	–	–8	nA	
Open Loop Voltage Gain	$A_{VOL}$	$V_{COMP} = 1.2\text{ V}$	–	65	–	dB	
Transconductance	gm	$400\text{ mV} < V_{FB}$		550	750	950	$\mu\text{A/V}$
		$0\text{ V} < V_{FB} < 400\text{ mV}$		275	375	475	
Output Current	$I_{EA}$	$V_{COMP} = 1.2\text{ V}$	–	$\pm 75$	–	$\mu\text{A}$	
<b>INTERNAL MOSFET PARAMETERS</b>							
High-Side MOSFET On Resistance [3]	$R_{DSON(HS)}$	$T_A = 25^\circ\text{C}$ , $I_{DS} = 100\text{ mA}$	–	80	–	$\text{m}\Omega$	
SW Node Rising Slew Rate	dV/dt	$12\text{ V} < V_{IN} < 16\text{ V}$	–	0.75	–	V/ns	
SW Leakage [1]	$I_{SW(LEAK)}$	$V_{EN} \leq 0.4\text{ V}$ , $V_{SW} = 5\text{ V}$ , $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$	–10	0	10	$\mu\text{A}$	
Low-Side MOSFET On Resistance [3]	$R_{DSON(LS)}$	$T_A = 25^\circ\text{C}$ , $I_{DS} = 100\text{ mA}$	–	55	–	$\text{m}\Omega$	
<b>OSCILLATOR</b>							
PWM Switching Frequency	$f_{SW}$	$R_{FSET} = 261\text{ k}\Omega$	–	100	–	kHz	
		$R_{FSET} = 61.9\text{ k}\Omega$		375	415	457	kHz
		$R_{FSET} = 10.5\text{ k}\Omega$		–	2.0	–	MHz
PWM Frequency Dithering	$f_{DITHER}$	No Dithering with FSET Synchronization	–	$\pm 13$	–	%	
Minimum Controllable On-Time	$t_{ON(MIN)}$	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$	–	95	135	ns	
Minimum Switch Off-Time	$t_{OFF(MIN)}$	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 1\text{ A}$	–	100	135	ns	

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**ELECTRICAL CHARACTERISTICS (continued):** Valid at  $4.0\text{ V} \leq V_{IN} \leq 36\text{ V}$ ;  $T_A = 25^\circ\text{C}$ ; • indicates specifications guaranteed  $-40^\circ\text{C} \leq T_A = T_J \leq 150^\circ\text{C}$ , unless noted otherwise.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>FSET SYNCHRONIZATION TIMING</b>						
Synchronization Frequency Range	$f_{SW\_MULT}$		100	–	2200	kHz
Synchronization Input Off-Time	$t_{SYNC\_OFF}$		0.2	–	1.3	$\mu\text{s}$
Synchronization Input Rise Time <sup>[3]</sup>	$t_{r(SYNC)}$		–	10	15	ns
Synchronization Input Fall Time <sup>[3]</sup>	$t_{f(SYNC)}$		–	10	15	ns
Synchronization Rising Threshold	$V_{SYNC(HI)}$	$V_{SYNC}$ rising	–	–	2.0	V
Synchronization Falling Threshold	$V_{SYNC(LO)}$	$V_{SYNC}$ falling	0.5	–	0.7	V
<b>CURRENT LOOP</b>						
Peak Inductor (Pulse-by-Pulse) Current Limit	$I_{PK\_LIM(MINON)}$	$t_{ON} = t_{ON(MIN)}$	4.1	4.7	5.3	A
	$I_{PK\_LIM(MINOFF)}$	$t_{ON} = 1/f_{SW} - t_{OFF(MIN)}$ , no sync	3.0	3.9	4.8	A
COMP to SW Current Gain	$g_{mPOWER}$		–	7.3	–	A/V
Slope Compensation	$S_E$	$R_{FSET} = 261\text{ k}\Omega$ , 100 kHz	–	0.056	–	A/ $\mu\text{s}$
		$R_{FSET} = 61.9\text{ k}\Omega$ , 415 kHz	0.09	0.24	0.43	A/ $\mu\text{s}$
		$R_{FSET} = 10.5\text{ k}\Omega$ , 2 MHz	–	1.3	–	A/ $\mu\text{s}$
<b>SOFT-START</b>						
SS FAULT/HICCUP Reset Voltage	$V_{SS(RST)}$	$V_{SS}$ falling due to $R_{SS(FLT)}$	–	200	275	mV
SS Maximum Charge Voltage	$V_{SS(MAX)}$		–	3.3	–	V
SS Startup (Source) Current <sup>[1]</sup>	$I_{SS(SU)}$	HICCUP = FAULT = 0	–30	–20	–10	$\mu\text{A}$
SS Hiccup (Sink) Current <sup>[1]</sup>	$I_{SS(HIC)}$	HICCUP = 1	1	2.2	5	$\mu\text{A}$
SS Pull-Down Resistance	$R_{SS(FLT)}$	FAULT = 1 or EN = 0	–	2	–	k $\Omega$
SS Switching Frequency	$f_{SS}$	$0\text{ V} < V_{FB} < 200\text{ mV}$	–	$f_{SW}/4$	–	–
		$200\text{ mV} < V_{FB} < 400\text{ mV}$	–	$f_{SW}/2$	–	–
		$400\text{ mV} < V_{FB}$	–	$f_{SW}$	–	–
<b>HICCUP MODE</b>						
Hiccup OCP Enable Threshold	$V_{HIC(EN)}$	$V_{SS}$ rising	–	2.3	–	V
Hiccup, OCP Count	$OCP_{LIM}$	$V_{SS} > 2.3\text{ V}$ , OCP pulses	–	240	–	counts
Hiccup, BOOT Shorted Count	$BOOT_{UV}$		–	64	–	counts
Hiccup, BOOT Open Count	$BOOT_{OPEN}$		–	7	–	counts
<b>NPOR OUTPUT</b>						
$V_{OUT}$ OV Threshold	$V_{OUT(OV)}$	$V_{FB}$ rising	840	880	920	mV
$V_{OUT}$ OV Hysteresis	$V_{OUT(OV,HYS)}$	$V_{FB}$ falling, relative to $V_{OUT(OV)}$	–	10	–	mV
$V_{OUT}$ UV Threshold	$V_{OUT(UV)}$	$V_{FB}$ falling	715	740	760	mV
$V_{OUT}$ UV Hysteresis	$V_{OUT(UV,HYS)}$	$V_{FB}$ rising, relative to $V_{OUT(UV)}$	–	10	–	mV
NPOR Rising Delay	$t_{d(NPOR)}$	$V_{FB}$ rising only	–	2500	–	PWM Cycles
NPOR Low Output Voltage	$V_{OL(NPOR)}$	$I_{POR} = 5\text{ mA}$	–	185	400	mV
NPOR Leakage <sup>[1]</sup>	$I_{NPOR(LEAK)}$	$V_{POR} = 5.5\text{ V}$	–	–	5	$\mu\text{A}$

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**ELECTRICAL CHARACTERISTICS (continued):** Valid at  $4.0\text{ V} \leq V_{\text{IN}} \leq 36\text{ V}$ ;  $T_{\text{A}} = 25^{\circ}\text{C}$ ; • indicates specifications guaranteed  $-40^{\circ}\text{C} \leq T_{\text{A}} = T_{\text{J}} \leq 150^{\circ}\text{C}$ , unless noted otherwise.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>THERMAL PROTECTION</b>						
TSD Rising Threshold	TSD	PWM stops immediately and COMP is pulled low and SS is reset	155	170	185	$^{\circ}\text{C}$
TSD Hysteresis [3]	TSD <sub>HYS</sub>		–	20	–	$^{\circ}\text{C}$
<b>EN INPUT THRESHOLDS</b>						
EN High Threshold	$V_{\text{EN(H)}}$	EN rising	–	1.41	2.0	V
EN Low Threshold	$V_{\text{EN(L)}}$	EN falling	0.7	1.36	–	V
EN Delay	$t_{\text{d(EN)}}$	EN transitioning low, $V_{\text{OUT}} < 25\%$	–	60	–	PWM cycles
EN Input Bias Current [1]	$I_{\text{EN BIAS}}$	EN = 5 V	–	500	–	nA

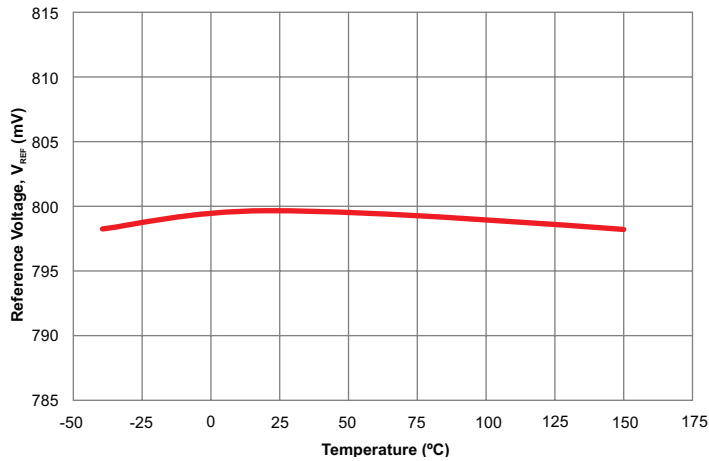
[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin or node.

[2] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.

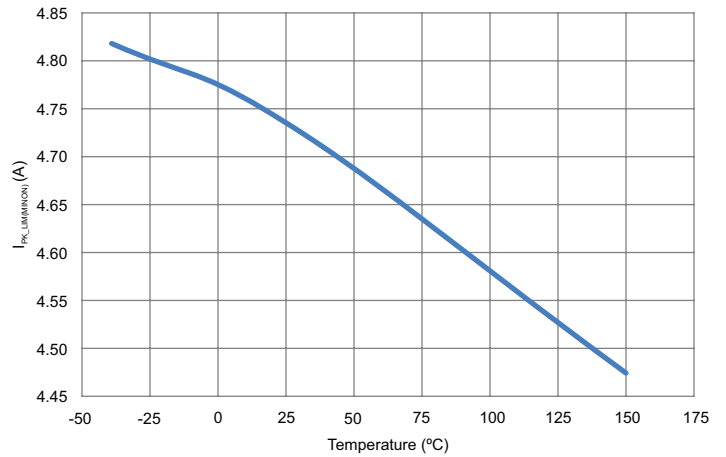
[3] Ensured by design and characterization, not production tested.



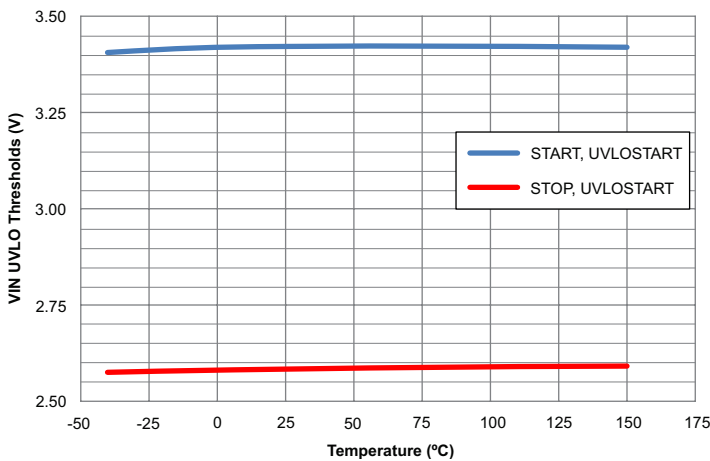
## TYPICAL PERFORMANCE CHARACTERISTICS



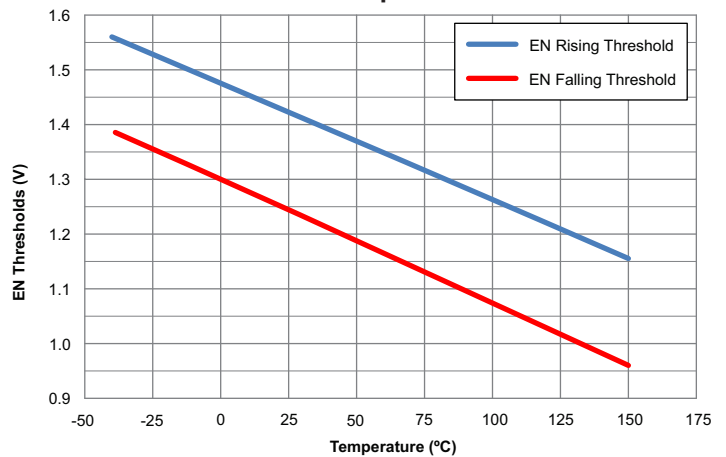
Reference Voltage versus Temperature



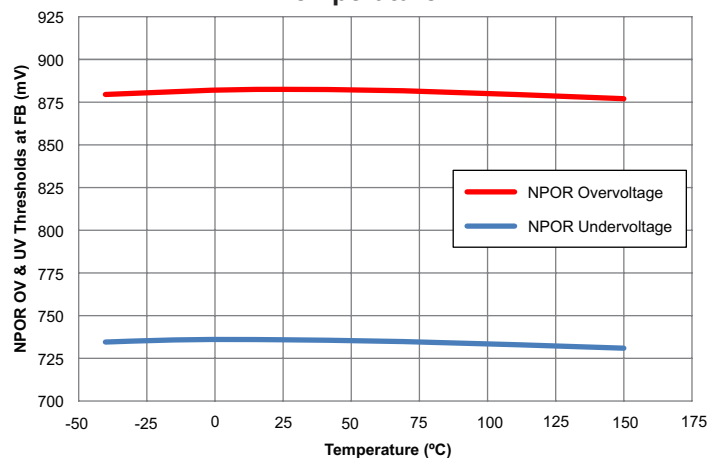
Pulse-by-pulse Current Limit at  $t_{ON(MIN)}$  ( $I_{PK\_LIM(MINON)}$ ) versus Temperature



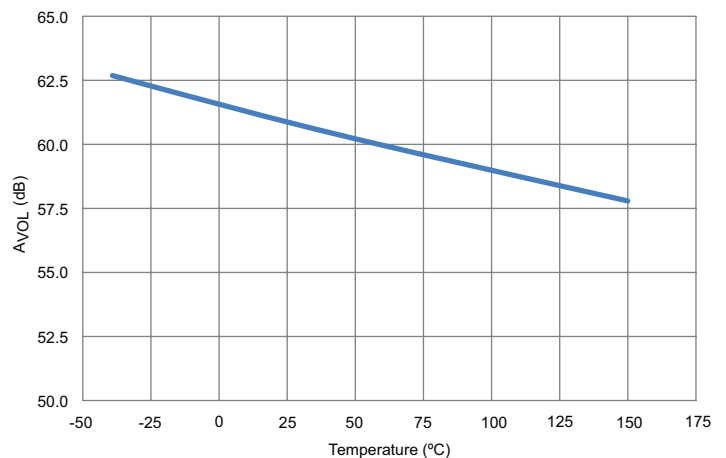
VIN UVLO START and STOP Thresholds versus Temperature



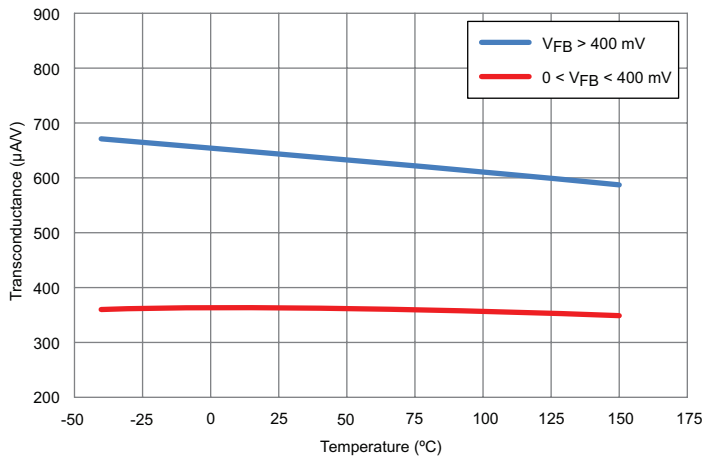
EN Rising and Falling Thresholds versus Temperature



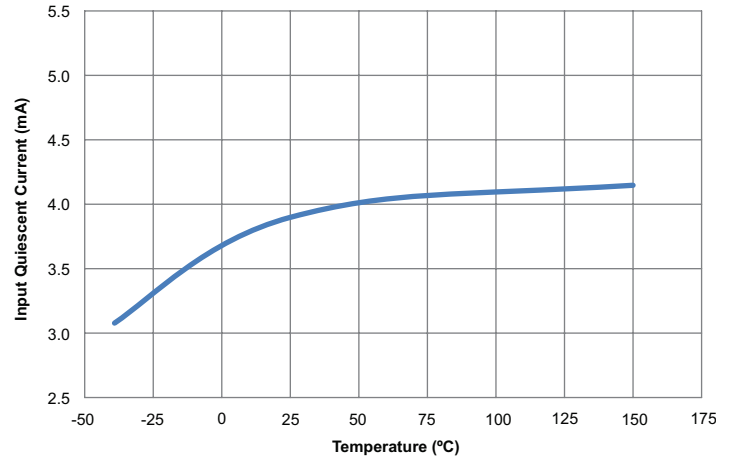
NPOR Overvoltage and Undervoltage Thresholds at FB versus Temperature



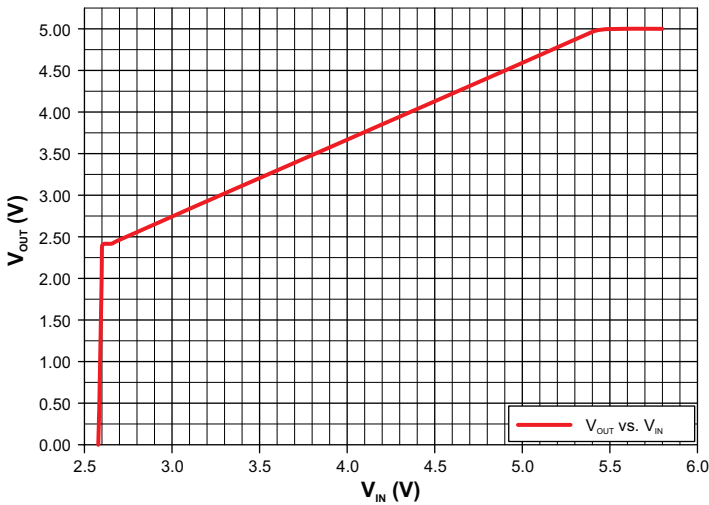
Open Loop Voltage Gain ( $A_{VOL}$ ) of Error Amplifier versus Temperature



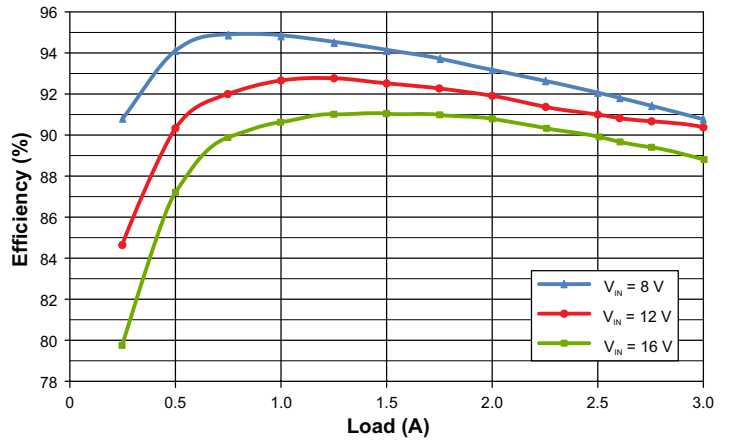
Error Amplifier Transconductance versus Temperature



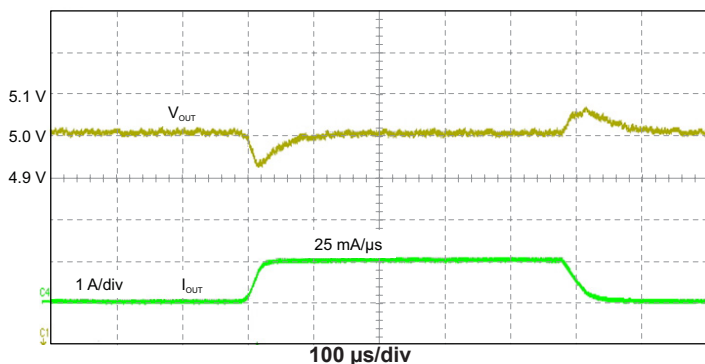
Quiescent Current  $I_{\text{Q}}$  versus Temperature



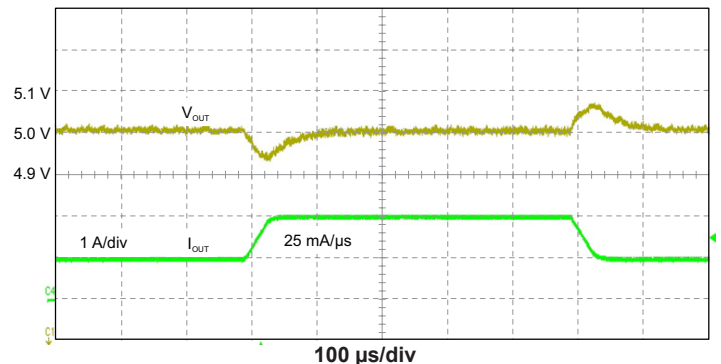
Low  $V_{\text{IN}}$  Dropout Operation at  $5 \Omega$  Load



Efficiency versus Output Current for Typical Designs  
(500 kHz in Table 3)



Transient Response 0 A to 1 A Load Step  
(Typical Design - 500 kHz in Table 3)



Transient Response 1 A to 2 A Load Step  
(Typical Design - 500 kHz in Table 3)

## FUNCTIONAL DESCRIPTION

### Overview

The A8654 is a synchronous PWM buck regulator that integrates low  $R_{DS(on)}$  high-side and low-side N-channel MOSFETs. It is designed to remain operational when input voltage falls as low as 2.6 V. The A8654 employs peak current-mode control to provide superior line and load regulation, pulse-by-pulse current limit, fast transient response, and simple compensation.

The features of the A8654 include an internal precision reference, an adjustable switching frequency, a transconductance error amplifier, an enable input, integrated top and bottom switching MOSFETs, adjustable soft-start time, pre-bias startup, and an NPOR output. Protection features of A8654 include  $V_{IN}$  undervoltage lockout, pulse-by-pulse overcurrent protection, BOOT overvoltage and undervoltage protection, hiccup mode short-circuit protection, overvoltage protection, and thermal shutdown. In addition, the A8654 provides open-circuit, adjacent pin short-circuit, and pin-to-ground short-circuit protection.

### Reference Voltage

The A8654 incorporates an internal precision reference that allows output voltages as low as 0.8 V. The accuracy of the internal reference is  $\pm 1\%$  from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $\pm 1.5\%$  across from  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ . The output voltage of the regulator is programmed with a resistor divider between  $V_{OUT}$  and the FB pin of the A8654.

### Oscillator/Switching Frequency and Synchronization

The PWM switching frequency of the A8654 is adjustable from 100 kHz to 2.2 MHz and has an accuracy of about  $\pm 10\%$  over the operating temperature range. Connecting a resistor from the FSET/SYNC pin to GND, as shown in the Applications Schematic, sets the switching frequency. An FSET resistor with  $\pm 1\%$  tolerance is recommended. A graph of switching frequency versus FSET resistor value is shown in the Component Selection section of this datasheet. The A8654 will suspend operation if the FSET pin is shorted to GND or left open.

The FSET/SYNC pin also can be used as a synchronization input that accepts an external clock to switch the A8654 from 100 kHz to 2.2 MHz and scales the slope compensation according to the synchronization frequency. When being used as a synchronization input, the applied clock pulses must satisfy the pulse width,

duty-cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet.

### Transconductance Error Amplifier

The transconductance error amplifier's primary function is to control the regulator's output voltage. The error amplifier is a three-terminal input device with two positive inputs and one negative input, as shown in Figure 1. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The error amplifier performs an "analog OR" selection between its positive inputs, operating according to the positive input with the lowest potential. The two positive inputs are used for soft-start and steady-state regulation. The error amplifier regulates to the soft-start pin voltage minus 400 mV during startup or the A8654's internal reference ( $V_{REF}$ ) during normal operation.

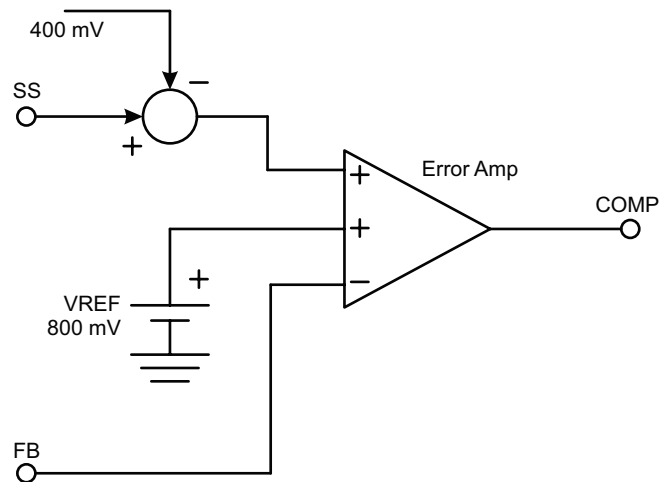


Figure 1: A8654 Error Amplifier

### Compensation Components

To stabilize the regulator, a series RC compensation network ( $R_Z$  and  $C_Z$ ) must be connected from the error amplifier's output (COMP pin) to GND as shown in the applications schematic. In most instances, an additional low value capacitor ( $C_P$ ) should be connected in parallel with the  $R_Z$ - $C_Z$  compensation network to reduce the loop gain at very high frequencies. However, if the  $C_P$  capacitor is too large, the phase margin of the converter may be reduced. Calculating  $R_Z$ ,  $C_Z$ , and  $C_P$  is covered in the Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled, the COMP pin is pulled to GND via the approximately 1 k $\Omega$  internal resistor and PWM switching is inhibited.

### Slope Compensation

The A8654 incorporates internal slope compensation to allow PWM duty cycles above 50% for a wide range of input/output voltages, switching frequencies, and inductor values. As shown in the functional block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset. The amount of slope compensation is scaled with the switching frequency when programming the frequency with a resistor or with an external clock.

The value of the output inductor should be chosen such that slope compensation rate  $S_E$  is between  $0.5\times$  and  $1\times$  the falling slope of the inductor current ( $S_F$ ).

### Current Sense Amplifier

The A8654 incorporates a high-bandwidth current sense amplifier to monitor the current through the top MOSFET. This current signal is used to regulate the peak current when the top MOSFET is turned on. The current signal is also used by the protection circuitry for the pulse-by-pulse current limit and hiccup mode short-circuit protection.

### Low-Dropout Operation and Undervoltage Lockout

The Undervoltage Lockout behavior is described in the following Protection Features section.

The A8654 is designed to allow operation when input voltage drops as low as 2.6 V which is the UVLO STOP threshold. When the input voltage falls towards the nominal output voltage, the high-side switch can remain on for maximum on-time to keep regulating the output. This is accomplished by decreasing the  $f_{SW}$  switching frequency. In this way, the dropout from the input to output voltage is minimized.

### Sleep Mode with Enable input

The A8654 provides a shutdown function via the EN pin. When this pin is low, the A8654 is shut down and the A8654 will enter a “sleep mode” where the internal control circuits will be shut off and draw less current from  $V_{IN}$ . If EN goes high, the A8654 will turn on and provided there are no fault conditions, soft-start

will be initiated and  $V_{OUT}$  will ramp to its final voltage in a time set by the soft-start capacitor ( $C_{SS}$ ). To automatically enable the A8654, the EN pin may be connected directly to  $V_{IN}$ .

### Power MOSFETs

The A8654 includes an 80 m $\Omega$ , high-side N-channel MOSFET. The A8654 also includes a 55 m $\Omega$ , low-side N-channel MOSFET to provide synchronous rectification.

When the A8654 is disabled via the EN input being low or a fault condition, the A8654’s output stage is tri-stated by turning off both the upper and lower MOSFETs.

### Pulse-Width Modulation (PWM) Mode

The A8654 employs fixed-frequency, peak current-mode control to provide excellent load and line regulation, fast transient response, and simple compensation.

A high-speed comparator and control logic is included in the A8654. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation signal, and a DC PWM ramp offset voltage ( $V_{PWM(OFFSET)}$ ).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop, the bottom MOSFET is turned off, the top MOSFET is turned on, and the inductor current increases. When the voltage at the non-inverting of PWM comparator rises above the error amplifier’s output COMP, the PWM flip flop is reset and the top MOSFET is turned off, the bottom MOSFET is turned on and the inductor current decreases.

The PWM flip-flop is reset dominant, so the error amplifier may override the CLK signal in certain situations.

### BOOT Regulator

The A8654 includes a regulator to charge its boot capacitor. The voltage across the BOOT capacitor is typically 5.0 V. If the boot capacitor is missing the A8654 will detect a boot overvoltage. Similarly, if the boot capacitor is shorted the A8654 will detect a boot undervoltage. Also, the boot regulator has a current limit to protect itself during a short-circuit condition.

### Soft-Start (Startup) and Inrush Current Control

The soft-start function controls the inrush current at startup. The soft-start pin (SS) is connected to GND via a capacitor. When the A8654 is enabled and all faults are cleared, the soft-start pin will source the charging current  $I_{SS(SU)}$  and the voltage on the soft-start capacitor  $C_{SS}$  will ramp upward from 0 V. When the voltage at the soft-start pin exceeds the Soft-Start COMP Release Threshold ( $V_{SS(RELEASE)}$ , typically 400 mV), the error amplifier will ramp up its output voltage above the PWM Ramp Offset. At that instant, the top and bottom MOSFETs will begin switching. There is a small delay ( $t_{SS(DELAY)}$ ) between the moments of EN pin transitioning high and the soft-start voltage reaching 400 mV to initiate PWM switching.

Once the A8654 begins PWM switching, the error amplifier will regulate the voltage at the FB pin to the soft-start pin voltage minus approximately 400 mV. During the active portion of soft-start, the voltage at the SS pin will rise from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin will rise from 0 V to 800 mV, and the regulator's output voltage will rise from 0 V to the setpoint determined by the feedback resistor divider.

During startup, the PWM switching frequency is reduced to 25% of  $f_{SW}$  while FB is below 200 mV. If FB is above 200 mV but below 400 mV, the switching frequency is 50% of  $f_{SW}$ . At the same time, the transconductance of the error amplifier,  $g_m$ , is reduced to 1/2 of nominal value when FB is below 400 mV. When FB is above 400 mV the switching frequency will be  $f_{SW}$  and the error amplifier's gain will be the nominal value. The reduced switching frequencies and error amplifier's gain are necessary to help improve output regulation and stability when  $V_{OUT}$  is at very low voltage. When  $V_{OUT}$  is very low, the PWM control loop requires on-time near the minimum controllable on-time and extra low duty cycles that are not possible at the nominal switching frequency.

When the voltage at the soft-start pin reaches approximately 1.2 V the error amplifier will "switch over" and begin regulating the voltage at the FB to A8654's adjusted reference voltage. The voltage at the soft-start pin will continue to rise to the internal LDO regulator's output voltage.

If the A8654 is disabled or a fault occurs, the internal fault latch is set and the capacitor at the SS pin is discharged to ground very

quickly through a 2 k $\Omega$  pull-down resistor. The A8654 will clear the internal fault latch when the voltage at the SS pin decays to approximately 200 mV. However, if the A8654 enters hiccup mode, the capacitor at the SS pin is slowly discharged through a current sink,  $I_{SS(HIC)}$ . Therefore, the soft-start capacitor  $C_{SS}$  not only controls the startup time but also the time between soft-start attempts in hiccup mode.

### Pre-Biased Startup

If the output of the buck regulator is pre-biased at a certain output voltage level, the A8654 will modify the normal startup routine to prevent discharging the output capacitors. As described in the Soft-Start (Startup) and Inrush Current Control section, the error amplifier usually becomes active when the voltage at the soft-start pin exceeds 400 mV. If the output is pre-biased, the voltage at the FB pin will be non-zero. The A8654 will not start switching until the voltage at SS pin rises to approximately  $V_{FB} + 400$  mV. From then on, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and  $V_{OUT}$  will ramp upward from the pre-bias level.

### Not Power-On Reset (NPOR) Output

The A8654 has an inverted Power-On Reset output (NPOR) with a fixed delay of its rising edge ( $t_{d(NPOR)}$ ). The NPOR output is an open-drain output so an external pull-up resistor must be used, as shown in the applications schematic. NPOR transitions high when the output voltage, sensed at the FB pin, is within regulation. The NPOR over- and undervoltage comparators incorporate a small amount of hysteresis (see EC table) and filtering (5  $\mu$ s, typical) to help reduce chattering due to the voltage ripple at the FB pin.

The NPOR output is immediately pulled low if either an under- or overvoltage condition occurs or the A8654's junction temperature exceeds the thermal shutdown threshold (TSD). For other faults, NPOR depends on the output voltage. Table 2 summarizes all the A8654 fault modes and their effects on NPOR.

At power-up, NPOR must be initialized (set to a logic low) when  $V_{IN}$  is relatively low. At power-down, NPOR must be held in the logic-low state as long as possible.



## PROTECTION FEATURES

The A8654 was designed to satisfy the most demanding automotive and nonautomotive applications. In this section, a description of each protection feature is described, and Table 2 summarizes the protections and their operation.

### Undervoltage Lockout Protection (UVLO)

An Undervoltage Lockout (UVLO) comparator in the A8654 monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the START threshold ( $V_{UVLO(START)}$ ,  $V_{IN}$  rising) or the STOP threshold ( $V_{UVLO(STOP)}$ ,  $V_{IN}$  falling). The UVLO comparator incorporates some hysteresis  $V_{UVLO(HYS)}$  to help reduce on/off cycling of the regulator due to the resistive or inductive drops in the VIN path during heavy loading or during startup.

### Pulse-by-Pulse Overcurrent Protection (OCP)

The A8654 monitors the current in the upper MOSFET, and if this current exceeds the pulse-by-pulse overcurrent threshold, then the upper MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The A8654 includes leading-edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the upper MOSFET is turned on.

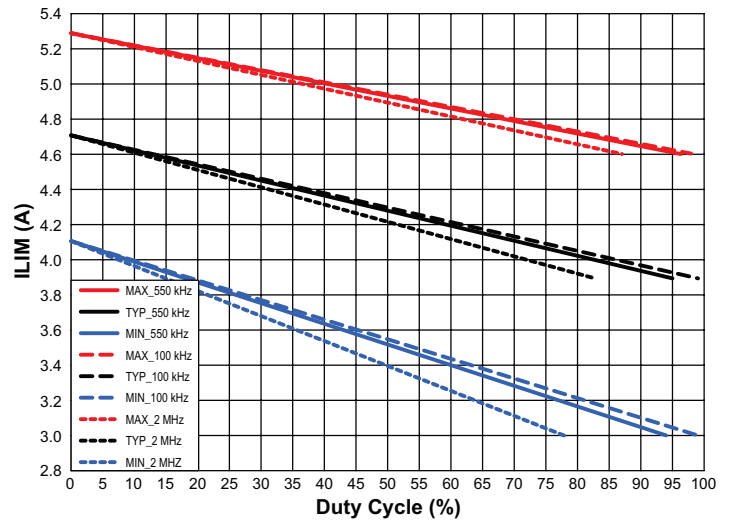
Because of the addition of the slope compensation ramp to the inductor current, the A8654 can deliver more current at lower duty cycles than at higher duty cycles to activate pulse-by-pulse overcurrent protection. Also, the slope compensation is not a perfectly linear function of switching frequency, so the current limit at lower switching frequency is larger compared with the limit at higher switching frequency for a given duty cycle.

Figure 2 shows the typical and worst-case pulse-by-pulse current limits versus duty cycles at 2 MHz, 550 kHz, and 100 kHz.

The exact current the buck regulators can support is heavily dependent on duty cycle ( $V_{IN}$ ,  $V_{OUT}$ ), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

### Overcurrent Protection (OCP) and Hiccup Mode

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load current is too high.



**Figure 2: Pulse-by-Pulse Current Limit vs. Duty Cycle at 100 kHz (long dashed lines), 550 kHz (solid lines) and 2 MHz (short dashed lines)**

When the voltage at the SS pin is below the Hiccup OCP Threshold, the hiccup mode counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

1.  $V_{SS} > V_{HIC(EN)}$  (2.3 V) and
2.  $V_{COMP}$  clamped at its maximum voltage ( $OCL = 1$ )

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP voltage decreases ( $OCL = 0$ ), the OCP counter is cleared. If the OCP counter reaches  $OCP_{LIM}$  counts (240), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 k $\Omega$ ).

The hiccup latch also enables a small current sink connected to the SS pin ( $I_{SS(HIC)}$ ). This causes the voltage at the soft-start pin to slowly ramp downward. When the voltage at the soft-start pin decays to a low-enough level ( $V_{SS(RST)}$ , 200 mV<sub>TYP</sub>) the hiccup latch is cleared, and the small current sink turned off. At that instant, the SS pin will begin to source current ( $I_{SS(SU)}$ ) and the voltage at the SS pin will ramp upward. This marks the beginning of a new, normal soft-start cycle as described earlier. When the voltage at the soft-start pin exceeds the error amp voltage by approximately 400 mV, the error amp will force the voltage at the COMP pin to quickly slew upward and PWM switching will resume. If the short circuit at the regulator's output remains,

another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the converter is disabled. If the short circuit is removed, the A8654 will soft-start normally and the output voltage will automatically recover to the desired level.

Thus, hiccup mode is a very effective protection for the overload condition. It can avoid false trigger for a short-term overload. On the other hand, for the extended overload, the average power dissipation during hiccup operation is very low to keep the controller cool and enhance the reliability.

Note that OCP is the only fault that results in hiccup mode being ignored while  $V_{SS} < 2.3$  V.

### BOOT Capacitor Protection

The A8654 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator will enter hiccup mode after 7 PWM cycles. If the BOOT capacitor is short-circuited, the regulator will enter hiccup mode after 64 PWM cycles.

For a BOOT fault, hiccup mode will operate virtually the same as described previously for an output short-circuit fault (OCP), with SS ramping up and down as a timer to initiate repeated soft-start attempts. BOOT faults are nonlatched conditions, so the A8654 will automatically recover when the fault is corrected.

### Overvoltage Protection (OVP)

The A8654 also includes an overvoltage comparator that monitors the FB pin exceeding 110%. When the voltage at the FB pin exceeds the overvoltage threshold ( $V_{OUT(OV)}$ ), A8654 will stop PWM switching, i.e., both high- and low-side switches will be turned off, and NPOR will be pulled low.

In most cases, the error amplifier will be able to maintain regulation since the synchronous output stage has excellent sink and source capability. However, the error amplifier and its regulation

voltage clamp are not effective when the FB pin is disconnected or when the output is shorted to the input supply. When the FB pin is disconnected from the feedback resistor divider, a tiny internal current source will force the voltage at the FB pin to rise above  $V_{OUT(OV)}$  and disable the regulator, preventing the load from being significantly overvoltage. If a higher external voltage is accidentally shorted to the A8654's output,  $V_{FB}$  will rise above the overvoltage threshold, triggering an OVP event and thus protecting the low-side switch. In either case, if the conditions causing the overvoltage are corrected, the regulator will automatically recover.

### Thermal Shutdown (TSD)

The A8654 monitors its junction temperature and will stop PWM switching and pull NPOR low if it becomes too hot. Also, to prepare for a restart, the SS and COMP pins will be pulled low until  $V_{SS} < V_{SS(RST)}$ . TSD is a nonlatched fault, so the A8654 will automatically recover if the junction temperature decreases by approximately 20°C.

### Pin-to-Ground and Pin-to-Pin Short Protections

The A8654 was designed to satisfy the most demanding automotive and nonautomotive applications. For example, the A8654 was carefully designed "up front" to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the A8654's pinout to optimize protection against pin-to-pin adjacent short circuits. For example, logic pins and high voltage pins were separated as much as possible. Inevitably, some low-voltage pins were located adjacent to high-voltage pins. In these instances, the low-voltage pins were designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the A8654.

**Table 1: Summary of A8654 Fault Modes and Operation**

Fault Mode	Fault Cases	V <sub>SS</sub>	During Fault Count, before Hiccup			Dropout Foldback	NPOR	BOOT Charging	LATCH	RESET
			V <sub>COMP</sub>	High-Side Switch	Low-Side Switch					
Positive Overcurrent Protection	1. Excessive I <sub>OUT</sub> 2. V <sub>OUT</sub> Shorted to GND 3. SW Soft Short To GND	Hiccup, after 240 faults of OCL	Clamped to achieve I <sub>LIM</sub> , and pulled low only by hiccup	CCM according to COMP	CCM according to COMP	f <sub>SW</sub> /4 or f <sub>SW</sub> /2 based on V <sub>FB</sub>	Depends on V <sub>OUT</sub>	Not affected	No	Auto, remove short
Negative Overcurrent Protection	1. Excessive Negative I <sub>OUT</sub> 2. Inductor Short	Hiccup, after 1 fault of LSOC	Pulled low only by hiccup	Forced Off Immediately	Forced off Immediately	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Not affected	No	Auto, remove short
SW Hard Short to GND	SW to GND hard Short	Hiccup at the end of blankOn	Pulled low only by hiccup	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Not affected	No (option available)	Auto, remove short
Thermal Shutdown	Die is too hot	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Forced Off Immediately	Forced off Immediately	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto, Cool Down
Boot Capacitor Greater than 7.0 V	BOOT capacitor Open	Hiccup, after 7 latched faults	Pulled low by hiccup	CCM according to COMP	CCM according to COMP	Dropout Foldback Disabled by Hiccup	Depends on V <sub>OUT</sub>	Off for rest of period	-	-
Boot Capacitor On Fault	BOOT Capacitor Open	Hiccup, after 7 latched faults	Pulled low by hiccup	CCM according to COMP	CCM according to COMP	Dropout Foldback Disabled by Hiccup	Depends on V <sub>OUT</sub>	Off only during hiccup	No	Auto, replace capacitor
Boot Capacitor Overcurrent	BOOT to GND Short	Not affected	Not affected	Not affected	Pulsed at minOff	Not affected	Depends on V <sub>OUT</sub>	Off until fault clears	-	-
Boot Capacitor Low Voltage	Normal Low V <sub>IN</sub> Operation	Not affected	Not affected	Not affected	Active during minOff period	Not affected	Depends on V <sub>OUT</sub>	On	-	-
Boot Capacitor Undervoltage	BOOT Capacitor Short	Not affected	Not affected	Forced Off Immediately	Active during minOff period	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	On	-	-
Low Side Switch Undervoltage	Low V <sub>IN</sub>	Not affected	Not affected	Forced Off Immediately	Forced Off Immediately	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Not affected	-	-
V <sub>REG</sub> Undervoltage	Low V <sub>IN</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Forced Off Immediately	Forced Off Immediately	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto
V <sub>IN</sub> Undervoltage	Low V <sub>IN</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Off	No	Auto

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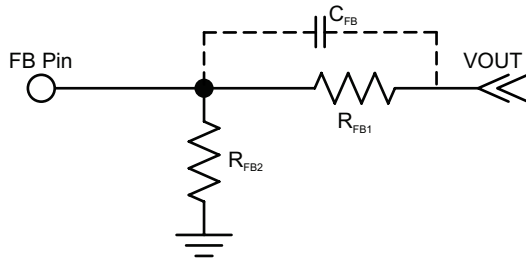
**Table 1: Summary of A8654 Fault Modes and Operation (continued)**

Fault Mode	Fault Cases	V <sub>SS</sub>	During Fault Count, before Hiccup			Dropout Foldback	NPOR	BOOT Charging	LATCH	RESET
			V <sub>COMP</sub>	High-Side Switch	Low-Side Switch					
Hiccup Delay (after fault count is reached)	Hiccup	Discharged with I <sub>SS(HIC)</sub> until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Pulled Low until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Forced Off at Start of Period	One Shot Diode Emulation	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Not affected, (off only for boot capacitor faults) (sleep option available)	-	-
Hiccup Restart or Startup (after V <sub>SS</sub> returns to V <sub>SS(RST)</sub> )	StartupHiccup	Charged with I <sub>SS(SU)</sub>	Released from 0 V, then responds to V <sub>SS</sub> ↑	CCM after V <sub>COMP</sub> > 400 mV	CCM after V <sub>COMP</sub> > 400 mV (pulsed at minOff)	Dropout Foldback Reset	Depends on V <sub>OUT</sub>	Not affected	-	-
FB Overvoltage	1. V <sub>OUT</sub> to VIN Short 2. FB Pin Open	Not affected	Not affected	Forced Off Immediately	One Shot Diode Emulation	Dropout Foldback Reset	Pulled Low Immediately	Off	No	Auto, V <sub>FB</sub> to normal range
FB Undervoltage	Startup	Not affected	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Pulled Low Immediately	Not affected	No	Auto, V <sub>FB</sub> to normal range
Feedback Less Than 400 mV	Startup	Not affected	Not affected	f <sub>SW</sub> /2	CCM according to COMP	Not affected	Pulled Low	Not affected	-	-
Feedback Less Than 200 mV	StartupV <sub>OUT</sub> to GND Short	Not affected	Not affected	f <sub>SW</sub> /4	CCM according to COMP	f <sub>SW</sub> already at 1/4	Pulled Low	Not affected	-	-
FSET Resistor Fault	1.FSET to GND short 2.FSET pulled high 3.Low R 4.High R	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Pulled Low Immediately & latched until V <sub>SS</sub> < V <sub>SS(RST)</sub>	Forced Off Immediately	One Shot Diode Emulation	Not affected	Depends on V <sub>OUT</sub>	Off	-	-
SS shorted to VIN	SS to VIN short	Clamped to Zener voltage internally	Not affected	CCM according to COMP	CCM according to COMP	Not affected	Depends on V <sub>OUT</sub>	Not affected	-	-
SS shorted to GND	SS to GND short	At GND	Loop response only	CCM according to COMP	CCM according to COMP	Not affected	Depends on V <sub>OUT</sub>	Not affected	-	-
COMP shorted to GND	COMP to GND short	Not affected	At GND	CCM according to COMP	CCM according to COMP	Not affected	Depends on V <sub>OUT</sub>	Not affected	-	-

## DESIGN AND COMPONENT SELECTION

### Setting the Output Voltage

The output voltage of the regulator is determined by connecting a resistor divider from the output node ( $V_{OUT}$ ) to the FB pin as shown in Figure 3. There are trade-offs when choosing the value of the feedback resistors. If the series combination ( $R_{FB1} + R_{FB2}$ ) is too low, then the light load efficiency of the regulator will be reduced. So, to maximize the efficiency, it is best to choose higher values of resistors. On the other hand, if the parallel combination ( $R_{FB1}/R_{FB2}$ ) is too high, then the regulator may be susceptible to noise coupling onto the FB pin. 1% resistors are recommended to maintain the output voltage accuracy.



**Figure 3: Connecting a Feedback Divider to Set the Output Voltage**

The feedback resistors must satisfy the ratio shown in equation 1 below to produce a desired output voltage ( $V_{OUT}$ ).

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT}}{0.8V} - 1 \quad (1)$$

A phase lead capacitor ( $C_{FB}$ ) can be connected in parallel with  $R_{FB1}$  to increase the phase and gain margins. It adds an additional zero and pole to the compensation network and boosts the loop phase at the crossover frequency. In general,  $C_{FB}$  should be less than 25 pF. If  $C_{FB}$  is too large, it will have no effect.

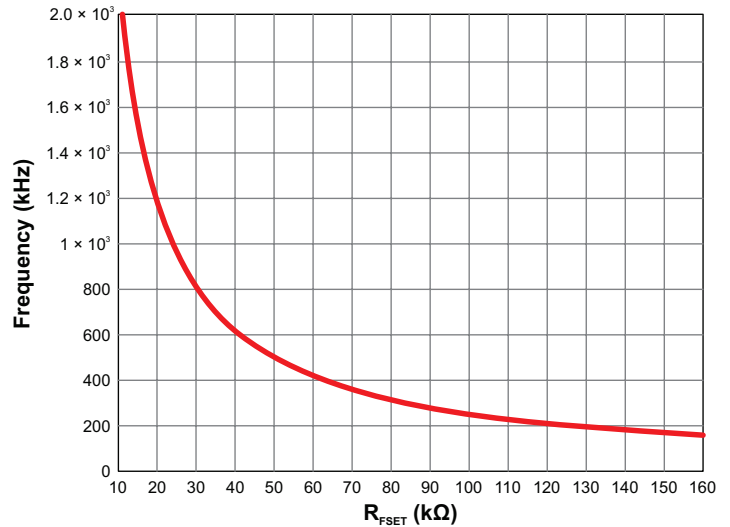
If  $C_{FB}$  is used,  $C_{FB}$  can be calculated from equation 2:

$$C_{FB} = \frac{1}{2\pi R_{FB1} f_c} \quad (2)$$

where  $f_c$  is crossover frequency.

### PWM Switching Frequency ( $f_{SW}$ , $R_{FSET}$ )

The PWM switching frequency is set by connecting a resistor from the FSET pin to ground. Figure 4 is a graph showing the relationship between the typical switching frequency (y-axis) and the FSET resistor  $R_{FSET}$  (x-axis).



**Figure 4: PWM Switching Frequency versus  $R_{FSET}$**

For a desired switching frequency ( $f_{SW}$ ), the FSET resistor can be calculated using equation 3, where  $f_{SW}$  is in kHz and  $R_{FSET}$  is in kΩ.

$$R_{FSET} = \frac{26000}{f_{SW}} - 2.2 \quad (3)$$

When the PWM switching frequency is chosen, the designer should be aware of the minimum controllable on-time,  $t_{ON(MIN)}$  of the A8654. If the system's required on-time is less than the minimum controllable on-time, pulse skipping will occur and the output voltage will have increased ripple or oscillations. The PWM switching frequency should be calculated using equation 4, where  $V_{OUT}$  is the output voltage,  $t_{ON(MIN)}$  is the minimum controllable on-time of the A8654 (See EC table), and  $V_{IN(MAX)}$  is the maximum required operational input voltage (not the peak surge voltage).

$$f_{SW} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (4)$$

If the A8654 synchronization function is employed, the base switching frequency should be chosen such that pulse skipping will not occur at the maximum synchronized switching frequency according to equation 4 (i.e.  $1.5 \times f_{SW}$  is less than the result from equation 4).

## Output Inductor ( $L_O$ )

For a peak current-mode regulator, it is common knowledge that without adequate slope compensation, the system will become unstable when the duty cycle is near or above 50%. However, the slope compensation in the A8654 is a fixed value ( $S_E$ ). Therefore, it is important to calculate an inductor value so the falling slope of the inductor current ( $S_F$ ) will work well with the A8654's slope compensation. Equations 5 and 6 can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the down slope of the inductor current. In equation 5, use the slope compensation ( $S_E$ ), which is a function of switching frequency according to equation 6.

$$\frac{V_{OUT}}{2 \times S_E} \leq L_O \leq \frac{V_{OUT}}{S_E} \quad (5)$$

$$S_E = 0.0445 \times f_{SW}^2 + 0.5612 \times f_{SW} \quad (6)$$

$S_E$  is in A/ $\mu$ s,  $f_{SW}$  is in MHz, and  $L_O$  will be in  $\mu$ H

If equations 5 or 6 yield an inductor value that is not a standard value, then the next highest available value should be used. The final inductor value should allow for 10%-20% of initial tolerance and 20%-30% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the A8654. Ideally, for output short-circuit conditions, the inductor should not saturate at the highest pulse-by-pulse current limit at minimum duty cycle; this may be too costly. At the very least, the inductor should not saturate at the peak operating current according to equation 7. In equation 7  $V_{IN(MAX)}$  is the maximum continuous input voltage.

$$I_{PEAK} = 5.3 - \frac{S_E \times V_{OUT}}{1.15 \times f_{SW} \times V_{IN(MAX)}} \quad (7)$$

Subtracting half of the inductor ripple current from equation 7 gives an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle ( $D$ ),

$$I_{OUT(DC)} \leq 5.3 - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_O} \quad (8)$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

## Output Capacitors

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage, and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin. The output voltage ripple ( $\Delta V_{OUT}$ ) is a function of the output capacitors parameters:  $C_O$ ,  $ESR_{CO}$ ,  $ESL_{CO}$ .

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_L}{8f_{SW}C_O} \quad (9)$$

The type of output capacitors will determine which terms of equation 9 are dominant.

For ceramic output capacitors, the  $ESR_{CO}$  and  $ESL_{CO}$  are virtually zero so the output voltage ripple will be dominated by the third term of equation 9.

$$\Delta V_{OUT} = \frac{\Delta I_L}{8f_{SW}C_O} \quad (10)$$

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (i.e. increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in equation 9 will be very small and the output voltage ripple will be determined primarily by the first two terms of equation 9.

$$\Delta V_{OUT} = \Delta I_L \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} \quad (11)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent  $ESR_{CO}$  and  $ESL_{CO}$  by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (i.e. increase the inductor value).

The ESR of some electrolytic capacitors can be quite high, so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the data-sheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10 $\times$ , which increases the output voltage ripple and in most cases reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of

the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient ( $di/dt$ ), the output voltage will change by the amount

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{CO} + \frac{di}{dt} ESL_{CO} \quad (12)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier will bring the output voltage back to its setpoint mainly depends on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components ( $R_Z$ ,  $C_Z$ ,  $C_P$ ) are discussed in more detail in the Compensation Components section of this datasheet.

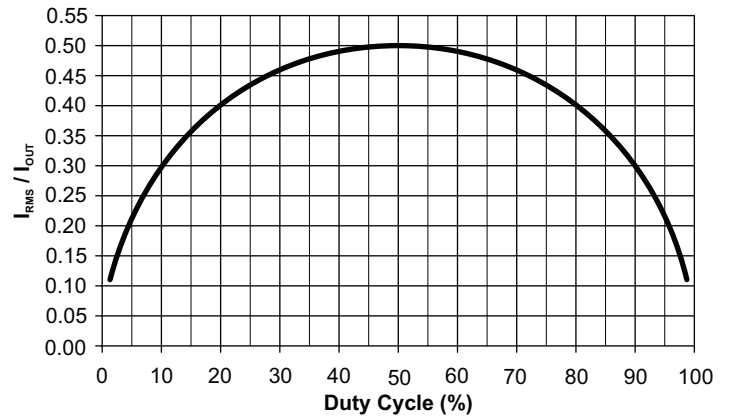
### Input Capacitors

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage  $dV/dt$  to something much less than the hysteresis of the VIN pin UVLO circuitry ( $V_{UVLO(HYS)}$ , nominally 800 mV for the A8654) at maximum loading and minimum input voltage.

The input capacitors must deliver the RMS current according to:

$$I_{RMS} = I_O \sqrt{D \times (1 - D)} \quad (13)$$

where the duty cycle  $D$  is  $D \approx V_{OUT} / V_{IN}$ . Figure 5 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle ( $D$ ) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 3.0 A of steady-state load current, the input capacitor(s) must support  $0.40 \times 3.0$  A or 1.2 A<sub>RMS</sub>.



**Figure 5: Input Capacitor Ripple vs. Duty Cycle**

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the A8654's UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}} \quad (14)$$

Where  $\Delta V_{IN(MIN)}$  is chosen to be much less than the hysteresis of the VIN UVLO comparator ( $\Delta V_{IN(MIN)} \leq 150$  mV is recommended), and  $f_{SW}$  is the nominal PWM frequency.

The  $D \times (1 - D)$  term in equation 13 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design based on  $I_{OUT} = 3.0$  A,  $f_{SW} = 85\%$  of 425 kHz,  $D \times (1 - D) = 0.25$ , and  $\Delta V_{IN} = 150$  mV,

$$C_{IN} \geq \frac{3.0 \text{ A} \times 0.25}{361 \text{ kHz} \times 150 \text{ mV}} = 14 \mu\text{F}$$

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size (i.e. 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage (such as a load dump as high as 40 V for automotive applications).

## Bootstrap Capacitor

A bootstrap capacitor must be connected between the BOOT and SW pins to provide the floating gate drive to the high-side MOSFET. Usually, 100 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

## Soft-Start and Hiccup Mode Timing ( $C_{SS}$ )

The soft-start time of the A8654 is determined by the value of the capacitance at the soft-start pin ( $C_{SS}$ ).

When the A8654 is enabled, the voltage at the soft-start pin will start from 0 V and will be charged by the soft-start current ( $I_{SS(SU)}$ ). However, PWM switching will not begin instantly because the voltage at the soft-start pin must rise above 400 mV. The soft-start delay ( $t_{SS(DELAY)}$ ) can be calculated using equation below,

$$t_{SS(DELAY)} = C_{SS} \times \left( \frac{400 \text{ mV}}{I_{SS(SU)}} \right) \quad (15)$$

If the A8654 is starting with a very heavy load, a very fast soft-start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the sum of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors

$$I_{CO} = C_O \times V_{OUT} / t_{SS}$$

is higher than the pulse-by-pulse current threshold, as shown in Figure 6. This phenomenon is more pronounced when using high value electrolytic type output capacitors.

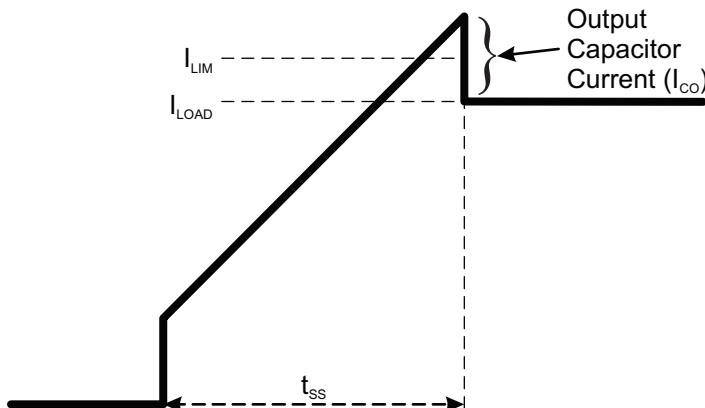


Figure 6: Output Current ( $I_{CO}$ ) During Startup

To avoid prematurely triggering hiccup mode, the soft-start capacitor ( $C_{SS}$ ) should be calculated according to equation below,

$$C_{SS} \geq \frac{I_{SS(SU)} \times V_{OUT} \times C_O}{0.8 \text{ V} \times I_{CO}} \quad (16)$$

where  $V_{OUT}$  is the output voltage,  $C_O$  is the output capacitance,  $I_{CO}$  is the amount of current allowed to charge the output capacitance during soft-start (recommend  $0.1 \text{ A} < I_{CO} < 0.3 \text{ A}$ ). Higher values of  $I_{CO}$  result in faster soft-start times. However, lower values of  $I_{CO}$  ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an  $I_{CO}$  of 0.1 A and increasing it only if the soft-start time is too slow. If a non-standard capacitor value for  $C_{SS}$  is calculated, the next larger value should be used.

The output voltage ramp time ( $t_{SS}$ ) can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}} \text{ or } 0.8 \text{ V} \times \frac{C_{SS}}{I_{SS(SU)}} \quad (17)$$

When the A8654 is in hiccup mode, the soft-start capacitor is used as a timing capacitor and sets the hiccup period. The soft-start pin charges the soft-start capacitor with  $I_{SS(SU)}$  during a startup attempt and discharges the same capacitor with  $I_{SS(HIC)}$  between startup attempts. Because the ratio of  $I_{SS(SU)}/I_{SS(HIC)}$  is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty cycle will be very low and the junction temperature will be kept low.

## Compensation Components ( $R_Z$ , $C_Z$ , $C_P$ )

To compensate the system, it is important to understand where the buck power stage, load resistance, and output capacitance form their poles and zeros in frequency. Also, it is important to understand that the (Type II) compensated error amplifier introduces a zero and two more poles and where these should be placed to maximize the system's stability, provide a high bandwidth, and optimize the transient response.

First, consider the power stage of the A8654, the output capacitors, and the load resistance. This circuitry is commonly referred as the "control to output" transfer function. The low frequency gain of this section depends on the COMP to SW current gain ( $gm_{POWER}$ ), and the value of the load resistor ( $R_L$ ). The DC gain ( $G_{CO(0HZ)}$ ) of the control-to-output is:



$$G_{CO(0Hz)} = gm_{POWER} \times R_L \quad (18)$$

The control to output transfer function has a pole ( $f_{p1}$ ) formed by the output capacitance ( $C_{OUT}$ ) and load resistance ( $R_L$ ) at:

$$f_{p1} = \frac{1}{2\pi \times R_L \times C_{OUT}} \quad (19)$$

The control to output transfer function also has a zero ( $f_{z1}$ ) formed by the output capacitance ( $C_{OUT}$ ) and its associated ESR

$$f_{z1} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad (20)$$

For a design with very low-ESR type output capacitors (i.e. ceramic or OSCON output capacitors), the ESR zero,  $f_{z1}$ , is usually at a very high frequency, so it can be ignored. On the other hand, if the ESR zero falls below or near the 0 dB crossover frequency of the system (as is the case with electrolytic output capacitors), then it should be cancelled by the pole formed by the  $C_p$  capacitor and the  $R_Z$  resistor (discussed and identified later as  $f_{p3}$ ).

Next, consider the feedback resistor divider, ( $R_{FB1}$  and  $R_{FB2}$ ), the error amplifier ( $gm$ ), and its compensation network  $R_Z$ - $C_Z$ - $C_p$ . It greatly simplifies the transfer function derivation if  $R_O \gg R_Z$ , and  $C_Z \gg C_p$  (where  $R_O$  is the error amplifier output impedance). In most cases,  $R_O > 2 \text{ M}\Omega$ ,  $1 \text{ k}\Omega < R_Z < 100 \text{ k}\Omega$ ,  $220 \text{ pF} < C_Z < 47 \text{ nF}$ , and  $C_p < 50 \text{ pF}$ , so the following equations are very accurate.

The low frequency gain of the control section ( $G_{C(0Hz)}$ ) is formed by the feedback resistor divider and the error amplifier. It can be calculated using equation 21:

$$\begin{aligned} G_{C(0Hz)} &= \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times gm \times R_O \\ &= \frac{V_{FB}}{V_{OUT}} \times gm \times R_O \\ &= \frac{V_{FB}}{V_{OUT}} \times A_{VOL} \end{aligned} \quad (21)$$

where

$V_{OUT}$  is the output voltage,

$V_{FB}$  is the reference voltage (0.8 V),

$gm$  is the error amplifier transconductance (750  $\mu\text{A/V}$ ), and

$R_O$  is the error amplifier output impedance ( $A_{VOL}/gm$ ).

The transfer function of the Type-II compensated error amp has a (very) low frequency pole ( $f_{p2}$ ) dominated by the output error amplifier's output impedance  $R_O$  and the  $C_Z$  compensation capacitor,

$$f_{p2} = \frac{1}{2\pi \times R_O \times C_Z} \quad (22)$$

The transfer function of the Type-II error amp also has a low frequency zero ( $f_{z2}$ ) dominated by the  $R_Z$  resistor and the  $C_Z$  capacitor.

$$f_{z2} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (23)$$

Lastly, the transfer function of the Type-II compensated error amp has a (very) high frequency pole ( $f_{p3}$ ) dominated by the  $R_Z$  resistor and the  $C_p$  capacitor

$$f_{p3} = \frac{1}{2\pi \times R_Z \times C_p} \quad (24)$$

Placing  $f_{z2}$  just above  $f_{p1}$  will result in excellent phase margin, but relatively slow transient recovery time.

The magnitude and phase of the entire system are simply the sum of the error amp response and the control-to-output response.

## A Generalized Tuning Procedure

1. Choose the system bandwidth,  $f_C$ , the frequency at which the magnitude of the gain will cross 0 dB. Recommended values for  $f_C$  based on the PWM switching frequency are  $f_{SW}/20 < f_C < f_{SW}/7.5$ . A higher value of  $f_C$  will generally provide a better transient response while a lower value of  $f_C$  will be easier to obtain higher gain and phase margins.
2. Calculate the  $R_Z$  resistor value to set the desired system bandwidth ( $f_C$ ),

$$R_Z = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2 \times \pi \times C_{OUT}}{gm_{POWER} \times gm} \quad (25)$$

3. Determine the frequency of the pole ( $f_{p1}$ ) formed by  $C_{OUT}$  and  $R_L$  by using equation 19 (repeated here).

$$f_{p1} = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

4. Calculate a range of values for the  $C_Z$  capacitor,

$$\frac{4}{2 \times \pi \times R_Z \times f_C} < C_Z < \frac{1}{2 \times \pi \times R_Z \times 1.5 \times f_{p1}} \quad (26)$$

To maximize system stability (i.e. have the most gain margin), use a higher value of  $C_Z$ . To optimize transient recovery time at the expense of some phase margin, use a lower value of  $C_Z$ .

5. Calculate the frequency of the ESR zero ( $f_{Z1}$ ) formed by the output capacitor(s) by using equation 20 (repeated here).

$$f_{Z1} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

- A. If  $f_{Z1}$  is at least 1 decade higher than the target crossover frequency ( $f_C$ ), then  $f_{Z1}$  can be ignored. This is usually

the case for a design using ceramic output capacitors. Use equation 24 to calculate the value of  $C_P$  by setting  $f_{P3}$  to either  $5 \times f_C$  or  $f_{SW}/2$ , whichever is higher.

- B. On the other hand, if  $f_{Z1}$  is near or below the target crossover frequency ( $f_C$ ) then use equation 24 to calculate the value of  $C_P$  by setting  $f_{P3}$  equal to  $f_{Z1}$ . This is usually the case for a design using high ESR electrolytic output capacitors.

Referring to Typical Application Diagram on the front page, several typical designs are provided in Table 2 for A8654.

**Table 2: Recommended Components Values for Three Typical Designs**

$f_{SW}$	$V_{OUT}$	$R_{FSET}$	$L_O$	$C_O$	$R_Z + C_Z // C_P$	$R_{FB1}$	$R_{FB2}$
500 kHz	5.0 V	52.3 k $\Omega$	10 $\mu$ H (74437368100)	44 $\mu$ F	14 k $\Omega$ + 2.7 nF/33 pF	24.9 k $\Omega$	4.75 k $\Omega$
1 MHz	3.3 V	23.7 k $\Omega$	6.8 $\mu$ H (74437368068)	44 $\mu$ F	14 k $\Omega$ + 2.2 nF/15 pF	16.5 k $\Omega$	5.23 k $\Omega$
2 MHz	5.0 V	10.5 k $\Omega$	6.8 $\mu$ H (74437368068)	32 $\mu$ F	37.4 k $\Omega$ + 1.8 nF/4.7 pF	24.9 k $\Omega$	4.75 k $\Omega$

## POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the A8654 is the sum of the power dissipated from the  $V_{IN}$  supply current ( $P_{IN}$ ), the power dissipated due to the switching of the high-side power MOSFET ( $P_{SW1}$ ), the power dissipated due to the RMS current being conducted by the high-side MOSFET ( $P_{COND1}$ ) and low-side MOSFET ( $P_{COND2}$ ), and the power dissipated by both gate drivers ( $P_{DRIVER}$ ).

The power dissipated from the  $V_{IN}$  supply current can be calculated using equation 27,

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times (Q_{G1} + Q_{G2}) \times f_{SW} \quad (27)$$

where

$V_{IN}$  is the input voltage,

$I_Q$  is the input quiescent current drawn by the A8654 (see EC table),

$V_{GS}$  is the MOSFET gate drive voltage (typically 5 V),

$Q_{G1}$  and  $Q_{G2}$  is the internal high-side and low-side MOSFET gate charges (approximately 5.8 nC and 10.4 nC, respectively), and

$f_{SW}$  is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using equation 28,

$$P_{SW1} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \quad (28)$$

where

$V_{IN}$  is the input voltage,

$I_{OUT}$  is the regulator output current,

$f_{SW}$  is the PWM switching frequency, and

$t_r$  and  $t_f$  are the rise and fall times measured at the SW node.

The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both  $t_r$  and  $t_f$  range from 10 to 20 ns.

The power dissipated by the high-side MOSFET while it is conducting can be calculated using equation 29,

$$P_{COND1} = I_{RMS(FET)}^2 \times R_{DS(ON)HS} = \left( \frac{V_{OUT}}{V_{IN}} \right) \times \left( I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \times R_{DS(ON)HS} \quad (29)$$

Similarly, the conduction losses dissipated by the low-side MOSFET while it is conducting can be calculated by the following equation:

$$P_{COND2} = I_{RMS(FET)}^2 \times R_{DS(ON)LS} = \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \times \left( I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right) \times R_{DS(ON)LS} \quad (30)$$

where

$I_{OUT}$  is the regulator output current,

$\Delta I_L$  is the peak-to-peak inductor ripple current,

$R_{DS(ON)HS}$  is the on-resistance of the high-side MOSFET,

$R_{DS(ON)LS}$  is the on-resistance of the low-side MOSFET

The  $R_{DS(ON)}$  of both MOSFETs have some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an  $R_{DS(ON)}$  with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated from the low-side MOSFET body diode during the non-overlap time can be calculated as follows:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW} \quad (31)$$

where

$V_{SD}$  is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and

$t_{NO}$  is the non-overlap time (15 ns(typ))

The sum of the power dissipated by the internal gate driver can be calculated using equation 32,

$$P_{DRIVER} = (Q_{G1} + Q_{G2}) \times V_{GS} \times f_{SW} \quad (32)$$

where

$V_{GS}$  is the gate drive voltage (typically 5 V),

$Q_{G1}$  and  $Q_{G2}$  is the gate charges to drive high-side and low-side MOSFETs to  $V_{GS} = 5$  V (about 5.8 nC and 10.4 nC respectively), and

$f_{SW}$  is the PWM switching frequency.

Finally, the total power dissipated by the A8654 ( $P_{TOTAL}$ ) is the sum of the previous equations,

$$P_{TOTAL} = P_{IN} + P_{SW1} + P_{COND1} + P_{COND2} + P_{NO} + P_{DRIVER} \quad (33)$$



The average junction temperature can be calculated with the equation below,

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A \quad (34)$$

where

$P_{TOTAL}$  is the total power dissipated from equation 33,

$R_{\theta JA}$  is the junction-to-ambient thermal resistance (34°C/W on a 4-layer PCB), and

$T_A$  is the ambient temperature.

The maximum junction temperature will be dependent on how

efficiently heat can be transferred from the PCB to the ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are trade-offs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

## PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical for the A8654 to provide clean, stable output voltages. Follow these guidelines to ensure a good PCB layout. Figure 7 shows a typical buck converter schematic with the critical power paths/loops. Figure 8 shows an example PCB component placement and routing with the same critical power paths/loops from the schematic.

1. Place the ceramic input capacitors as close as possible to the VIN pin and GND pins to make the loop area minimal; and the traces of the input capacitors to VIN pin should be short and wide to minimize the inductance. This critical loop is shown as Trace 1 in Figure 7 and Figure 8. The larger input capacitor can be located further away from VIN pin. The input capacitors and A8654 IC should be on the same side of the board with traces on the same layer.
2. The loop from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground should be minimized with relatively wide traces.
3. When the high-side MOSFET is off, free-wheeling current flows from ground, through the synchronous low-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces. This loop is shown as Trace 2 in Figure 7 and Figure 8.
4. Place the output capacitors relatively close to the output inductor ( $L_O$ ) and the A8654. Ideally, the output capacitors, output inductor and the controller IC A8654 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection to the GND. These critical connections are shown as Trace 3 in Figure 7.
5. Place the output inductor ( $L_O$ ) as close as possible to the SW pin with short and wide traces. This critical trace is shown as Trace 4 in Figure 7 and Figure 8. The SW node voltage transitions from 0 V to  $V_{IN}$  and with a high  $dV/dt$  rate. This node is the root cause of many noise issues. It is suggested to minimize the SW copper area to minimize the coupling capacitance between SW node and other noise-sensitive nodes. However, the SW node area cannot be too small in order to conduct high current. A ground copper area can be placed beneath the SW node to provide additional shielding. Also, keep low-level analog signals (like FB, COMP) away from the SW polygon.
6. Place the feedback resistor divider ( $R_{FB1}$  and  $R_{FB2}$ ) very close to the FB pin. Make the ground side of  $R_{FB2}$  as close as possible to the A8654.
7. Place the compensation components ( $R_Z$ ,  $C_Z$ , and  $C_P$ ) as close as possible to the COMP pin. Also make the ground side of  $C_Z$  and  $C_P$  as close as possible to the A8654.
8. Place the FSET resistor as close as possible to the SYNC/FSET pin. Place the soft-start capacitor  $C_{SS}$  as close as possible to the SS pin.
9. The output voltage sense trace (from VOUT to  $R_{FB1}$ ) should be connected as close as possible to the load to obtain the best load regulation.
10. Place the bootstrap capacitor ( $C_{BOOT}$ ) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible.
11. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors.
12. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.
13. The thermal pad under the A8654 IC should be connected to the GND plane (preferably on the top and bottom layer) with as many vias as possible. Allegro recommends vias with an approximately 0.25 to 0.30 mm hole and a 0.13 and 0.18 mm ring.
14. EMI/EMC issues are always a concern. Allegro recommends having locations for an RC snubber from SW to ground. The resistor should be 0805 or 1206 size.

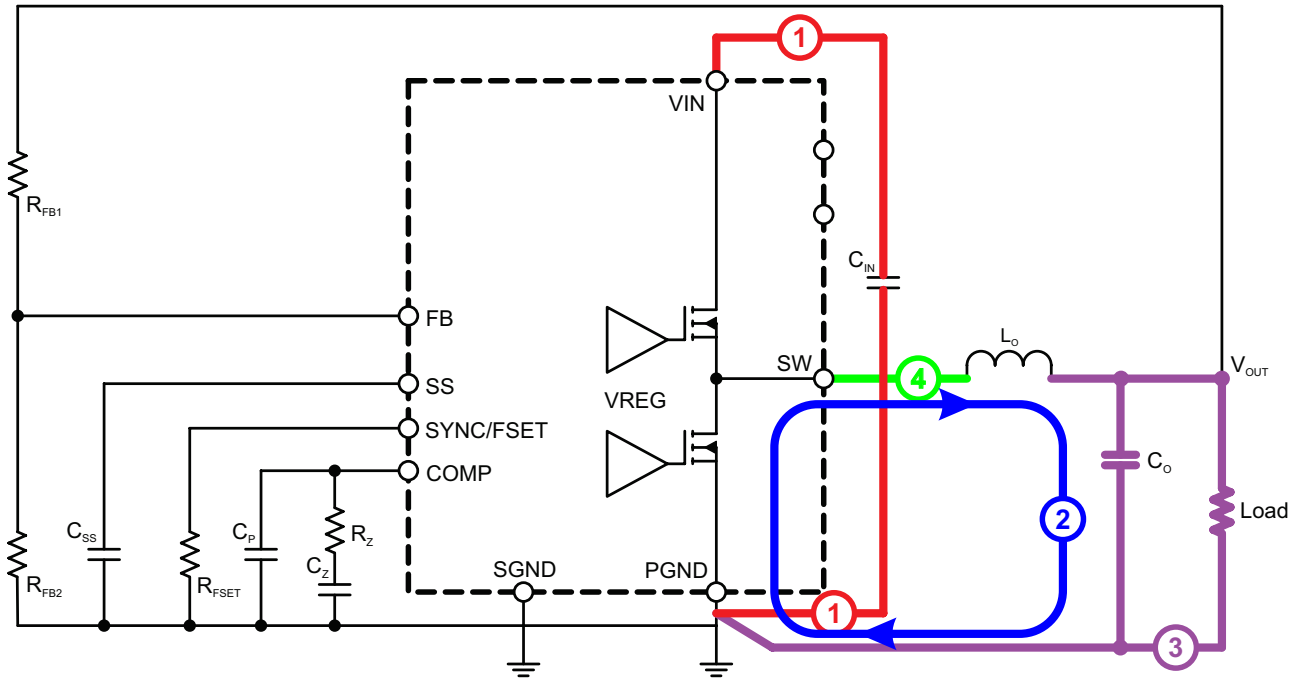


Figure 7: Typical Synchronous Buck Regulator

A single-point ground is recommended, which could be the exposed thermal pad under the IC.

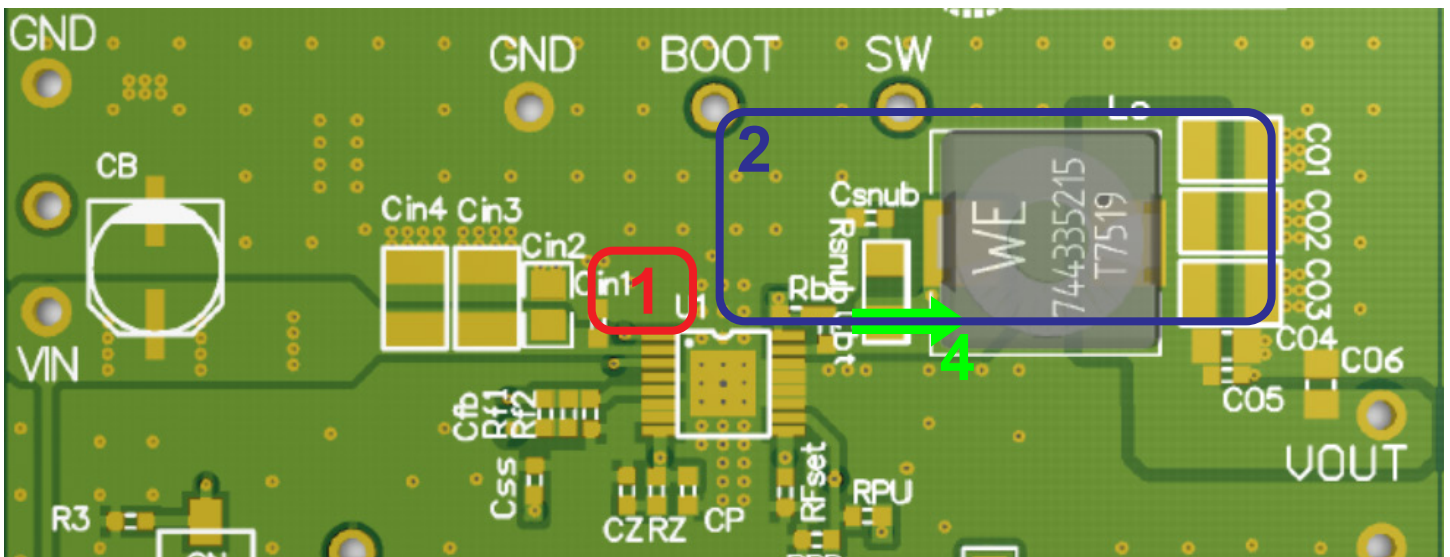


Figure 8: Example PCB Component Placement and Routing

## PACKAGE OUTLINE DRAWING

### For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

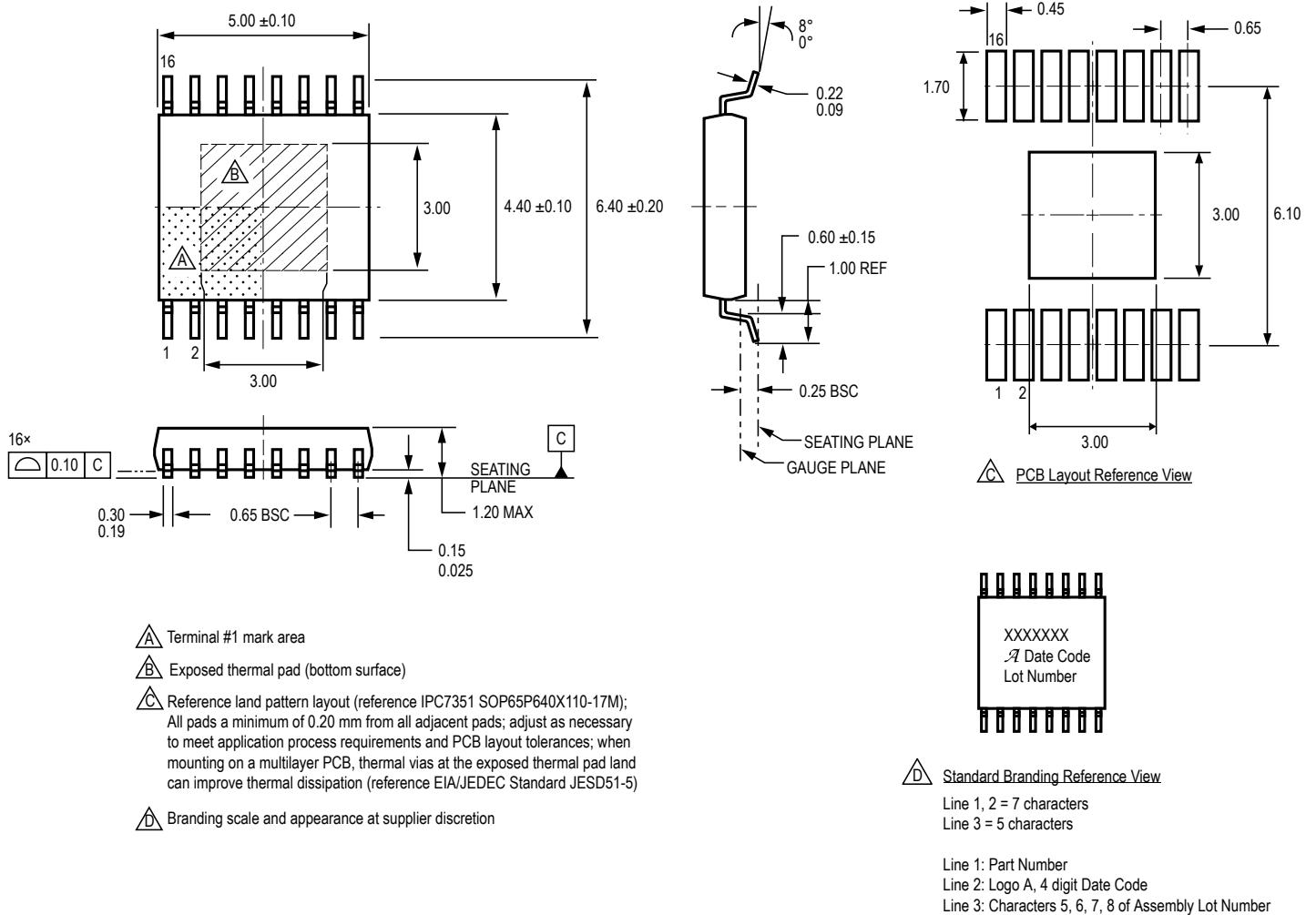


Figure 9: Package LP, 16-Pin eTSSOP with Exposed Thermal Pad

## Revision Table

Number	Date	Description
–	February 10, 2015	Initial Release
1	March 4, 2016	Added AEC-Q100 qualification to Features and Benefits
2	April 6, 2016	Updated Electrical Characteristics table: SW Leakage Current, PWM Switching Frequency (page 6), Peak Inductor (Pulse-by-Pulse) Current Limit, Slope Compensation, SS Maximum Charge Voltage, SS Switching Frequency, $V_{OUT}$ UV Threshold (page 7); Multiple editorial changes (all pages).
3	April 22, 2020	Minor editorial updates
4	November 13, 2020	Minor editorial updates
5	November 19, 2021	Updated package drawing (page 28)

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